RX63N Group, RX631 Group

Clock Synchronous SCIc Communication Using the DMACA

R01AN1064EJ0100
Rev.1.00
Apr. 05, 2013

Abstract

This application note describes a method for clock synchronous serial communication using the RX63N and RX631's DMA controller (DMAC) and serial communication interface (SCI)

Products

- RX63N Group, 177- and 176-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 145- and 144-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 100-pin version, ROM capacity: 768 KB to 2 MB
- RX631 Group, 177- and 176-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 145- and 144-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 100-pin version, ROM capacity: 256 KB to 2 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This sample program performs clock synchronous serial transmission and reception using the SCI module.

The transmit data is stored in advance in a RAM transmit data storage area and is transferred using a DMAC. The receive data is transferred to the RAM receive data storage area using a DMAC.

Serial communication is started when a falling edge is detected on the interrupt request pin (IRQ15).

- Transfer rate: 38,400 bps
- Communication format: 8 bits, LSB first
- Clock input/output: Clock output (master)
- Transmission/reception operation: Transmission and reception can be performed at the same time.

Table 1.1 lists the peripheral function used and their applications and figure 1.1 shows the block diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
SCIc channel 9 (SCI9)	Clock synchronous serial transmission and reception
DMACA channel 0 (DMAC0)	Transfer of SCI receive data to RAM
DMACA channel 1 (DMAC1)	Transfer of RAM transmit data to the SCI module
IRQ15	Start trigger for serial transmission or reception

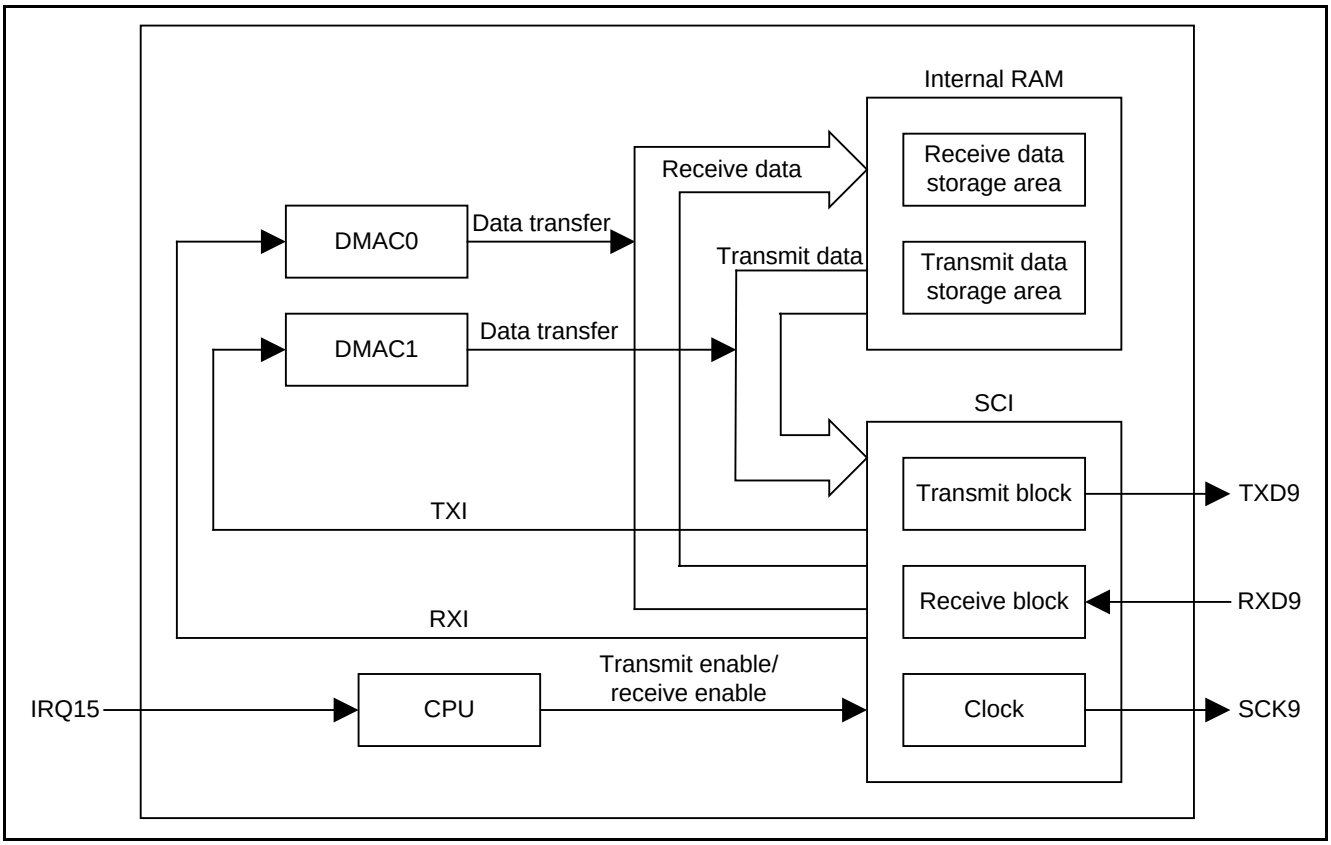


Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Description
Microcontroller used	R5F563NBDDFC (RX63N Group)
Operating frequency	Main clock: 12 MHz PLL: 192 MHz (Main clock divided by 1 and multiplied by 16) System clock (ICLK): 96 MHz (PLL divided by 2) Peripheral module clock B (PCLKB): 48 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V.1.02 Release 01
	Compiler options -cpu=rx600 -output=obj="$(CONFIGDIR)\$(FILELEAF).obj" -debug -nologo (The integrated development environment default settings are used.)
iodefine.h version	Version 1.50
Endian order	Little-endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit+ for RX63N (Product number: R0K50563NC000BE)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX63N Group, RX631 Group Initial Setting Rev.1.00 (R01AN1245EJ0100_RX63N)

The initialization functions from the above application note are used by the sample code in this application note. The revision number shown is the one used when this application note was written.

If there is a more recent version, use the latest version. Check the Renesas Electronics Corporation web site to verify and download the latest version.

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows a connection example.

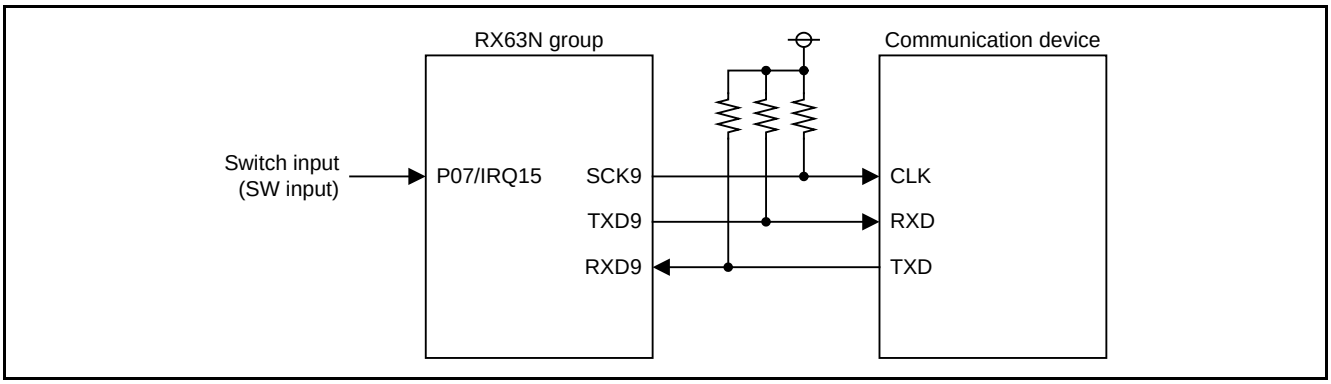


Figure 4.1 Connection Example

4.2 Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P07/IRQ15	Input	Transmit/receive start switch input
PB5/SCK9	Output	SCI9 clock output
PB6/RXD9	Input	SCI9 receive data input
PB7/TXD9	Output	SCI9 transmit data output

5. Software

This sample code implements automatic SCI transmission and reception operations by using the DMAC. When the transmit/receive start switch is pressed a SCI transmit/receive operation is started.

If transmission is enabled and a TXI9 interrupt request occurs, it functions as a DMAC1 transfer request. DMAC1 transfers data in the transmit data storage area to the TDR register and that data is transmitted.

If a reception completes, an RXI9 interrupt request is generated and it functions as a DMAC0 transfer request. DMAC0 is used to transfer the receive data to the receive data storage area.

When the transfer of transmit data has been performed 256 times, a DMAC1 interrupt is generated. This disables the TXI9 interrupt and enables the TEI9 interrupt.

When the transfer of receive data has been performed 256 times, a DMAC0 interrupt is generated. This disables the RXI9 interrupt and sets the reception complete flag to 1. If the transmission complete flag is 1 at this time, SCI transmit/receive operations are disabled.

When 256 bytes of transmissions and 256 bytes of receptions have been completed, a TEI9 interrupt is generated. This disables the TEI9 interrupt and sets the transmission complete flag to 1. If the reception complete flag is 1 at this time, SCI transmit/receive operations are disabled.

The settings of the peripheral functions are listed below.

SCI9

- Communication mode: Clock synchronous
- SCK9 pin: Internal clock output (master)
- Clock source: PCLKB/4
- Transfer rate: 38,400 bps (BRR register setting = (PCLKB/(8×2×38,400 bps)) -1)
- Transmit operation: Enabled
- Receive operation: Enabled
- Data transfer direction: LSB first
- Interrupts used: Transmission complete interrupt (TEI9)
  Transmit data empty interrupt (TXI9)
  Receive data full interrupt (RXI9)
  Receive error interrupt (ERI9)

DMAC0

- Start factor: RXI9 interrupt request
  The IR flag for the RXI9 interrupt is cleared to 0 at the start of transfer.
- Transfer source address: SCI9.RDR register
- Transfer source address update mode: Fixed address
- Transfer destination address: RAM (start address of the receive data storage area)
- Transfer destination address update mode: Increment
- Transfer mode: Normal mode
- Data transfer size: 8 bits
- Transfer count: 256 transfers
- Interrupts used: Transfer complete interrupt (DMAC0I)

DMAC1

- Start factor: TXI9 interrupt request
  The IR flag for the TXI9 interrupt is cleared to 0 at the start of transfer.
- Transfer source address: RAM (start address of the transmit data storage area)
- Transfer source address update mode: Increment
- Transfer destination address: SCI9.TDR register
- Transfer destination address update mode: Fixed address
- Transfer mode: Normal mode
- Data transfer size: 8 bits
- Transfer count: 256 transfers
- Interrupts used: Transfer complete interrupt (DMAC1I)

IRQ15 input pin

- Detection method: Falling edge detection
- Digital filter: Enabled (sampling clock: PCLKB/8)
- Interrupts used: None

5.1 Operational Overview

5.1.1 Transmit Operation

(1) Initialization
After initialization, the sample code waits for a transmit/receive start switch input.

(2) Transmit/receive start switch input detection
When a transmit/receive start switch input is detected, the IRQ15 interrupt IR flag is set to 0. After verifying that transmission and reception have completed by checking the transmission complete flag and the reception complete flag, the transmission complete flag is set to 0 (transmission in progress). The DMAC1 transfer source address and transfer count are set and DMA transfers are enabled.
The SCI9.SCR.TEIE, TIE, RIE, TE, and RE bits are all set to 1 at the same time to enable transmission and reception operations. The TXI9 interrupt IR flag is set to 1 by the SCI9.TCR.TIE and TE bits being set to 1 at the same time.

(3) Data transfer start
When the TXI9 interrupt is enabled, DMAC1 is started and the TXI9 interrupt IR flag is set to 0. The first byte of transmit data is transferred from the RAM transmit data storage area to the SCI9.TSR register.

(4) Data transmission start
Data is transferred from the SCI9.TDR register to the SCI9.TSR register, the TXI9 interrupt IR flag is set to 1, and the first byte of transmit data is output from the TXD9 pin. DMAC1 is started by the TXI9 interrupt request and the second byte of transmit data is transferred.

(5) DMAC1I interrupt
When the 256th data transfer completes, a DMAC1I interrupt request is generated. The TXI9 interrupt is disabled and the TEI9 interrupt is enabled during DMAC1I interrupt handling.

(6) TEI9 interrupt
Since the SCI9.TDR register is not updated when the last bit of the 256th byte is transmitted, a TEI9 interrupt request is generated. During TEI9 interrupt handling, the TEI9 interrupt is disabled and the transmission complete flag is set to 1 (transmission complete). If the reception complete flag is 1 (reception complete), transmission and reception are disabled.
Execution is then repeated from step (2) above.

Figure 5.1 shows the timing chart for the transmission operation.

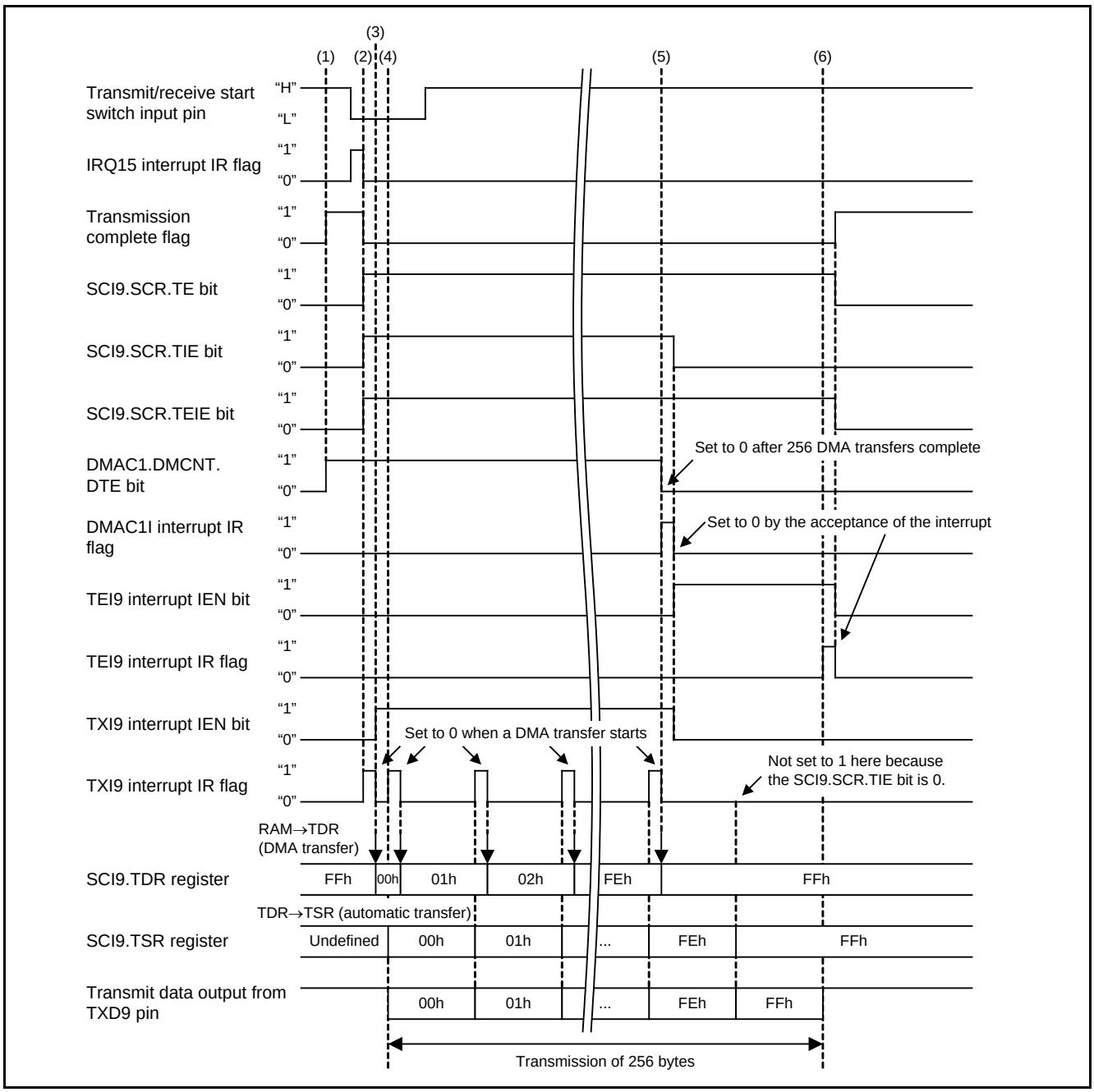


Figure 5.1 Transmission Operation Timing Chart

5.1.2 Reception Operation

(1) Initialization

After initialization, the sample code waits for a transmit/receive start switch input.

(2) Transmit/receive start switch input detection

When a transmit/receive start switch input is detected, the IRQ15 interrupt IR flag is set to 0. After verifying that transmission and reception have completed by checking the transmission complete flag and the reception complete flag, the reception complete flag is set to 0 (reception in progress). The DMAC0 transfer destination address and transfer count are set and DMA transfers are enabled.

The SCI9.SCR.TEIE, TIE, RIE, TE, and RE bits are all set to 1 at the same time to enable transmission and reception operations and the RXI9 interrupt.

(3) Data reception completion

When reception of the first byte of data completes, the data is transferred from the SCI9.RSR register to the SCI9.RDR register and the RXI9 interrupt IR flag is set to 1.

(4) Data transfer start

DMAC0 is started by the RXI9 interrupt request and the RXI9 interrupt IR flag is cleared to 0. The first byte of receive data is transferred from the SCI9.RDR register to the RAM receive data storage area.

(5) DMAC0I interrupt

When the 256th data transfer completes, a DMAC0I interrupt request is generated. During DMAC0I interrupt handling, the RXI9 interrupt is disabled and the reception complete flag is set to 1 (reception complete). If the transmission complete flag is 1 (transmission complete), transmission and reception are disabled. Execution is then repeated from step (2) above.

Figure 5.2 shows the timing chart for the transmission operation.

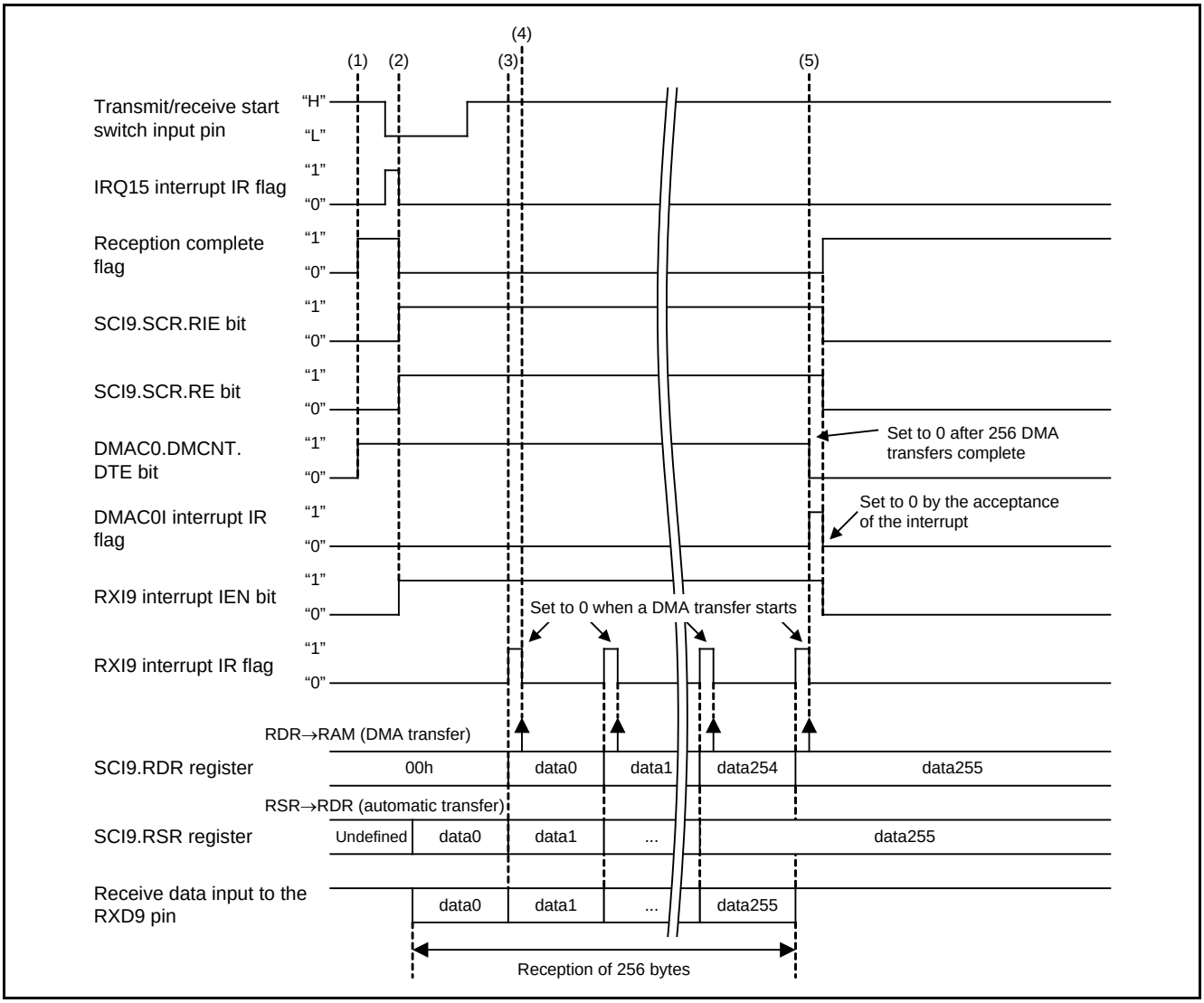


Figure 5.2 Reception Operation Timing Chart

Notes on Embedding the Sample Code in the User System

When embedding the sample code from this application note in the actual system, note the following:

- When operating in slave mode, if the interrupts used in this application are forced to wait for extended periods due to, for example, the handling of other interrupts, this code may not operate correctly.

5.2 File Composition

Table 5.1 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 5.1 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing	
r_init_stop_module.c	Stops peripheral modules that are operating after a reset	
r_init_stop_module.h	Header file for r_init_stop_module.c	
r_init_non_existent_port.c	Initialization for ports that do not exist	
r_init_non_existent_port.h	Header file for r_init_non_existent_port.c	
r_init_clock.c	Initialization for clock	
r_init_clock.h	Header file for r_init_clock.c	

5.3 Option-Setting Memory

Table 5.2 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 5.2 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	Stops IWDT after a reset Stops WDT after a reset
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	Disables voltage monitoring 0 resets after a reset Disables HOCO oscillation after a reset
MDES	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little-endian

5.4 Constants

Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
MASTER	00h	Set value of the SCI9.SCR.CKE[1:0] bits: Internal clock (master)
SLAVE	02h	Set value of the SCI9.SCR.CKE[1:0] bits: External clock (slave)
SCI_CLK	MASTER	Set value of the SCI9.SCR.CKE[1:0] bits: Master mode selected
BUF_SIZE	256	Size of the transmission and reception data storage areas
DMAC_CNT	BUF_SIZE	DMAC transfer count
SW_ON	1	Switch input on state
SW_OFF	0	Switch input off state

5.5 Variable

Table 5.4 lists the global variables.

Table 5.4 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	rcv_end_flag	Reception complete flag 0: Reception in progress 1: Reception complete	main Excep_DMAC_DMAC0I Excep_SCI9_TEI9
unsigned char	trn_end_flag	Transmission complete flag 0: Transmission in progress 1: Transmission complete	main Excep_DMAC_DMAC0I Excep_SCI9_TEI9
unsigned char	rcvbuf[BUF_SIZE]	Receive data storage area	dmac0_init sci9_start
unsigned char	trnbuf[BUF_SIZE]	Transmit data storage area	main dmac1_init sci9_start

5.6 Functions

Table 5.5 lists the functions used in the sample code.

Table 5.5 Functions Used in the Sample Code

Function Name	Outline
main	Main processing
port_init	Port initialization
R_INIT_StopModule	Stop processing for active peripheral functions after a reset
R_INIT_NonExistentPort	Nonexistent port initialization
R_INIT_Clock	Clock initialization
peripheral_init	Peripheral function initialization
sci9_init	SCI9 initialization
dmac0_init	DMAC0 initialization
dmac1_init	DMAC1 initialization
sci9_start	Starts SCI9 transmission and reception
Excep_DMAC_DMAC0I	DMAC0 transfer complete interrupt handler
Excep_DMAC_DMAC1I	DMAC1 transfer complete interrupt handler
Excep_SCI9_TEI9	SCI9 transmission complete interrupt handler
Excep_ICU_GROUP12	Group 12 interrupt handler (SCI9 receive error interrupt)

5.7 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	After initialization, this function starts SCI9 transmission and reception operations when a transmit/receive start switch input is detected.
Arguments	None
Return Value	None

port_init	
Outline	Port initialization
Header	None
Declaration	void port_init(void)
Description	Initializes the ports.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Stop processing for active peripheral functions after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Configures the setting to enter the module-stop state.
Arguments	None
Return Value	None
Remarks	Transition to the module-stop state is not performed in the sample code. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.00 application note for details of this function.

R_INIT_NonExistentPort	
Outline	Nonexistent port initialization
Header	r_init_non_existent_port.h
Declaration	void R_INIT_NonExistentPort(void)
Description	Initializes port direction registers for ports that does not exist in products with less than 176 pins.
Arguments	None
Return Value	None
Remarks	The number of pins in the sample code is set for the 176-pin package (PIN_SIZE=176). After this function is called, when writing in byte units to the PDR registers or PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.00 application note for details of this function.

R_INIT_Clock	
Outline	Clock initialization
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Initializes the clock.
Arguments	None
Return Value	None
Remarks	The sample code selects processing which uses PLL as the system clock without using the sub-clock. Refer to the RX63N Group, RX631 Group Initial Setting Rev. 1.00 application note for details of this function.

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Description	Initializes the peripheral functions used.
Arguments	None
Return Value	None

sci9_init	
Outline	SCI9 initialization
Header	None
Declaration	void sci9_init(void)
Description	Initializes SCI9.
Arguments	None
Return Value	None

dmac0_init	
Outline	DMAC0 initialization
Header	None
Declaration	void dmac0_init(void)
Description	Initializes DMAC0.
Arguments	None
Return Value	None

dmac1_init	
Outline	DMAC1 initialization
Header	None
Declaration	void dmac1_init(void)
Description	Initializes DMAC1.
Arguments	None
Return Value	None

sci9_start	
Outline	Starts SCI9 transmission and reception
Header	None
Declaration	void sci9_start(void)
Description	Starts the SCI9 transmission and reception operation.
Arguments	None
Return Value	None

Excep_DMAC_DMAC0I	
Outline	DMAC0 transfer complete interrupt handler
Header	None
Declaration	void Excep_DMAC_DMAC0I(void)
Description	Disables the RXI9 interrupt and sets the reception complete flag. If the transmission complete flag is 1, it disables SCI9 transmission and reception.
Arguments	None
Return Value	None

Excep_DMAC_DMAC1I	
Outline	DMAC1 transfer complete interrupt handler
Header	None
Declaration	void Excep_DMAC_DMAC1I(void)
Description	Disables the TXI9 interrupt and enables the TEI9 interrupt.
Arguments	None
Return Value	None

Excep_SCI9_TEI9	
Outline	SCI9 transmission complete interrupt handler
Header	None
Declaration	void Excep_SCI9_TEI9(void)
Description	Disables the TEI9 interrupt and sets the transmission complete flag. If the reception complete flag is 1, it disables SCI9 transmission and reception.
Arguments	None
Return Value	None

Excep_ICU_GROUP12	
Outline	Group 12 interrupt handler (SCI9 receive error interrupt)
Header	None
Declaration	void Excep_ICU_GROUP12 (void)
Description	Handles group 12 interrupts (SCI9 receive error interrupt).
Arguments	None
Return Value	None
Remarks	This sample code does not perform the SCI9 receive error handling; it simply executes an infinite loop. Add a program if required.

5.8 Flowcharts

5.8.1 Main Processing

Figure 5.3 shows the flowchart for the main processing.

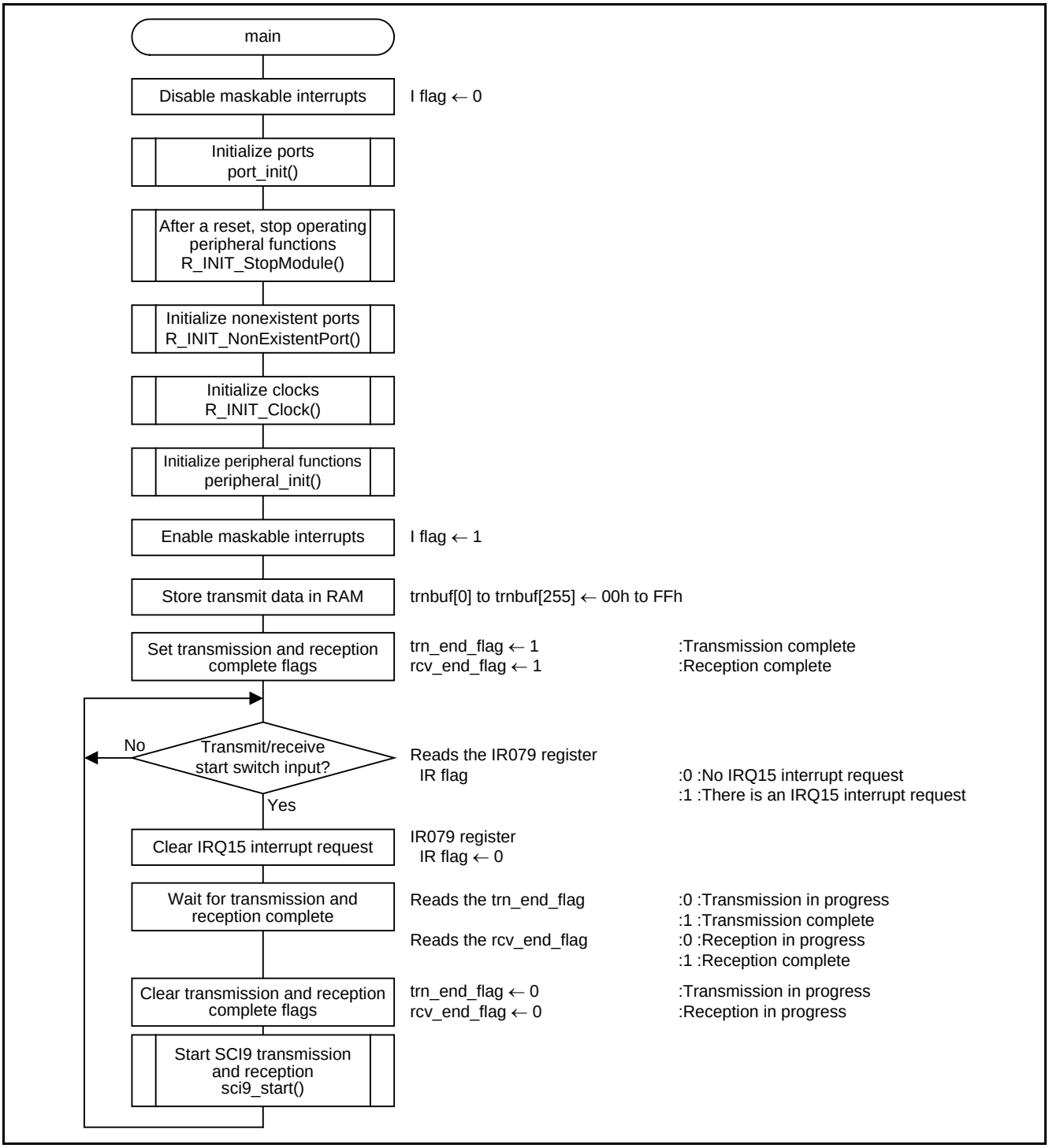


Figure 5.3 Main Processing

5.8.2 Port Initialization

Figure 5.4 shows the flowchart for the port initialization.

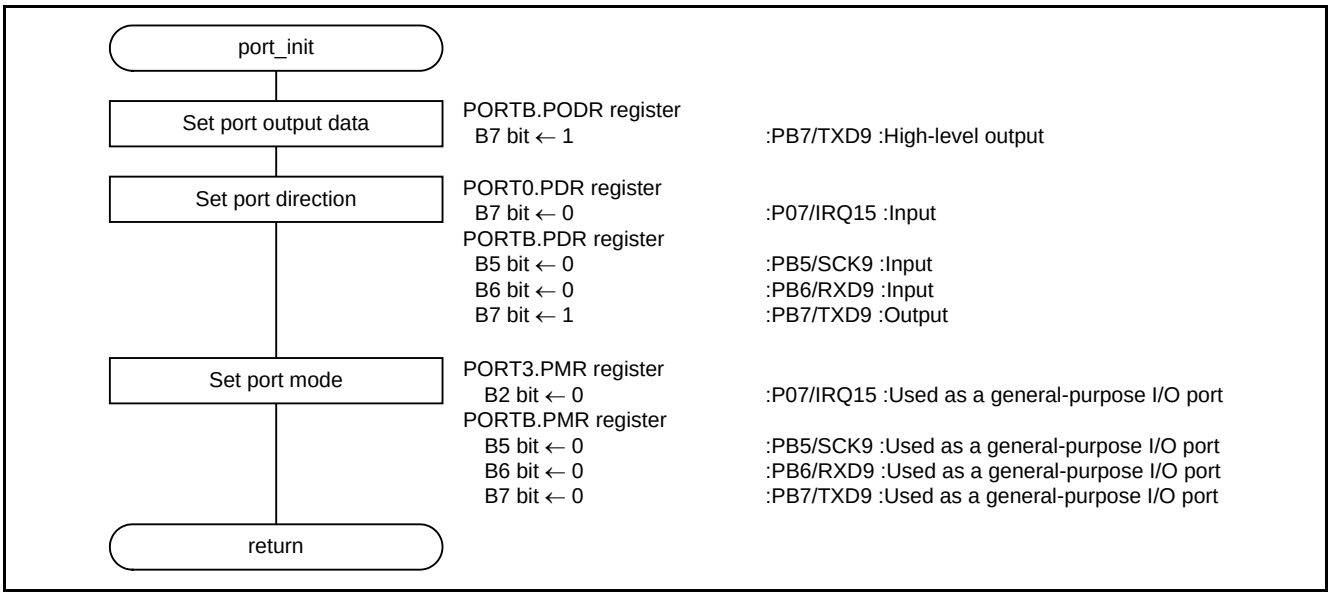


Figure 5.4 Port Initialization

5.8.3 Peripheral Function Initialization

Figure 5.5 shows the flowchart for the peripheral function initialization.

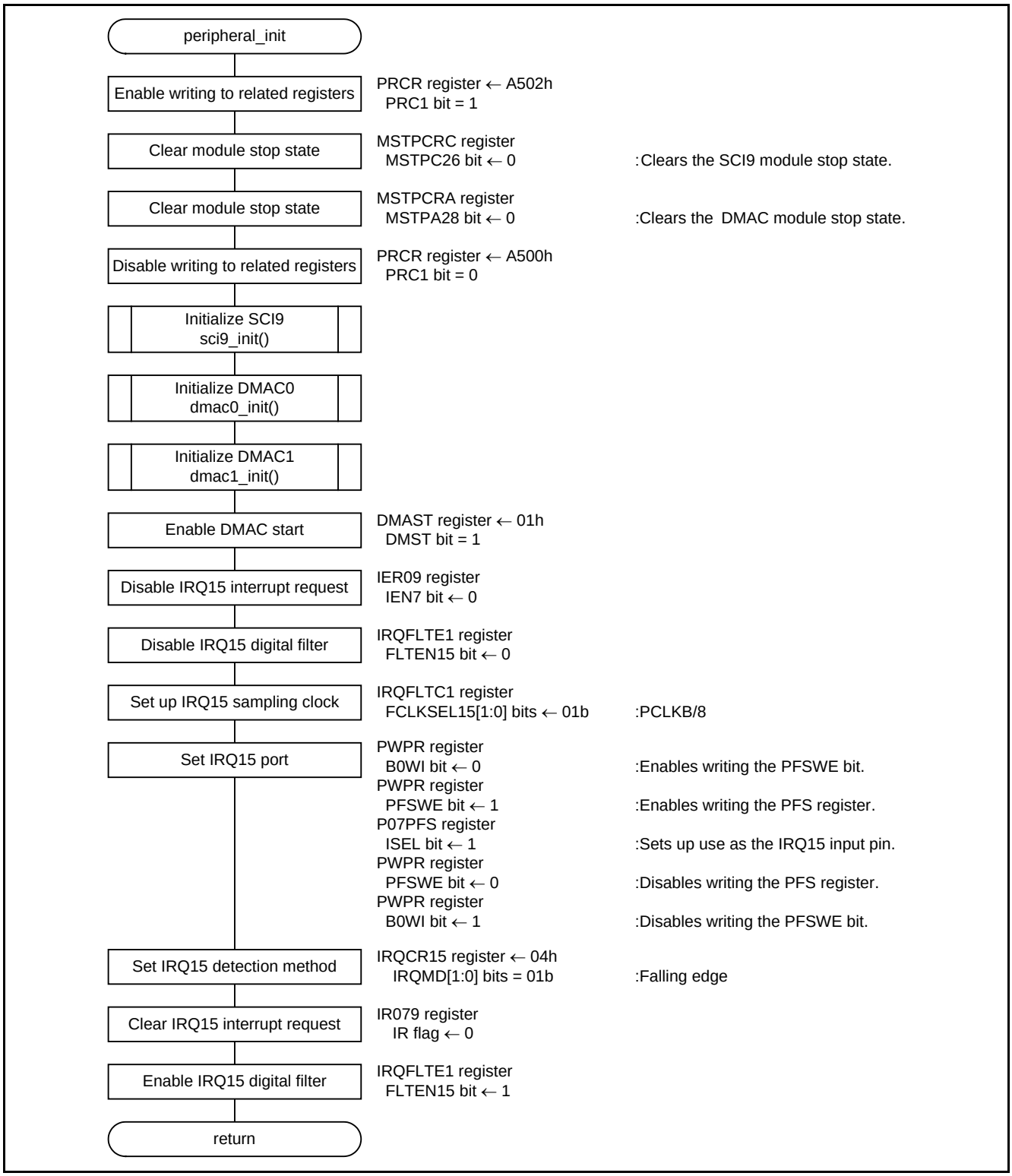


Figure 5.5 Peripheral Function Initialization

5.8.4 SCI9 Initialization

Figure 5.6 shows the flowchart for the SCI9 initialization.

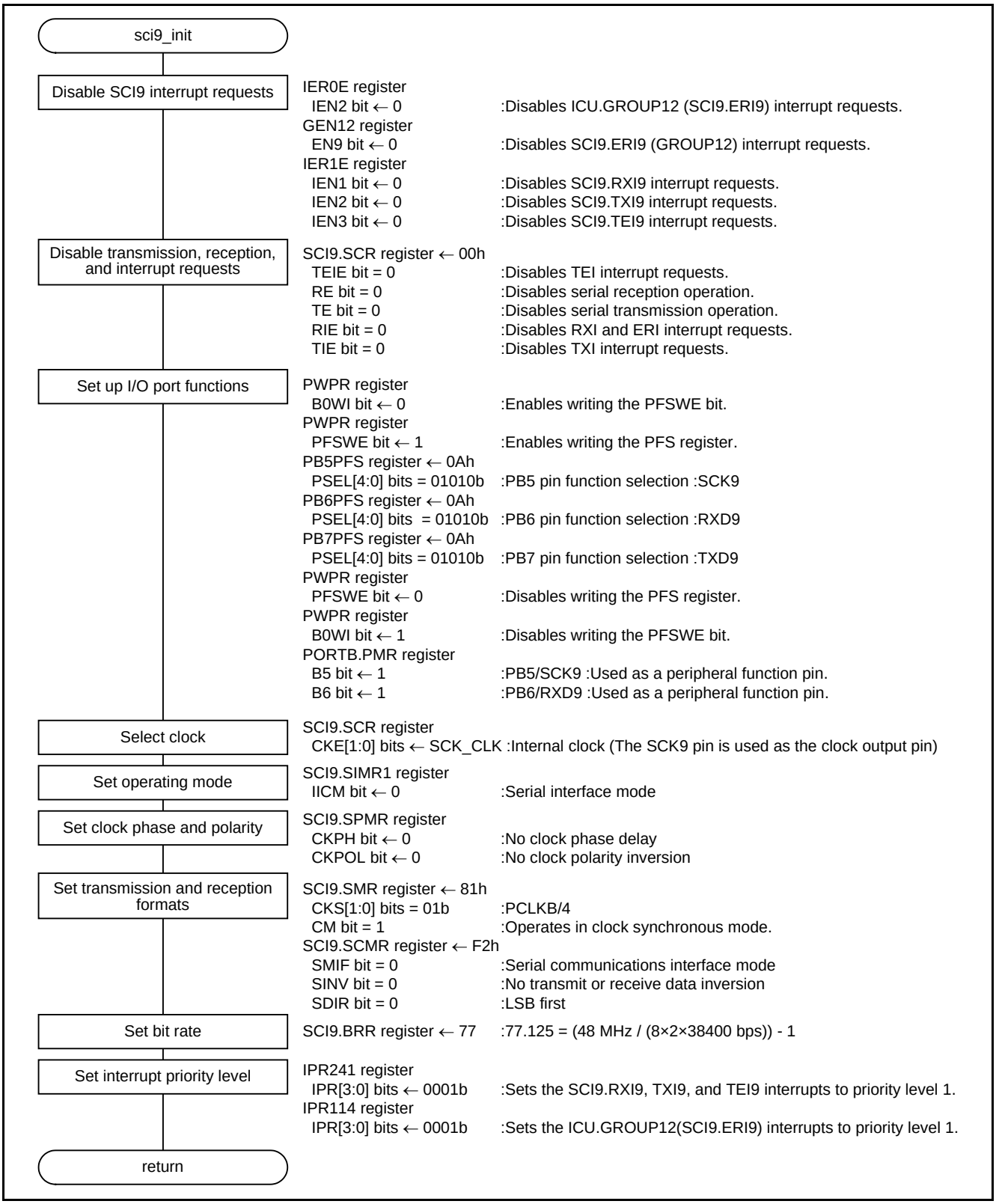


Figure 5.6 SCI9 Initialization

5.8.5 DMAC0 Initialization

Figure 5.7 shows the flowchart for the DMAC0 initialization.

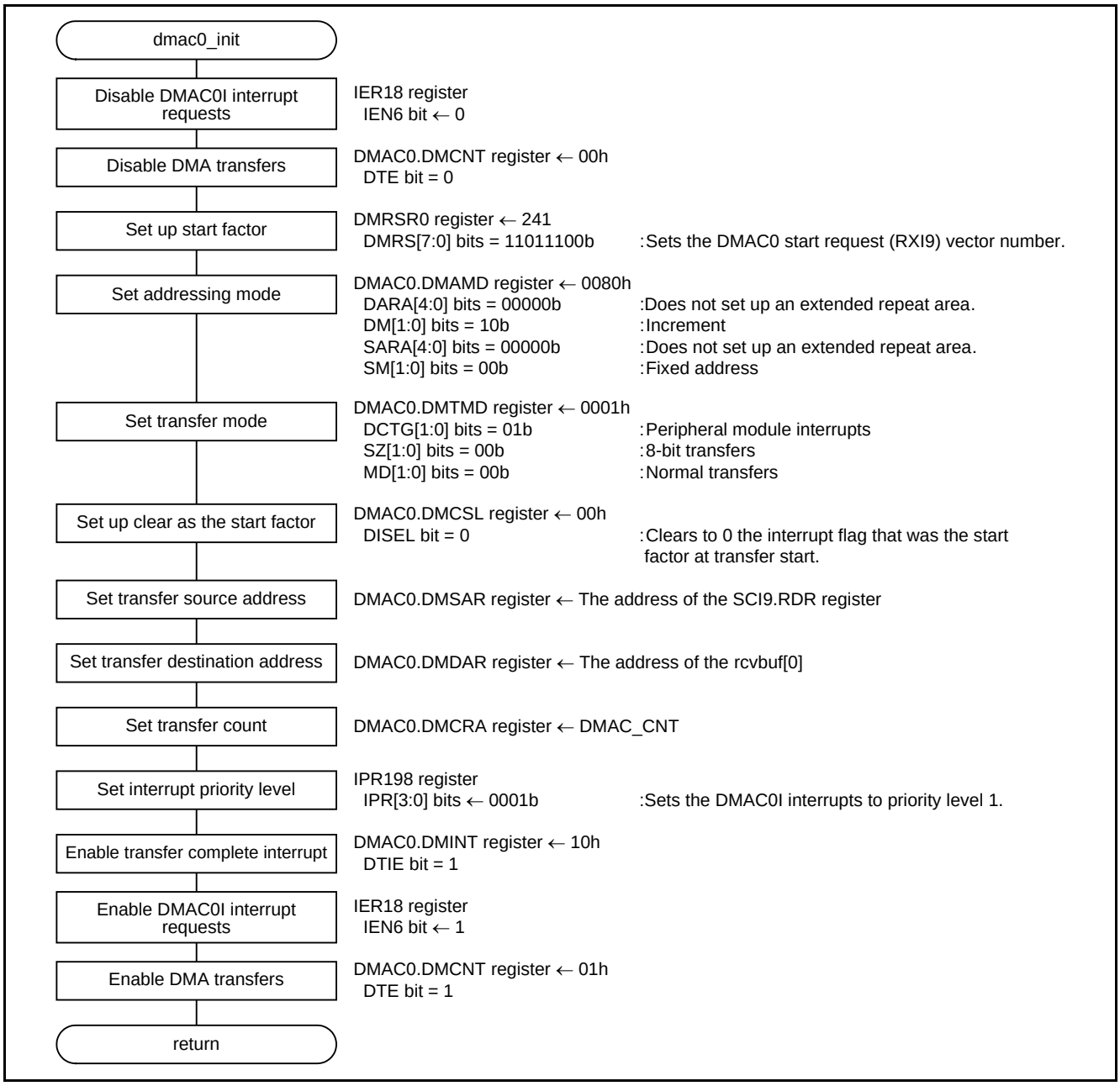


Figure 5.7 DMAC0 Initialization

5.8.6 DMAC1 Initialization

Figure 5.8 shows the flowchart for the DMAC1 initialization.

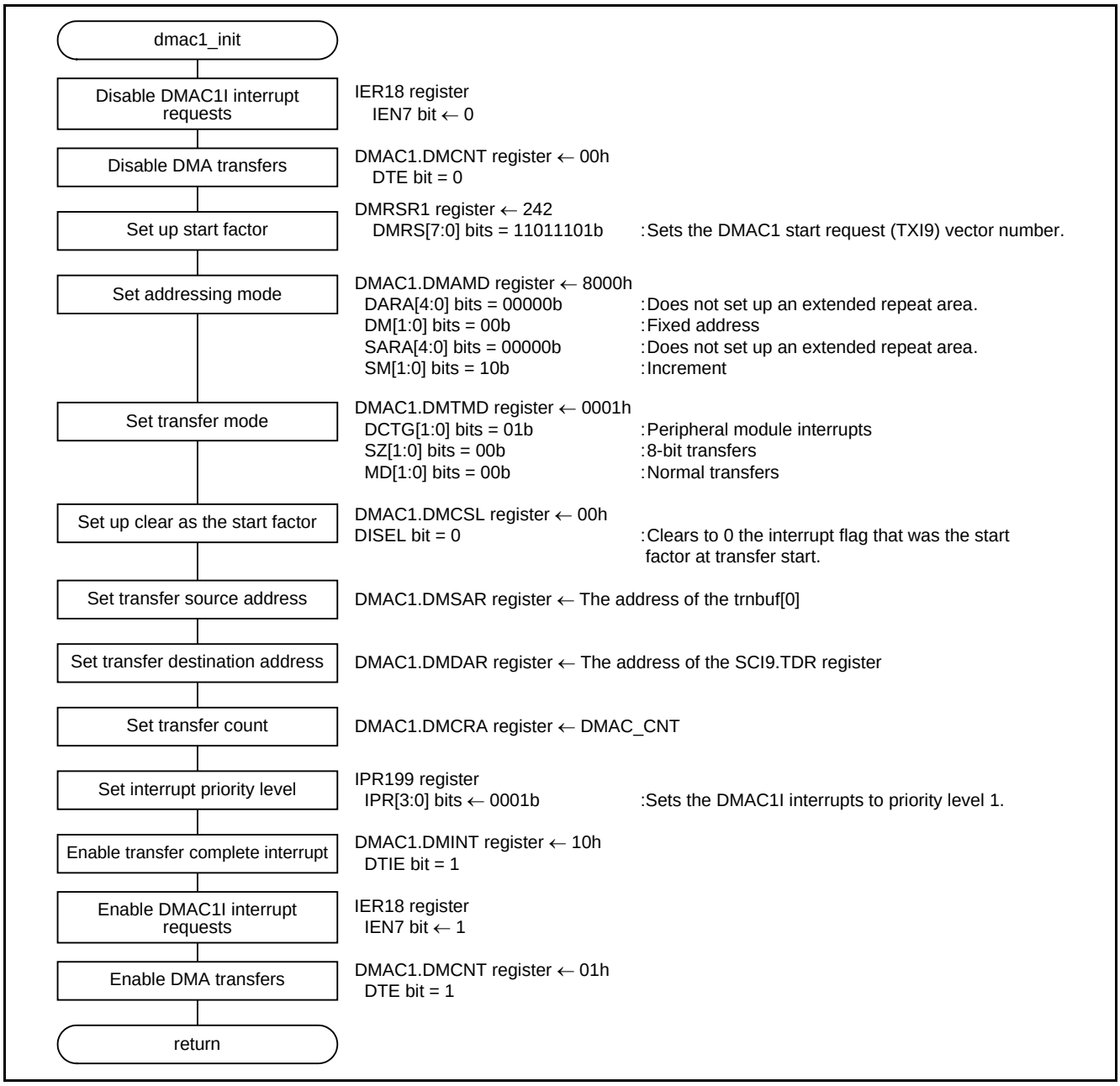


Figure 5.8 DMAC1 Initialization

5.8.7 SCI9 Transmission and Reception Start

Figure 5.9 shows the flowchart for the SCI9 transmission and reception start.

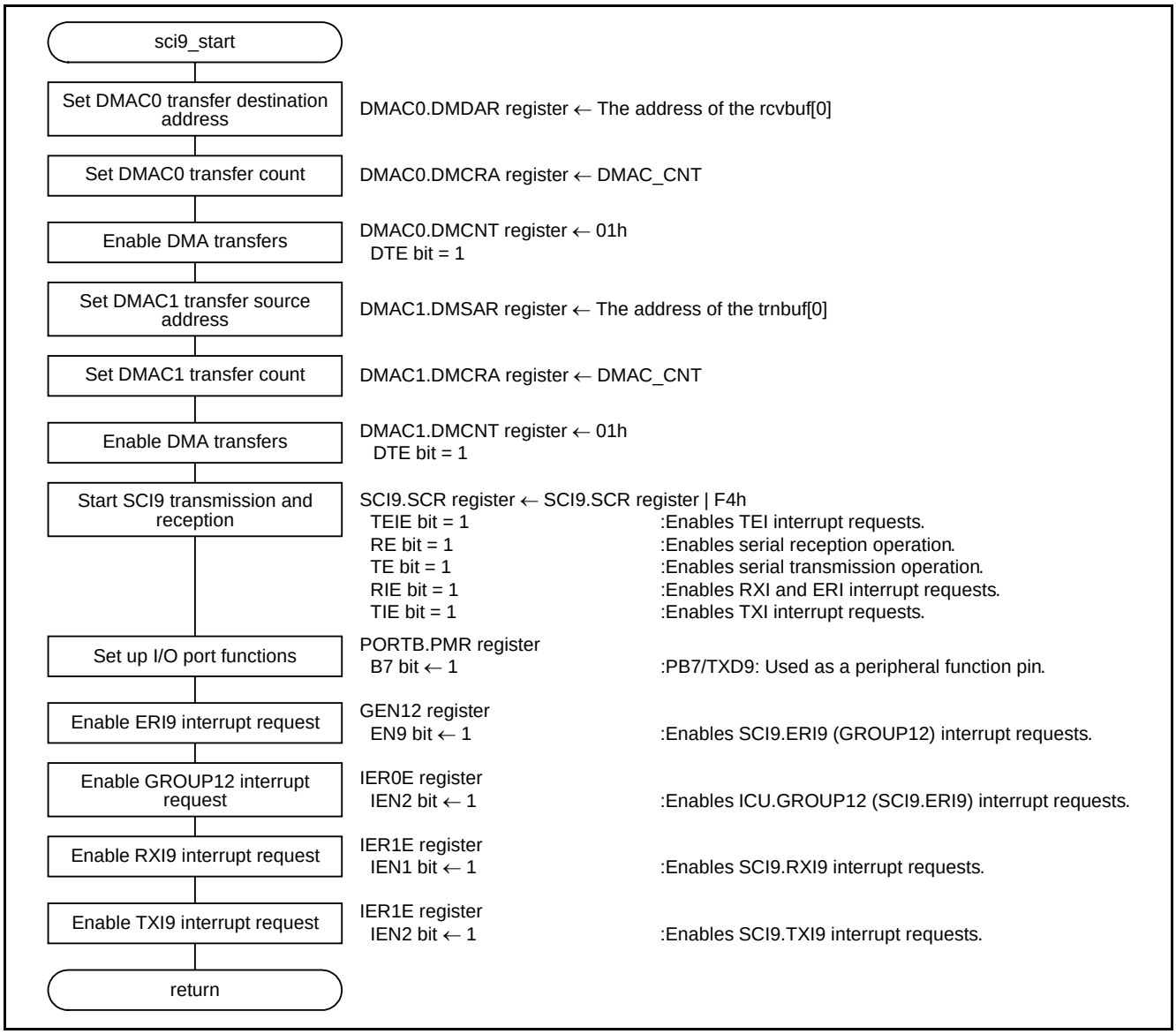


Figure 5.9 SCI9 Transmission and Reception Start

5.8.8 DMAC0 Transfer Complete Interrupt Handler

Figure 5.10 shows the flowchart for the DMAC0 transfer complete interrupt handler.

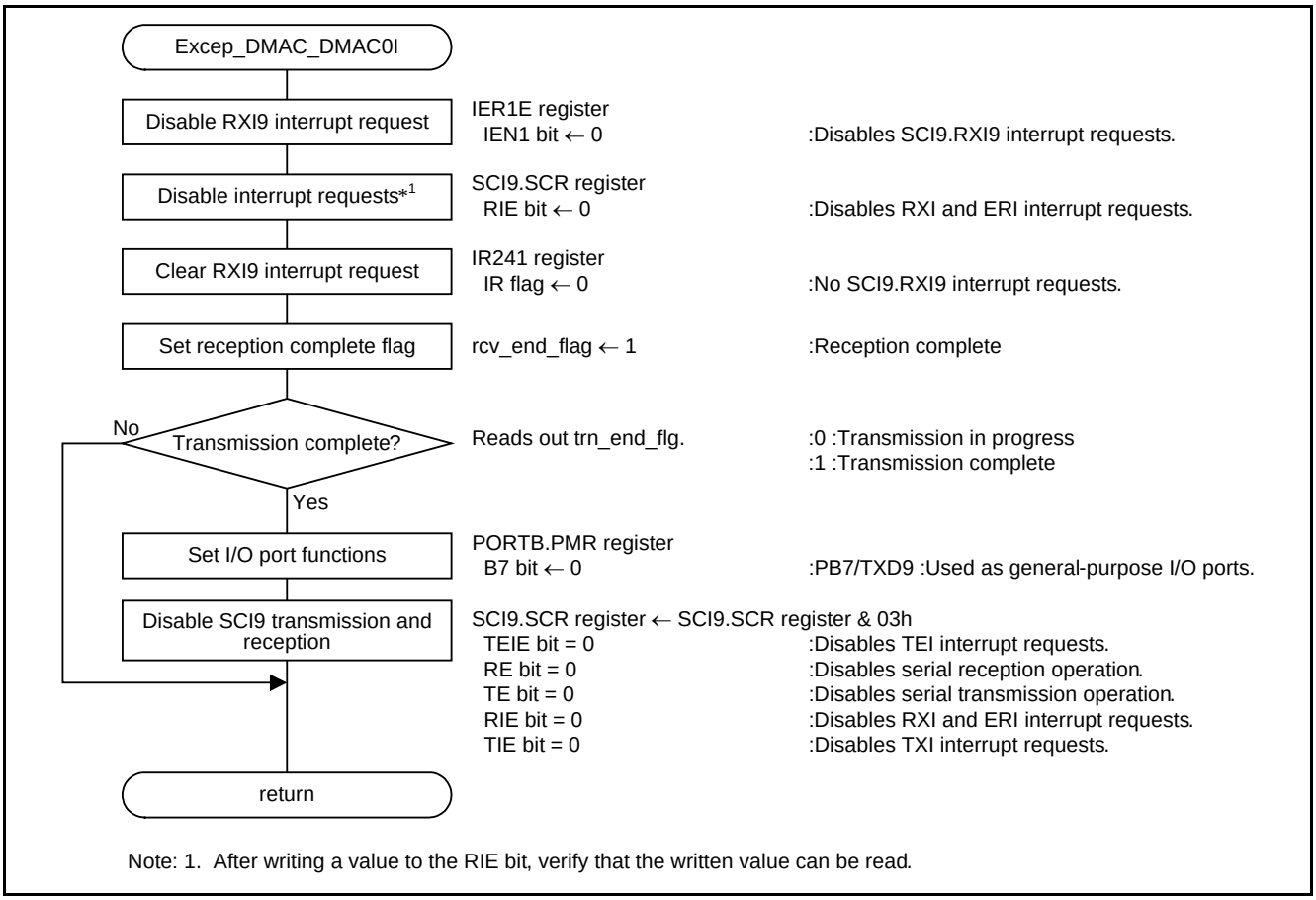


Figure 5.10 DMAC0 Transfer Complete Interrupt Handler

5.8.9 DMAC1 Transfer Complete Interrupt Handler

Figure 5.11 shows the flowchart for the DMAC1 transfer complete interrupt handler.

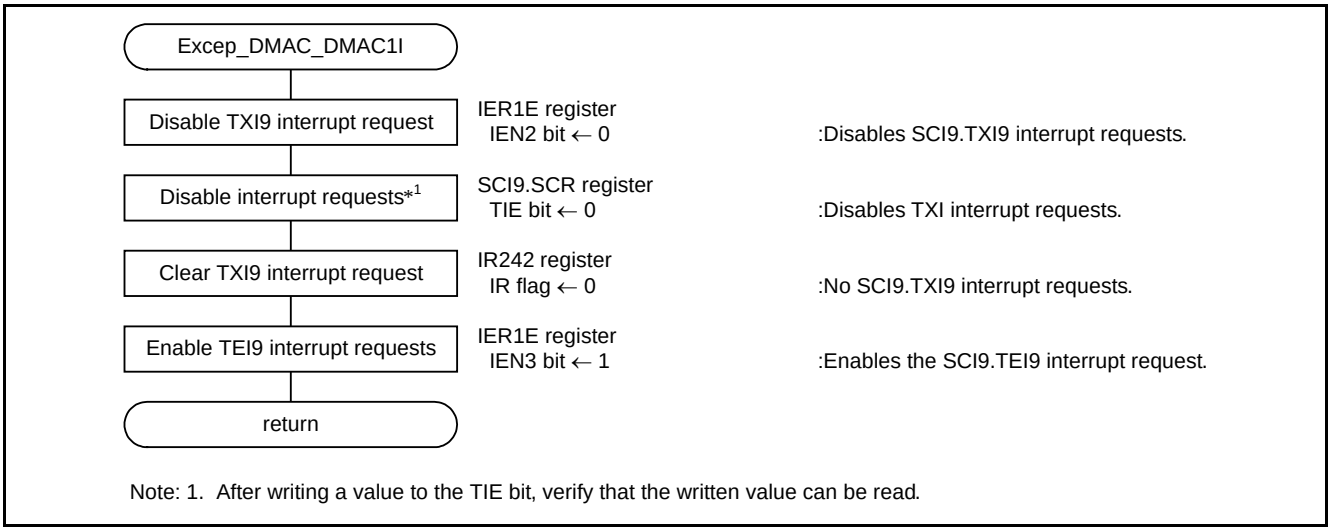
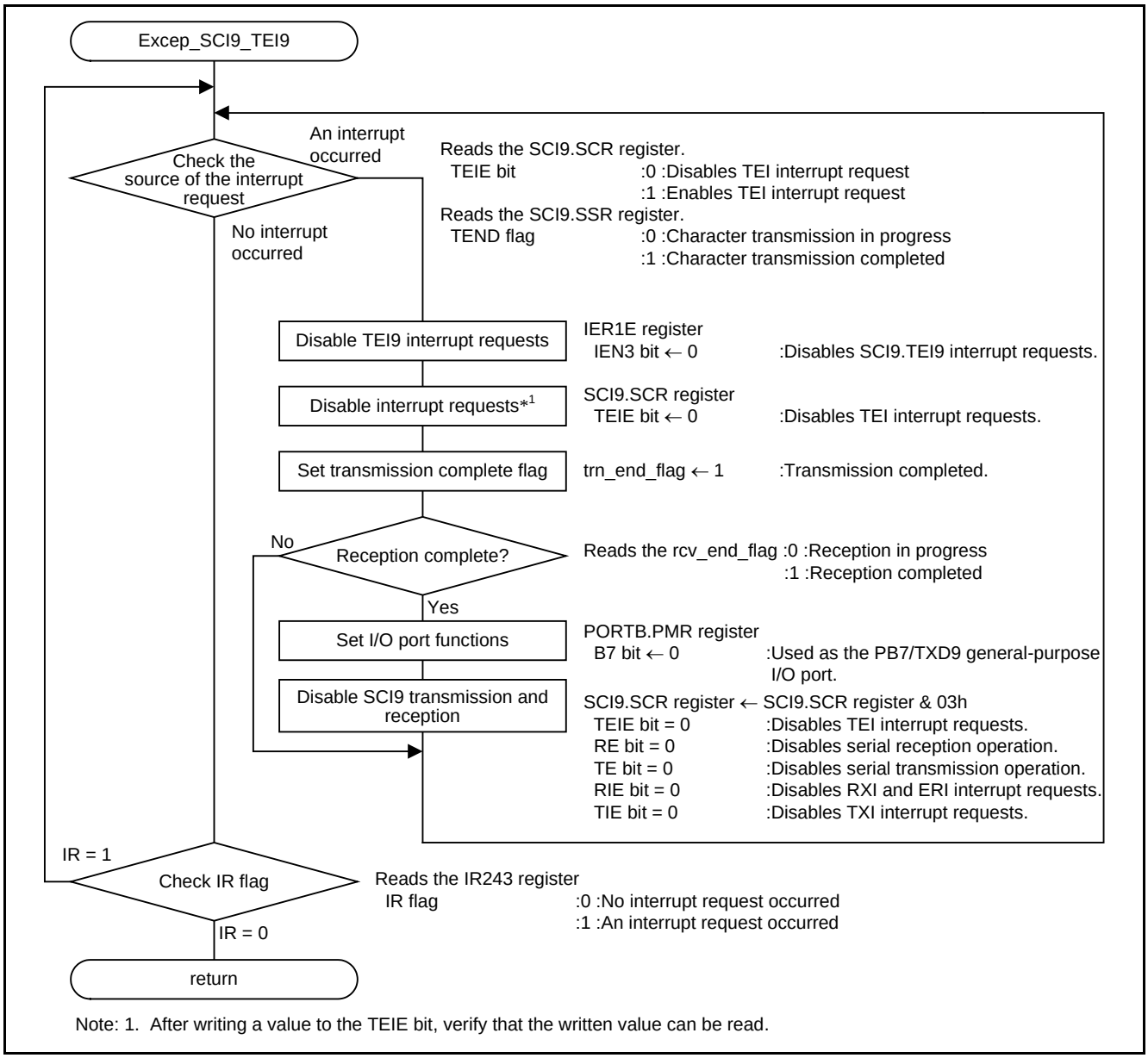


Figure 5.11 DMAC1 Transfer Complete Interrupt Handler

5.8.10 SCI9 Transmission Complete Interrupt Handler

Figure 5.12 shows the flowchart for the SCI9 transmission complete interrupt handler.



Note: 1. After writing a value to the TEIE bit, verify that the written value can be read.

Figure 5.12 SCI9 Transmission Complete Interrupt Handler

5.8.11 Group 12 Interrupt Handler (SCI9 Reception Error Interrupt)

Figure 5.13 shows the flowchart for the Group 12 interrupt handler (SCI9 reception error interrupt).

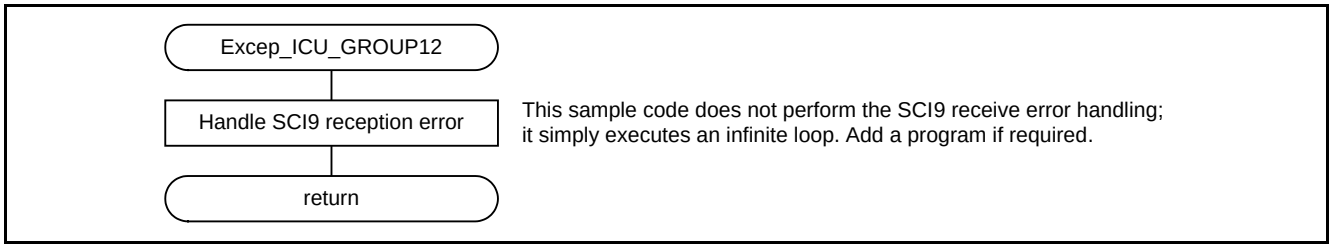


Figure 5.13 Group 12 Interrupt Handler (SCI9 Reception Error Interrupt)

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware Rev.1.50 (R01UH0041EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

http://www.renesas.com

Inquiries

http://www.renesas.com/contact/

REVISION HISTORY	RX63N Group, RX631 Group Application Note Clock Synchronous SCIc Communication Using the DMACA

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 05, 2013	—	First edition issued

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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