RX600, RX700 Series

Design Guide for Sub-Clock Circuits

R01AN1187EJ0110
Rev. 1.10
Mar. 7, 2016

Abstract

The sub-clock oscillation circuit is a circuit with a low gain used to reduce power consumption. Due to the low gain, there is a risk that noise may cause the MCU to operate erroneously. This document describes how to minimize this risk when using a low CL resonator; it does not guarantee system operation.

Products

RX600 Series (LQFP, TFLGA, LFBGA packages)

RX700 Series (LQFP, TFLGA, LFBGA packages)

As wiring differs between packages, confirm that the wiring for each package is accurate.

Contents

1. Points on Board Design

1.1 Points on XCIN and XCOUT Wiring

(1) to (6) below describe points on wiring for XCIN and XCOUT. Figures 1.1 through 1.3 show examples of traces for each package.

(1) Do not cross the XCIN and XCOUT wires with other signal wires.

(2) Do not add an observation pin to XCIN and XCOUT.

(3) Make the XCIN and XCOUT wire width between 0.1 and 0.3 mm. The wire length from the MCU pins to the crystal resonator pins should be less than 10 mm, or at least as close to 10 mm if longer.

(4) The wire connected to the XCIN pin and the wire connected to the XCOUT pin should have as much space between them (at least 0.3 mm) as possible.

(5) Connect external capacitors as close together as possible. Connect the wire for the capacitors to the ground trace (hereinafter referred to as ground shield) on the component side. For details on the ground shield, refer to section 1.2. When the capacitors cannot be laid out as shown in Figure 1.1 to 1.3, use the layout shown in Figure 1.4.

(6) In order to decrease the parasitic capacitance between XCIN and XCOUT, include a ground trace between the resonator and the MCU.

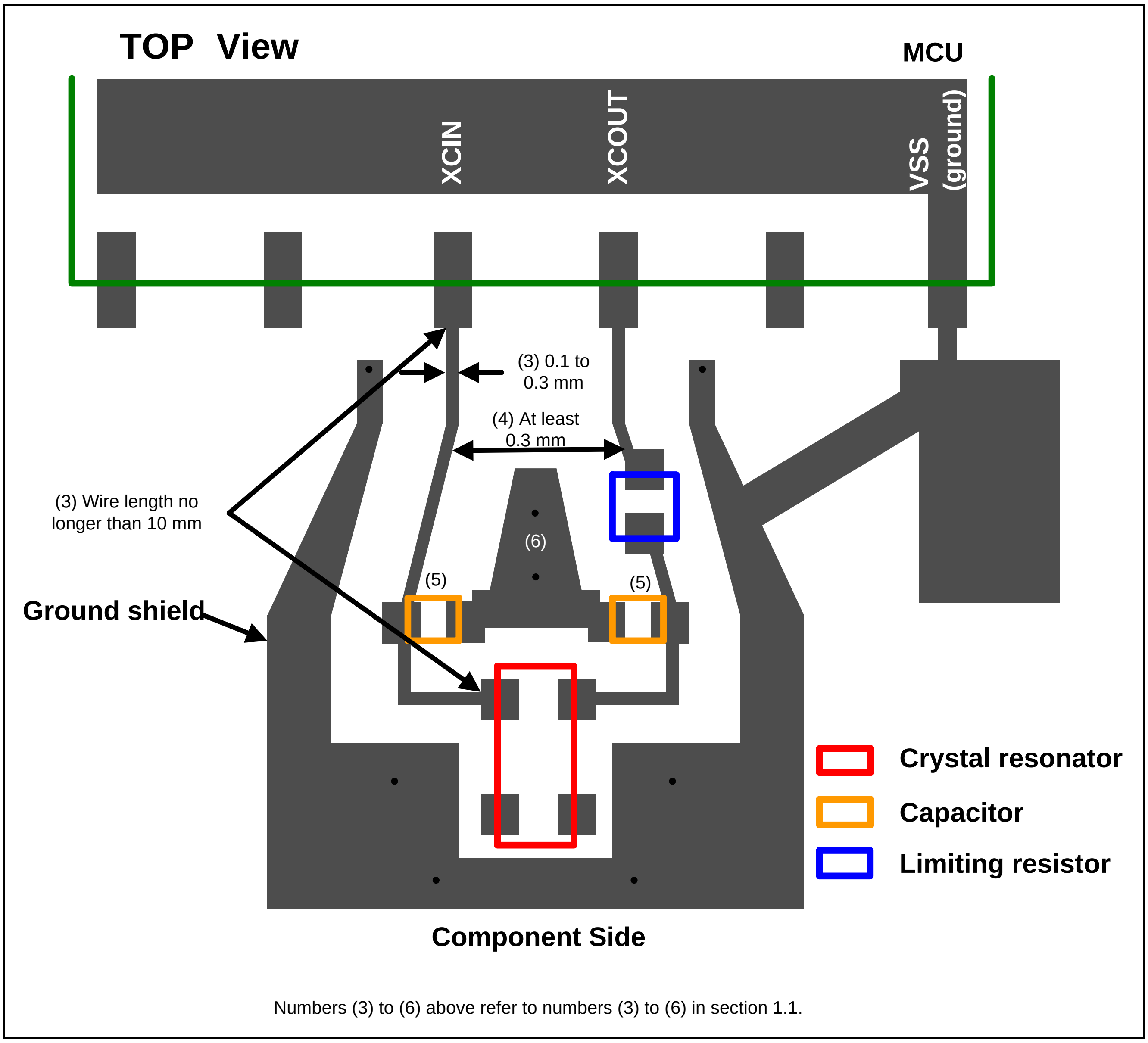

Figure 1.1 Example of Preferred Trace for XCIN and XCOUT Wiring in the 100-pin, 144-pin, and 176-pin LQFP Packages

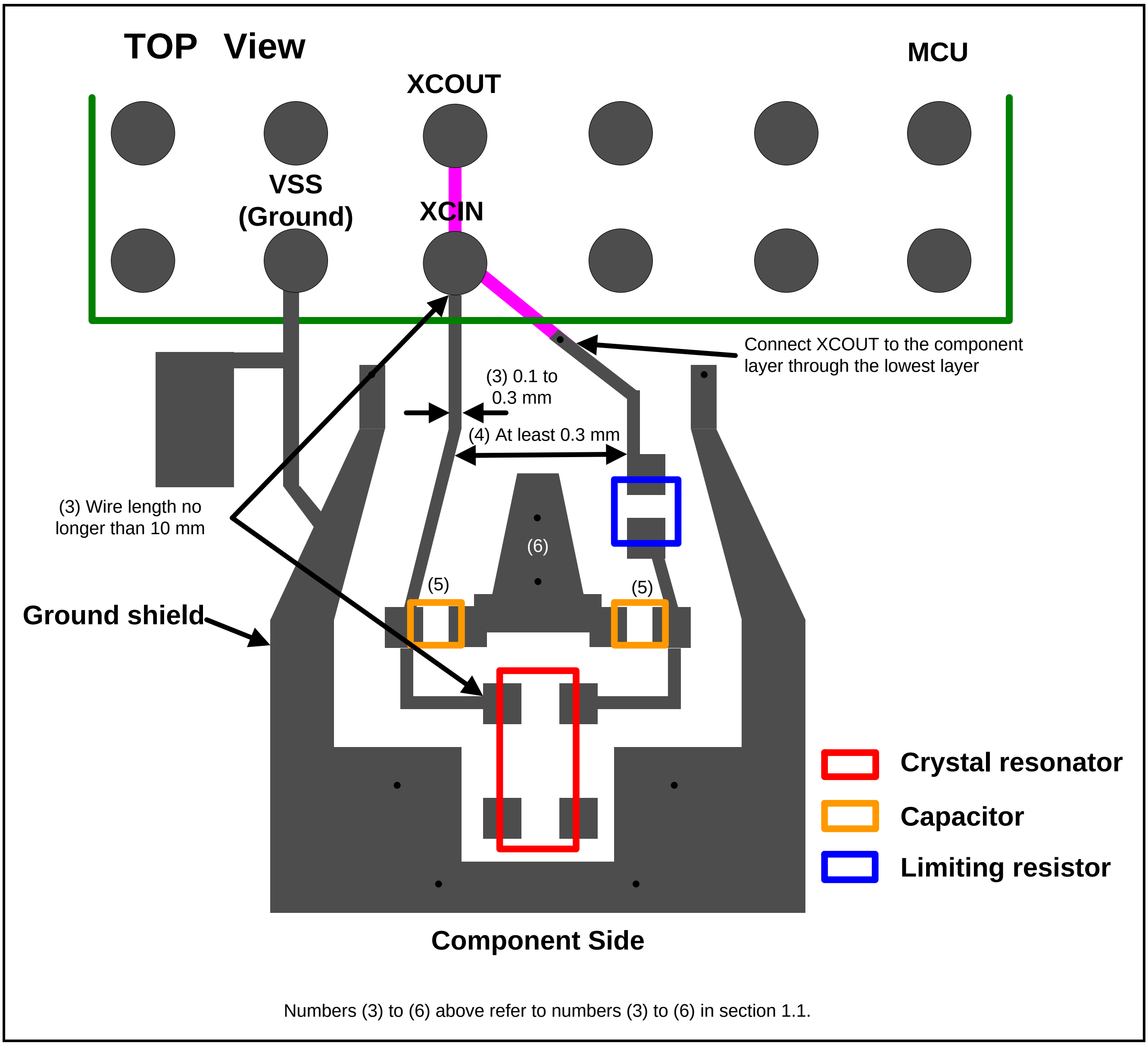

Figure 1.2 Example of Preferred Trace for XCIN and XCOUT Wiring in the 145-pin TFLGA Package

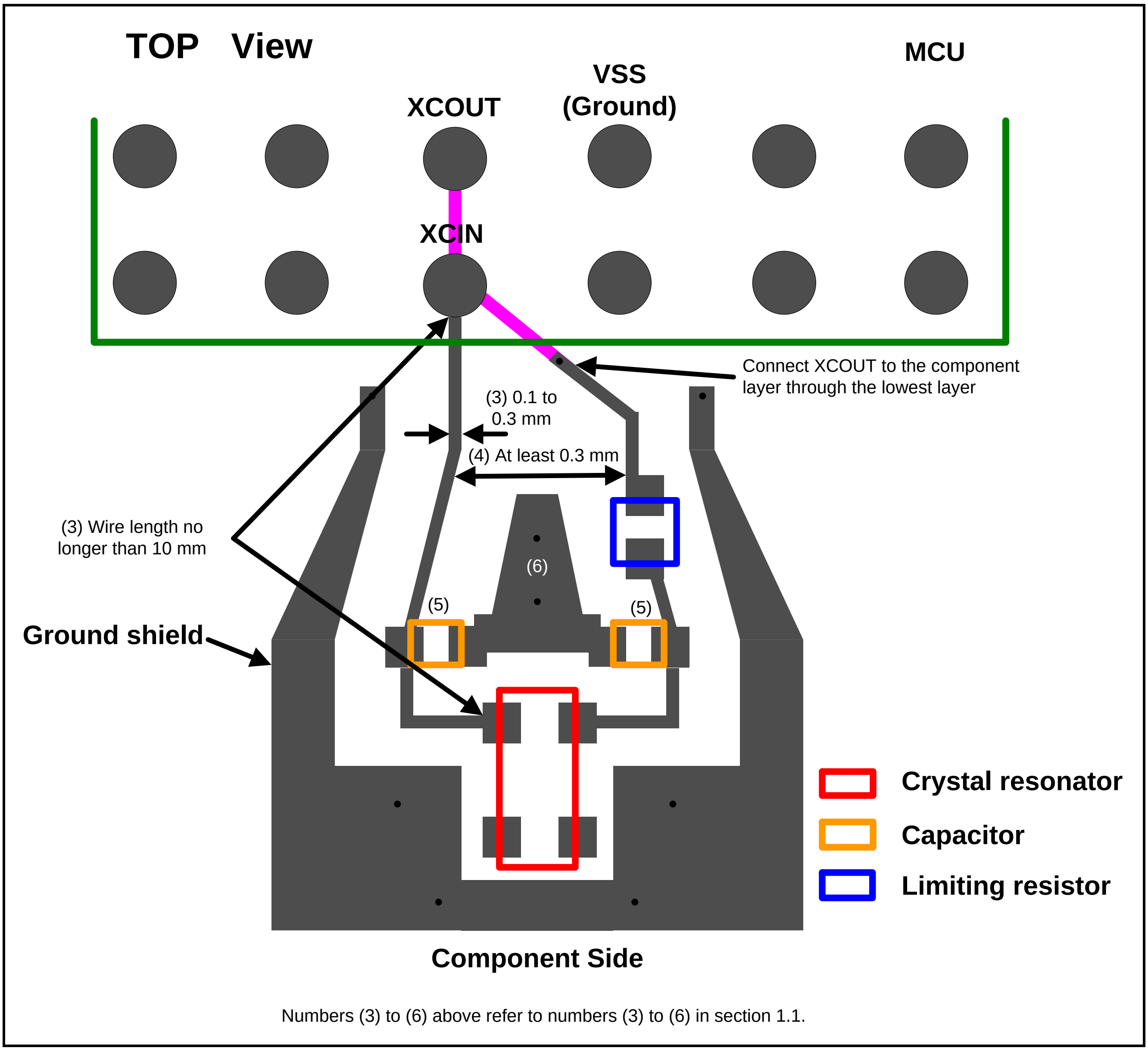

Figure 1.3 Example of Preferred Trace for XCIN and XCOUT Wiring in the 176-pin LFBGA and 177-pin TFLGA Packages

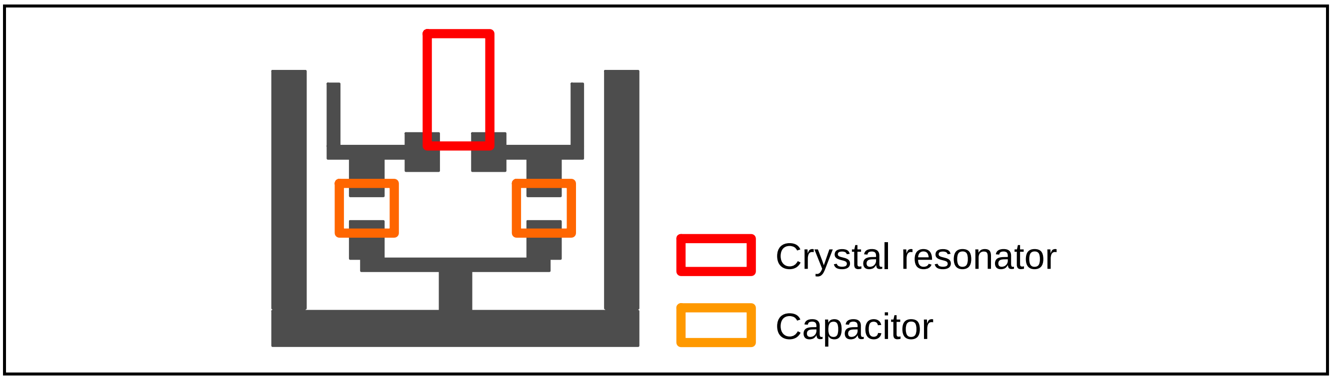

Figure 1.4 Example of Alternate Trace for XCIN and XCOUT Wiring

1.2 Points Regarding the Ground Shield

Shield the crystal resonator with a ground trace. (1) to (4) below describe the points regarding the ground shield. Figures 1.5 to 1.7 show trace examples for each package.

(1) Lay out the ground shield on the same layer as the crystal resonator wiring.

(2) Make the ground shield wire width at least 0.3 mm, and leave a 0.3 to 2.0 mm gap in between wires.

(3) Wire the ground shield as close to the VSS pin on the MCU as possible, and ensure that the wire width is at least 0.3 mm.

(4) In the 100-pin LQFP, 144-pin LQFP, 176-pin LQFP, and 145-pin TFLGA packages, to prevent current from running to the ground shield, branch the ground shield and the ground on the board near the VSS pin on the board. The VSS pin and ground shield in the 176-LFBGA and 177-pin TFLGA packages are different and do not apply here.

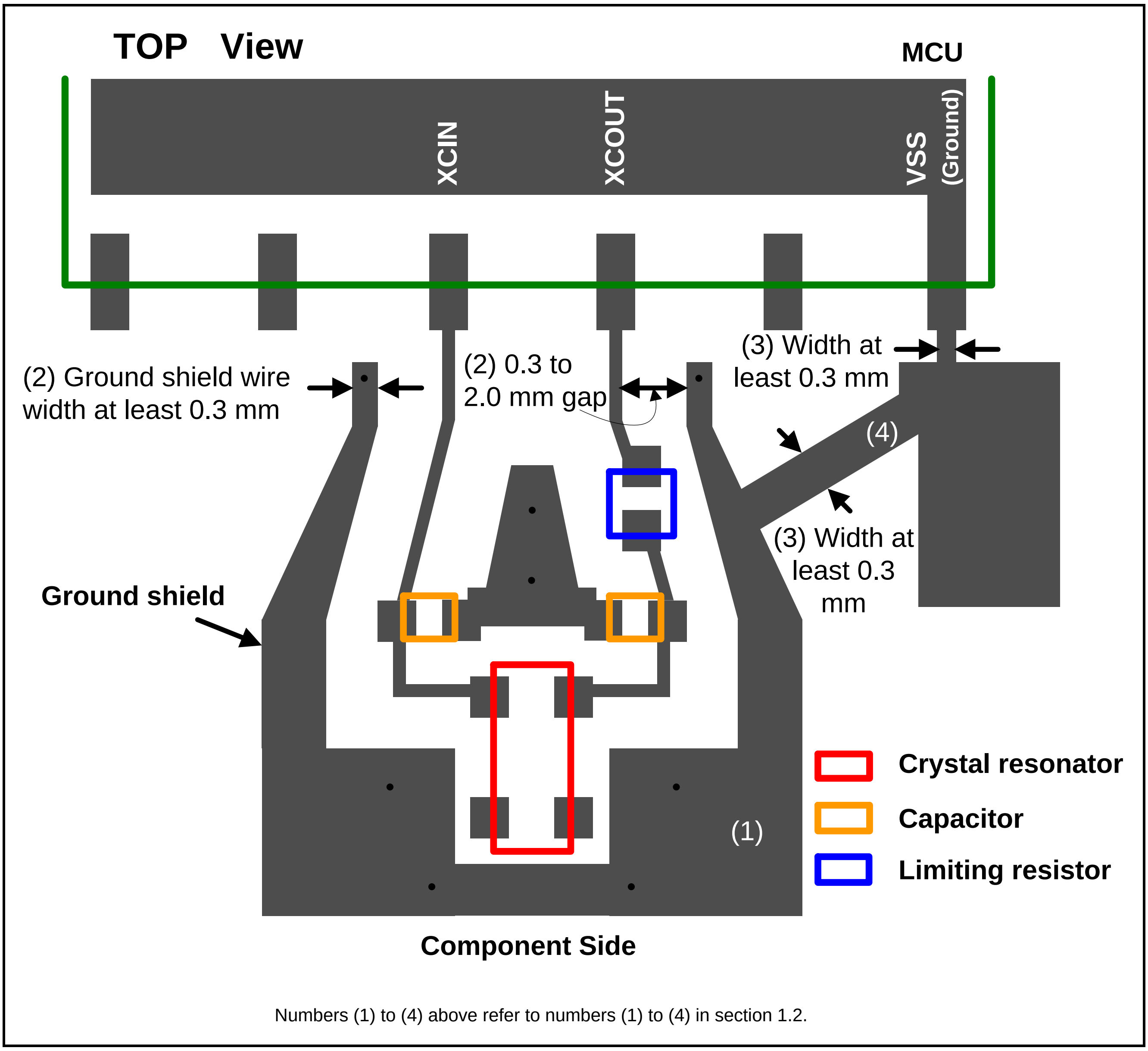

Figure 1.5 Trace Example for the Ground Shield in the 100-pin, 144-pin, and 176-pin LQFP Packages

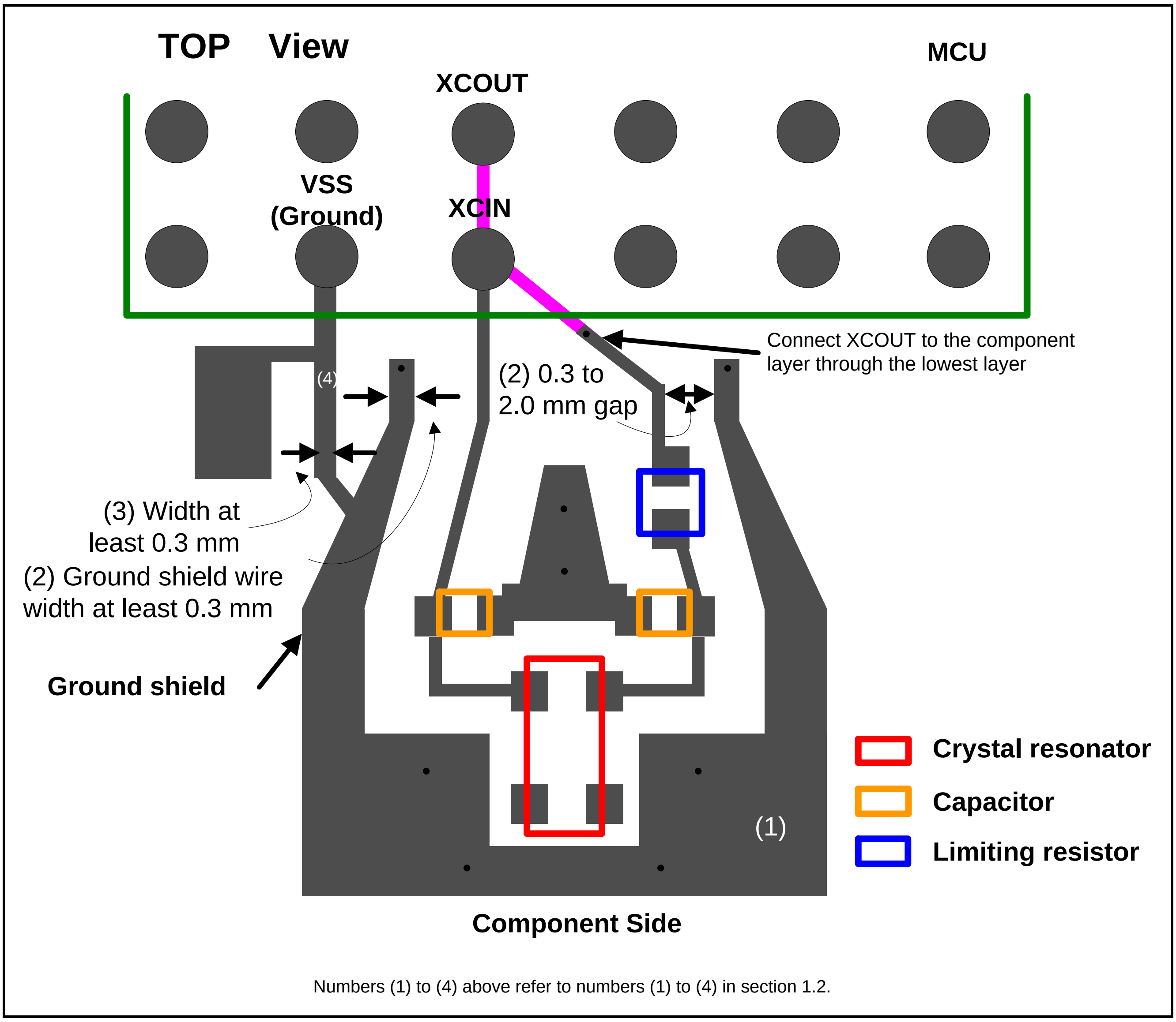

Figure 1.6 Trace Example for the Ground Shield in the 145-pin TFLGA Package

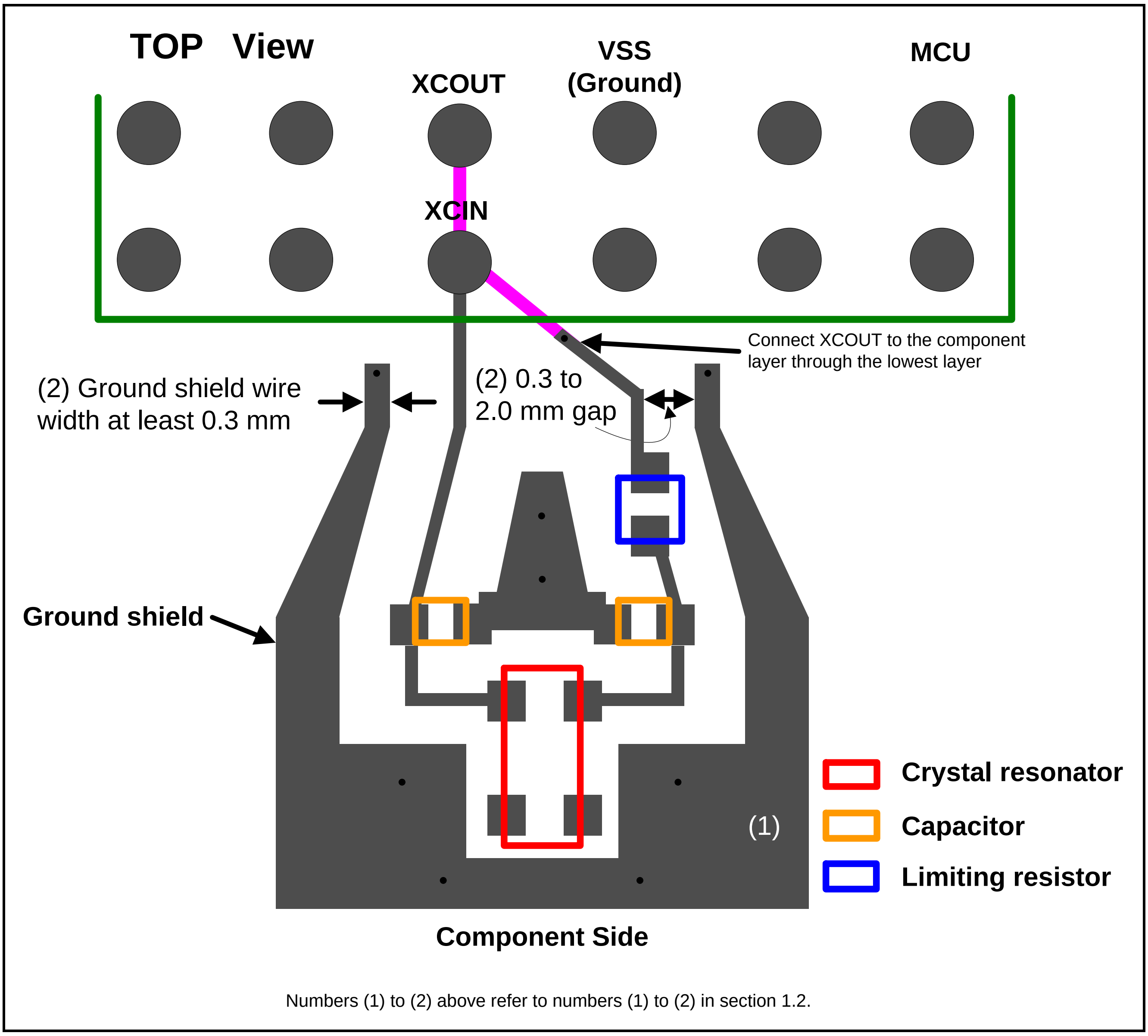

Figure 1.7 Trace Example for the Ground Shield in the 176-pin LFBGA and 177-pin TFLGA Packages

1.3 Points Regarding the Bottom Ground

1.3.1 Points When a Multilayered Board is at Least 1.2 mm

For boards that are at least 1.2 mm thick, lay out a ground trace on the solder side (hereinafter referred to as bottom ground) of the crystal resonator area (see Figure 1.8).

(1) through (3) describe points when making a multilayered board that is at least 1.2 mm thick. Figures 1.8 to 1.10 show trace examples of each package.

(1) Do not lay out any traces in the middle layers of the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either.

(2) Connect the ground shield terminator to the bottom ground.

(3) Make the bottom ground at least 0.1 mm bigger than the ground shield.

- For the 100-pin LQFP, 144-pin LQFP, 176-pin LQFP, and 145-pin TFLGA pin packages

  Only connect the ground shield to the bottom ground of the component side of the board. Connect the bottom ground to the VSS pin through the ground shield. Do not connect the bottom ground or the ground shield to a ground other than the VSS pin.

- For the 176-pin LFBGA and 177-pin TFLGA Packages

  Connect the bottom ground directly to the VSS pin. Do not connect the bottom ground or the ground shield to a ground other than the VSS pin.

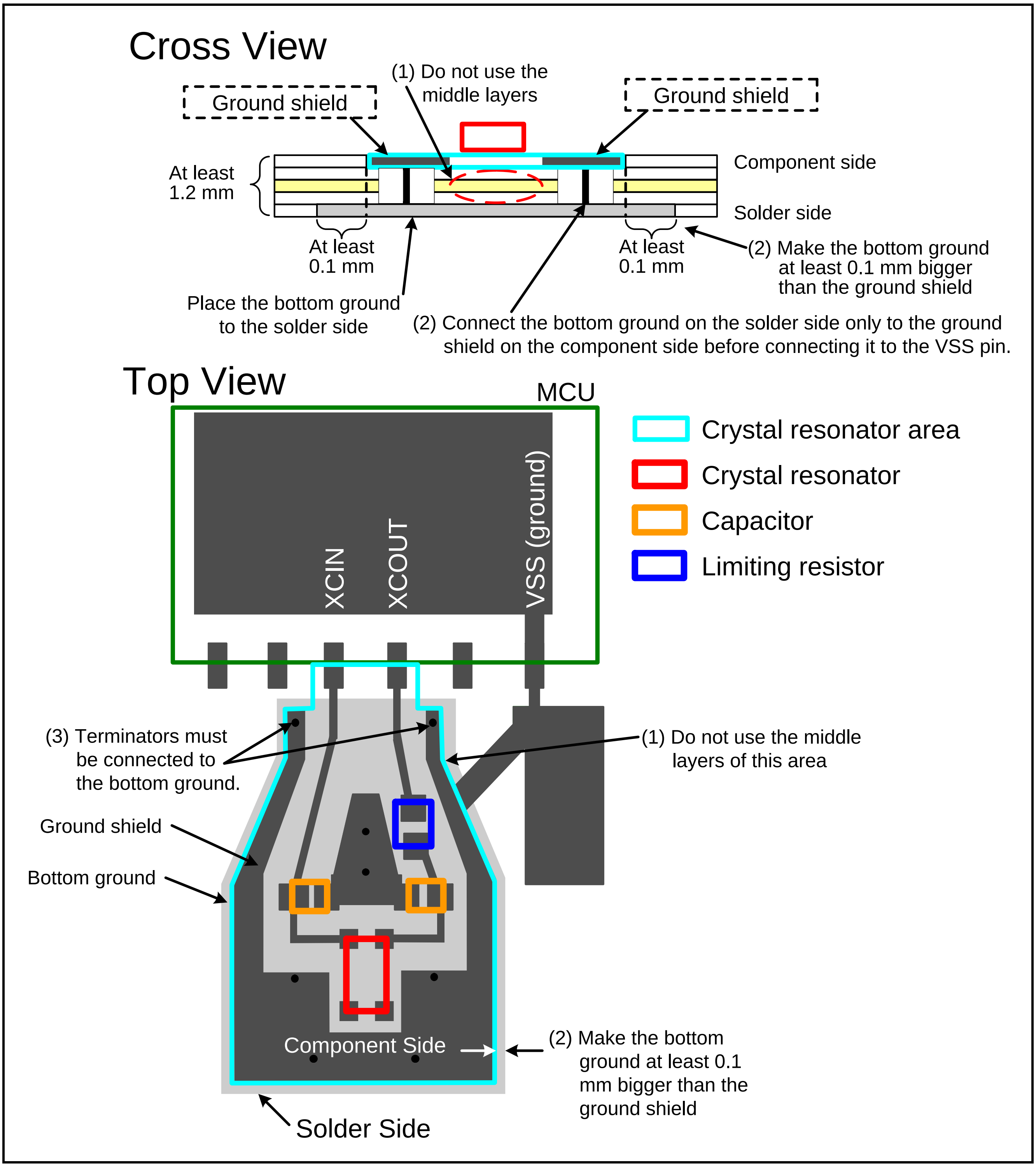

Figure 1.8 Trace Example When a Multilayered Board is at Least 1.2 mm Thick in the 100-pin, 144-pin, and 176-pin LQFP Packages

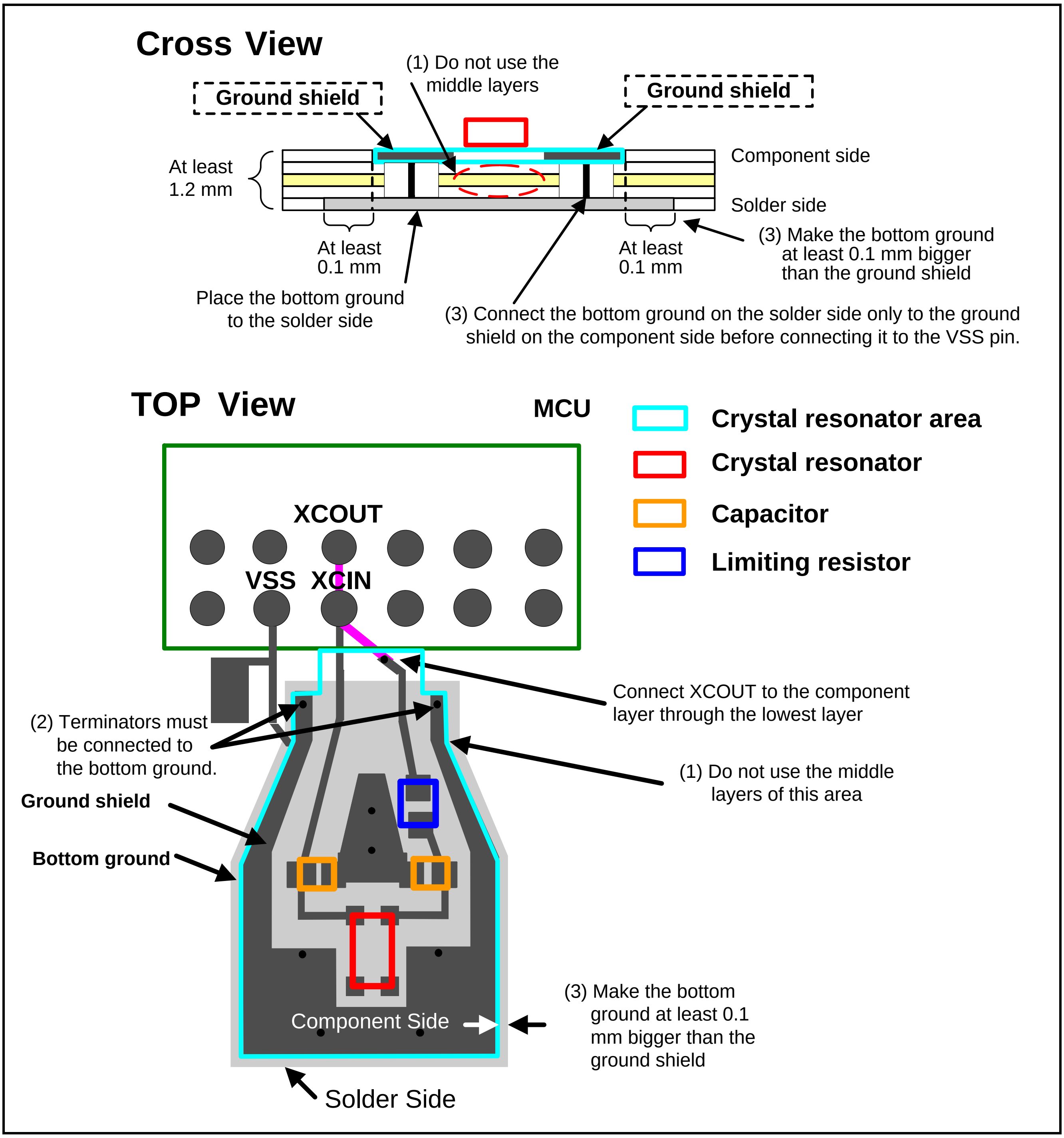

Figure 1.9 Trace Example When a Multilayered Board is at Least 1.2 mm Thick in the 145-pin TFLGA Package

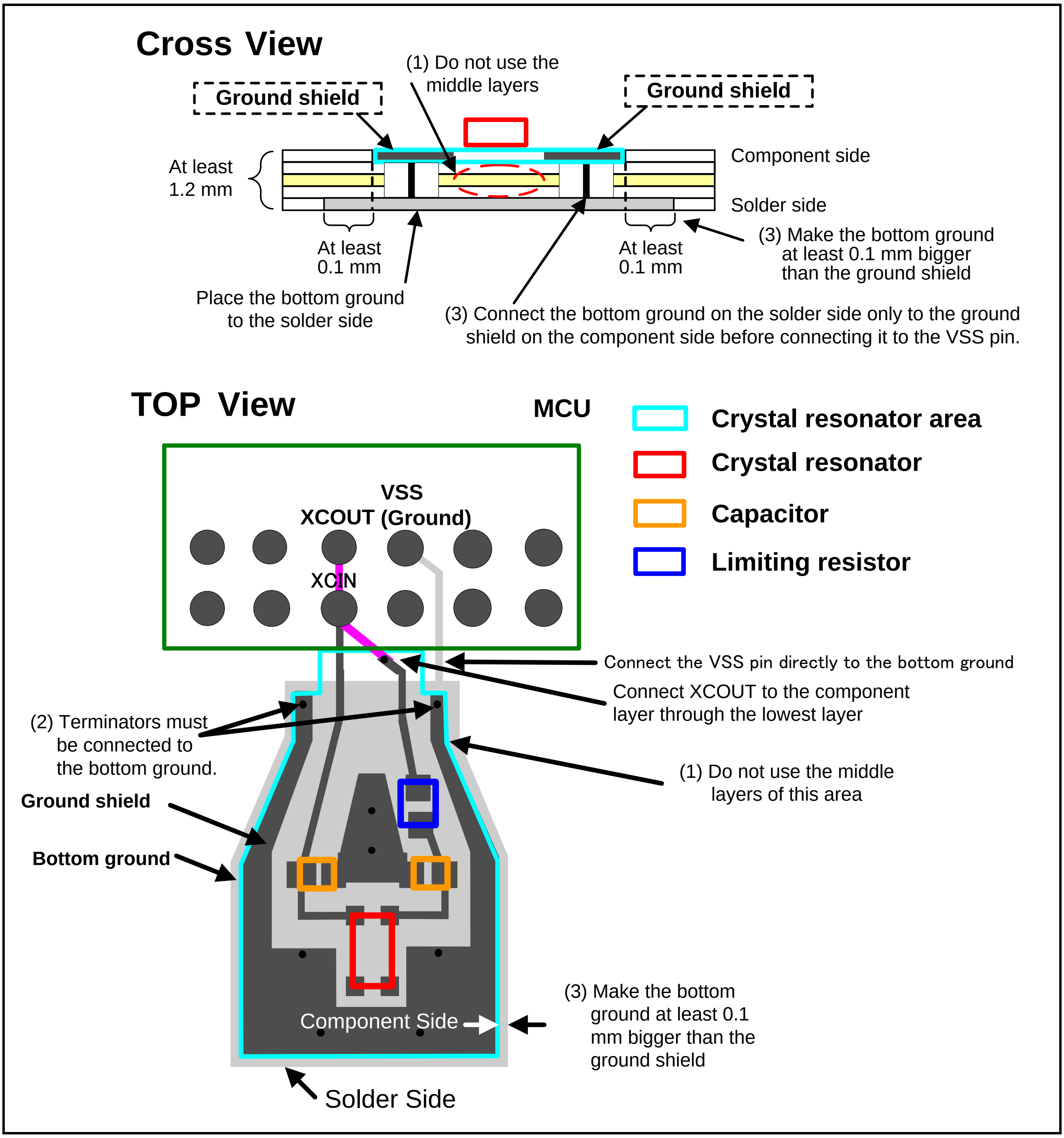

Figure 1.10 Trace Example When a Multilayered Board is at Least 1.2 mm Thick in the 176-pin LFBGA and 177-pin TFLGA Packages

1.3.2 Points When a Multilayered Board is Less Than 1.2 mm Thick

(1) describes points when making a multilayered board that is less than 1.2 mm thick, and Figure 1.11 shows a trace example.

(1) Do not lay out any traces to layers other than the component side for the crystal resonator area. Do not lay out power supply and ground traces in this area. Do not pass signal wires through this area either.

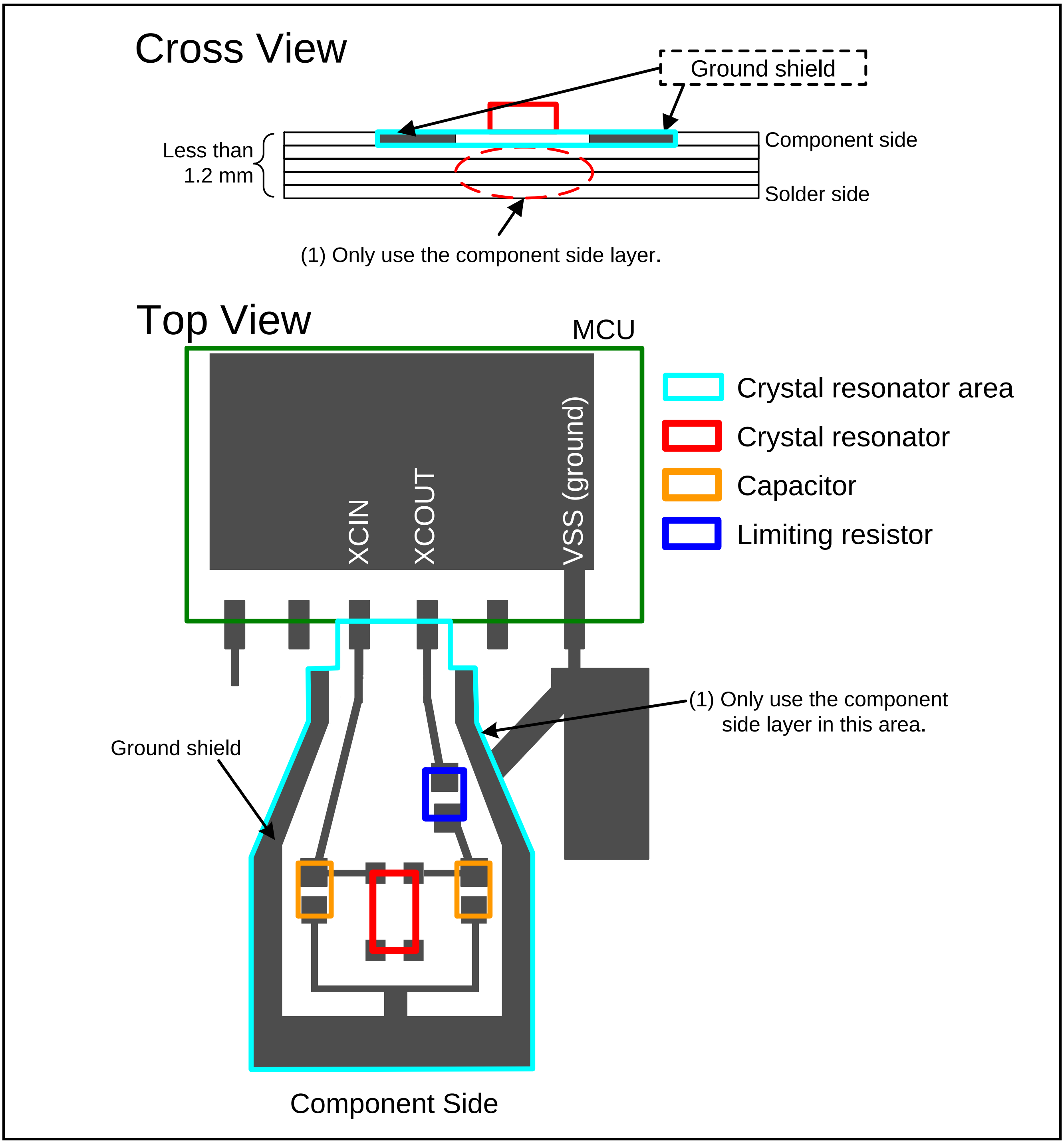

Figure 1.11 Trace Example When a Multilayered Board is Less Than 1.2 mm Thick in the 100-pin, 144-pin, and 176-pin LQFP Packages

1.4 Other Points

(1) to (4) below describe other points common between packages. Figure 1.12 shows a trace example for the 100-pin, 144-pin, and 176-pin LQFP packages.

(1) Do not place the XCIN and XCOUT wires near wires that have big changes in current.

(2) Do not run the XCIN and XCOUT wires parallel to other signal wires like those for adjacent pins.

(3) Pin wiring that runs adjacent to the XCIN and XCOUT pins should not just be laid out outside the MCU. Lay out the wiring through the bottom side of the MCU first and then lay out the wiring to an area away from the XCIN and XCOUT pins (to avoid the wiring from laying out the wiring parallel with the XCIN and XCOUT wiring).

(4) Lay out as much of the ground trace on the bottom side of the MCU as possible.

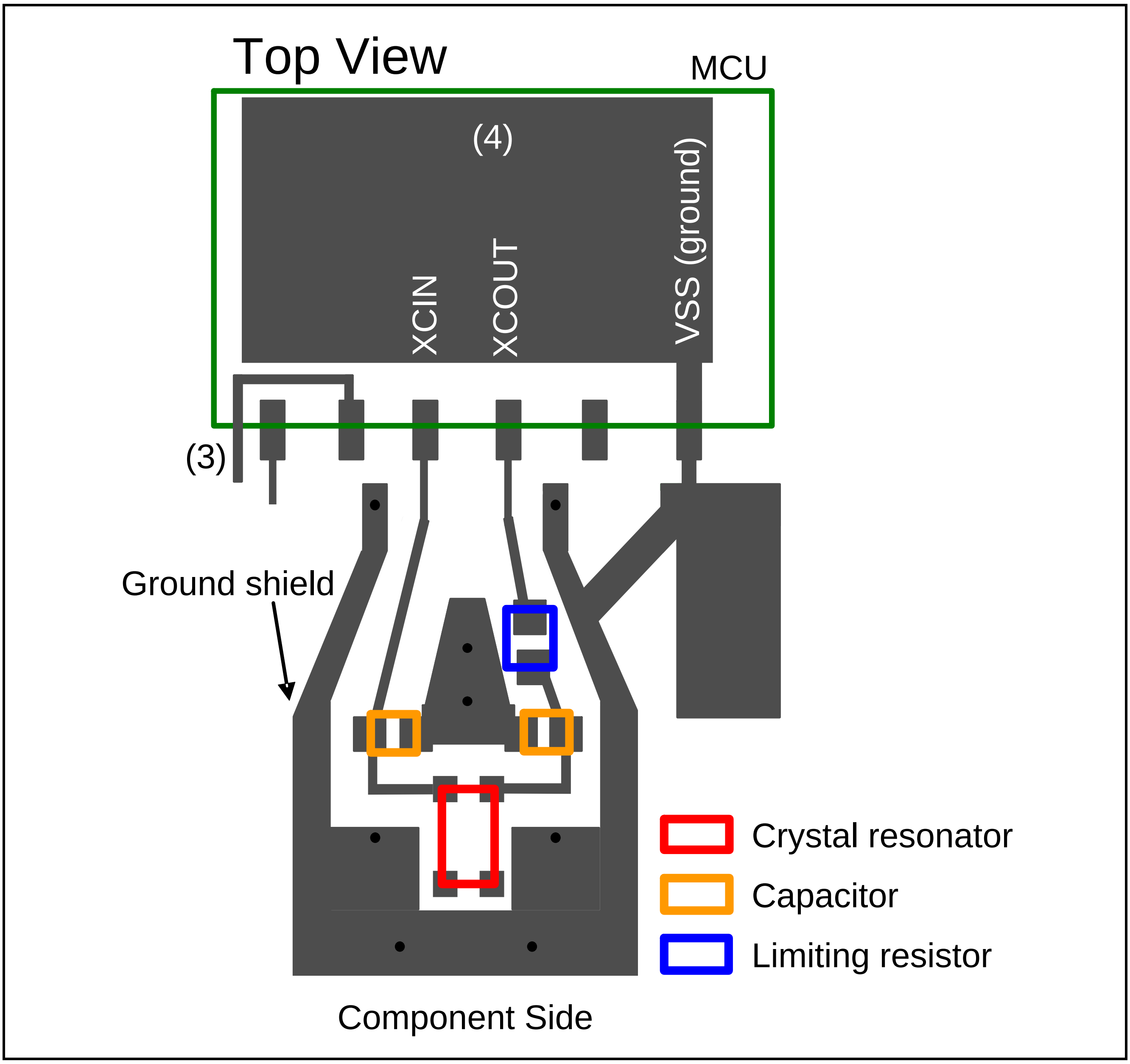

Figure 1.12 Trace Example for Other Points in the 100-pin, 144-pin, and 176-pin LQFP Packages

1.5 Points on Wiring the Main Clock Resonator

(1) describes points on wiring the main clock resonator, and Figure 1.13 shows a trace example.

(1) Shield the main clock resonator wiring with a ground. Do not connect the ground shield for the main clock and sub-clock together. Note that if the main clock ground shield is connected directly to the sub-clock ground shield, there is a possibility that noise from the main clock resonator may transfer through and affect the sub-clock.

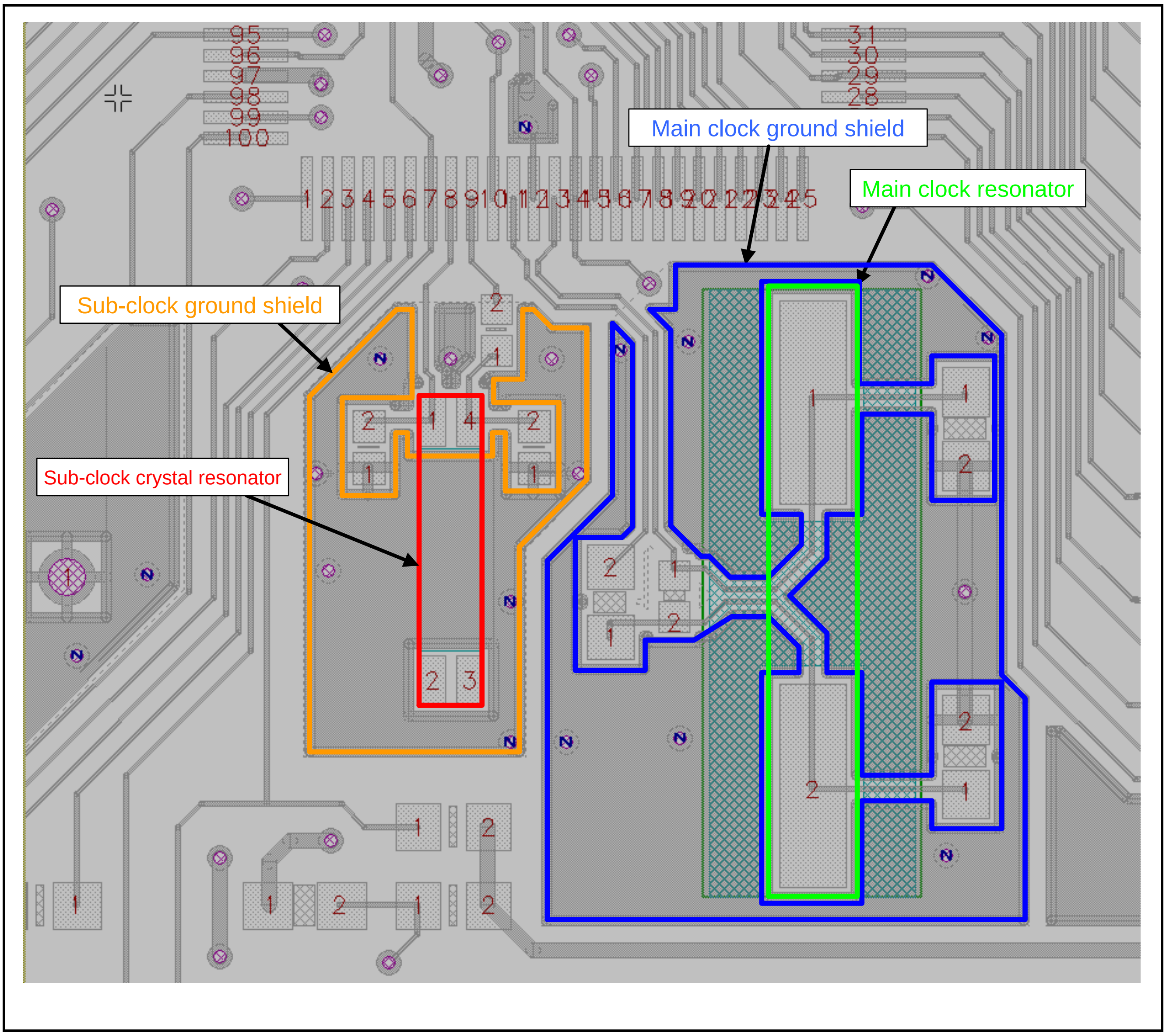

Figure 1.13 Trace Example When Shielding the Main Clock Resonator With a Ground

2. Trace Example Showing a High Risk of Erroneous Operation Due to Noise

Do not lay out traces described in (1) through (9) (these points apply to all packages). Laying out the traces below may cause the low CL resonator to not oscillate correctly. Figure 1.8 shows a trace example.

(1) XCIN and XCOUT wires cross other signal wires (risk of erroneous operation).

(2) Observation pins are attached to XCIN and XCOUT (risk of oscillation stopping).

(3) XCIN and XCOUT wires are long (risk of erroneous operation or decreased accuracy).

(4) The ground shield does not cover the entire area, and where there is a ground shield, the wiring is long and narrow (easily affected by noise, and there is a risk that accuracy will decrease from the ground potential difference generated by the MCU and external capacitor).

(5) Ground shield is not detached near VSS pin (risk of erroneous operation from MCU current flowing to the ground shield).

(6) Power supply or ground trace are under the XCIN and XCOUT wiring (risk of losing the clock or oscillation stopping).

(7) A wire with a large-current is routed nearby (risk of erroneous operation).

(8) Parallel wiring for adjacent pins is close and long (risk of losing the clock or oscillation stopping).

(9) The middle layers are used (risk of oscillation characteristics decreasing or signals operating erroneously).

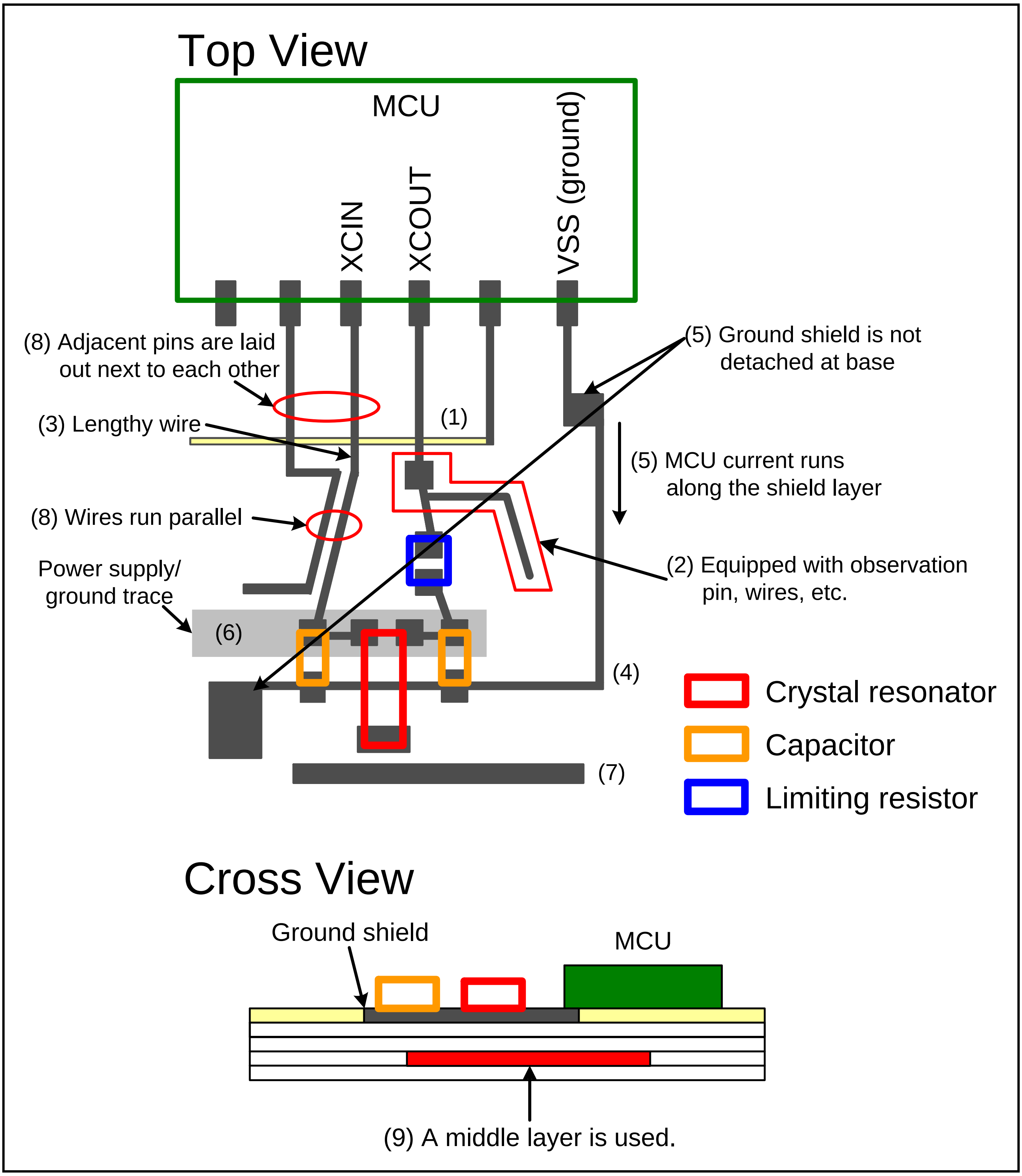

Figure 2.1 Trace Example Showing a High Risk of Erroneous Operation Due to Noise

3. Reference Oscillation Circuit Constants and Verified Resonator Operation

Table 1.1 lists the reference oscillation circuit constants for the verified resonator operation, and Figure 3.1 shows a trace example of the verified resonator operation.

Table 3.1 Reference Oscillation Circuit Constants for the Verified Resonator Operation

Manufacturer	Product	SMD/ With Leads	Frequency	Sub-Clock Oscillation Mode	Load Capacity Cl	Load Capacity Cg (1)	Load Capacity Cd (2)	Oscillation Stabilization Time	Negative Resistance
Seiko Instruments Inc.	SSP-T7-FL (1)	SMD	32.768 kHz	Low CL drive capacity	4.4 pF	5 pF	3 pF	1 second	-406 kΩ
Seiko Epson Inc.	MC-146 (2)	SMD	32.768 kHz	Standard CL drive capacity	7 pF	9 pF	9 pF	1.15 seconds	-1000 kΩ
Seiko Epson Inc.	MC-146L (2)	SMD	32.768 kHz	Low CL drive capacity	3.7 pF	3 pF	3 pF	1 second	-510 kΩ

Note:

1. When using this resonator, contact Seiko Instruments Inc. for details on matching (http://www.sii-crystal.com).
2. When using this resonator, contact Seiko Epson Inc. for details on matching (http://www5.epsondevice.com/en/).

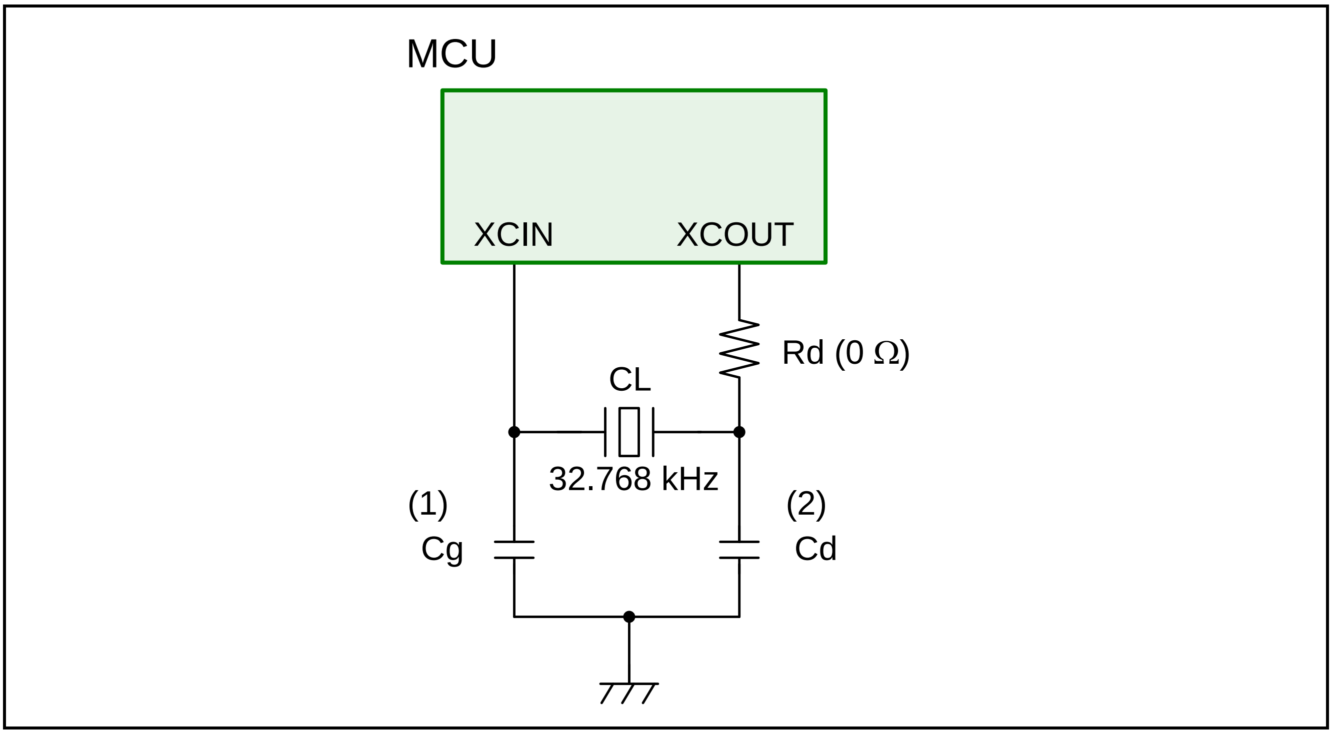

Figure 3.1 Trace Example for Verified Resonator Operation

The verified resonator operation and reference oscillation circuit constants listed here are based on information from the resonator manufacturer and not guaranteed. As reference oscillation circuit constants are measurements surveyed under fixed conditions by the manufacturer, values measured in the user system may vary. To achieve the optimum reference oscillation circuit constants for use in the actual user system, inquire with the resonator manufacturer to perform an evaluation on the actual circuit.

The conditions in the figure are conditions for oscillating the resonator connected to the MCU and are not operating conditions for the MCU itself. Refer to the specifications in the electrical characteristics for details on the MCU operating conditions.

4. Reference Documents

User's Manual: Hardware
The latest revision can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	July 1, 2012	-	First edition issued
1.10	Mar. 7, 2016	1	Changed the target device to RX600, RX700 Series.
		13	Added a reference oscillation circuit constants in Table 3.1 (Manufactured by Seiko Epson Inc.)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 5.0