# RX210 Group

## Differences Between Chip Versions B and C

## Abstract

This document confirms the differences between chip versions B and C in the RX210 Group.

## Products

RX210 Group

## Contents

## 1.    RX210 Chip Version B and C Products

Chip version C has products only with less than or equal to 100 pins, and 512 KB or 384 KB ROM. Chip version B covers all RX210 Group products except chip version C products.

Table 1.1 lists the RX210 Group Chip Version B and C Products. In the table, B indicates chip version B and C indicates chip version C.

**Table 1.1   RX210 Group Chip Version B and C Products**

| ROM/RAM | Number of Pins | | | | |
|---|---|---|---|---|---|
| | 48 pins | 64 pins | 80 pins | 100 pins | 144 and 145 pins |
| 1 MB/96 KB | — | — | — | B [1] | B [2] |
| 768 KB/96 KB | — | — | — | B [1] | B [2] |
| 512 KB/64 KB | — | C | C | C | B [2] |
| 384 KB/64 KB | — | C | C | C | B [2] |
| 256 KB/32 KB | B | B | B | B | B [2] |
| 128 KB/16 KB | B | B | B | B | B [2] |
| 96 KB/16 KB | B | B | — | — | — |
| 64 KB/12 KB | B | B | — | — | — |

Notes:
  1. Bit rate of the RSPI can be set to a maximum of 16 Mbps.
  2. Bit rate of the RSPI can be set to a maximum of 16 Mbps, TPU is on-chip, and all 12 channels of SCIc can be used.

## 2. Differences of Specifications Between Chip Versions B and C

Chip version B has the same functions as chip version C. Furthermore chip version B has additional and improved functions. The same software can be used for functions common to these two chip versions.

Table 2.1 lists the Additional, Improved, and Changed Functions in Chip Version B. Figure 2.1 shows the Software Compatibility Between Chip Versions B and C.

**Table 2.1   Additional, Improved, and Changed Functions in Chip Version B**

| No. | Addition/Improvement | | Description | Reference |
|---|---|---|---|---|
| 1 | Operating power control mode | Addition | Added middle-speed operating mode 2A and 2B. | 2.1.1 |
| 2 | PLL power control register | Addition | Added the register to turn on and off the PLL power supply. | 2.1.2 |
| 3 | 16-bit timer pulse unit (TPU) | Addition | Added the 16-bit timer pulse unit (only for products with 144 pins or more). | 2.1.3 |
| 4 | Serial communications interface (SCIc) | Addition | Added 6 channels. All 12 channels can be used (only for products with 144 pins or more). | 2.1.4 |
| 5 | Low-speed operating mode 1 | Improvement | Improved the maximum frequency. | 2.2.1 |
| 6 | Serial peripheral interface (RSPI) | Improvement | Improved the maximum bit rate from 8.0 Mbps to16.0 Mbps (only for chip version B products with 768 KB or more of the flash memory, or with 144 pins or more). | 2.2.2 |
| 7 | Specification of the software cut 0 bits (SOFTCUT[2:0]) | Specification changed | No control function provided for supplying power to the flash memory when in software standby mode. | 2.3.1 |
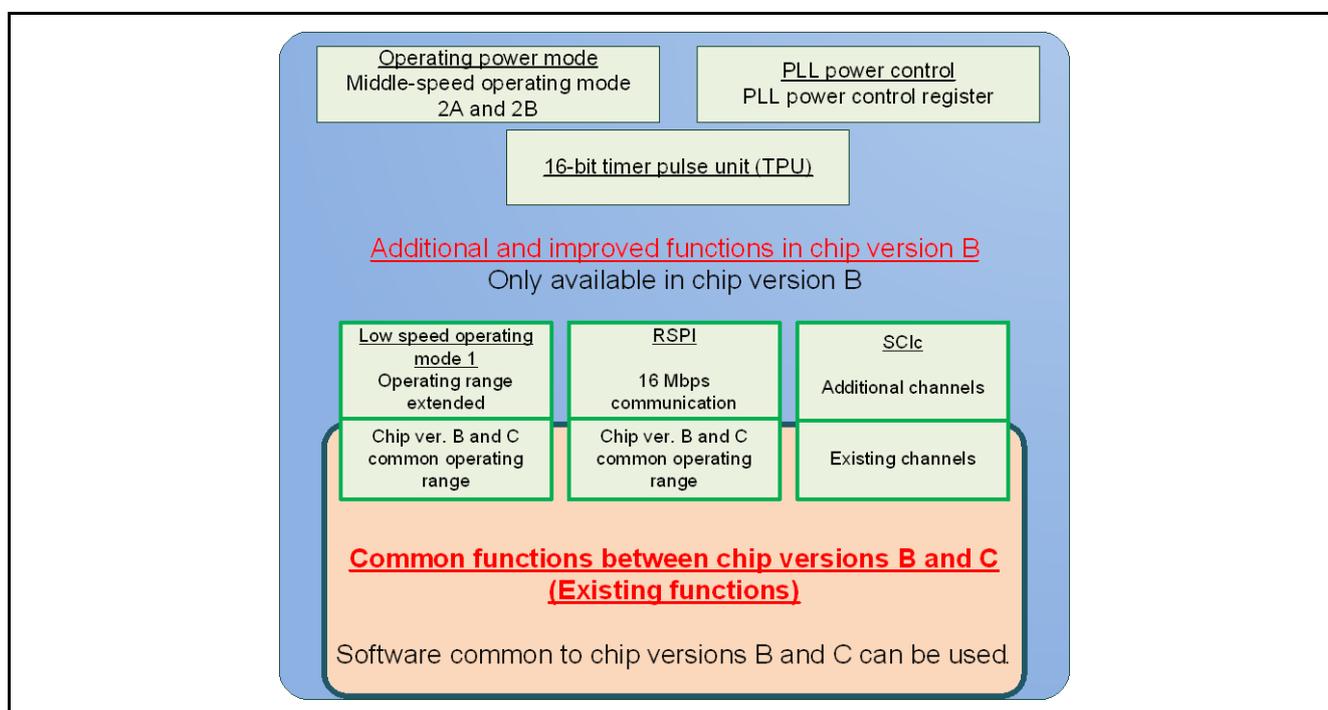


**Figure 2.1   Software Compatibility Between Chip Versions B and C**

## 2.1 Functions Added in Chip Version B

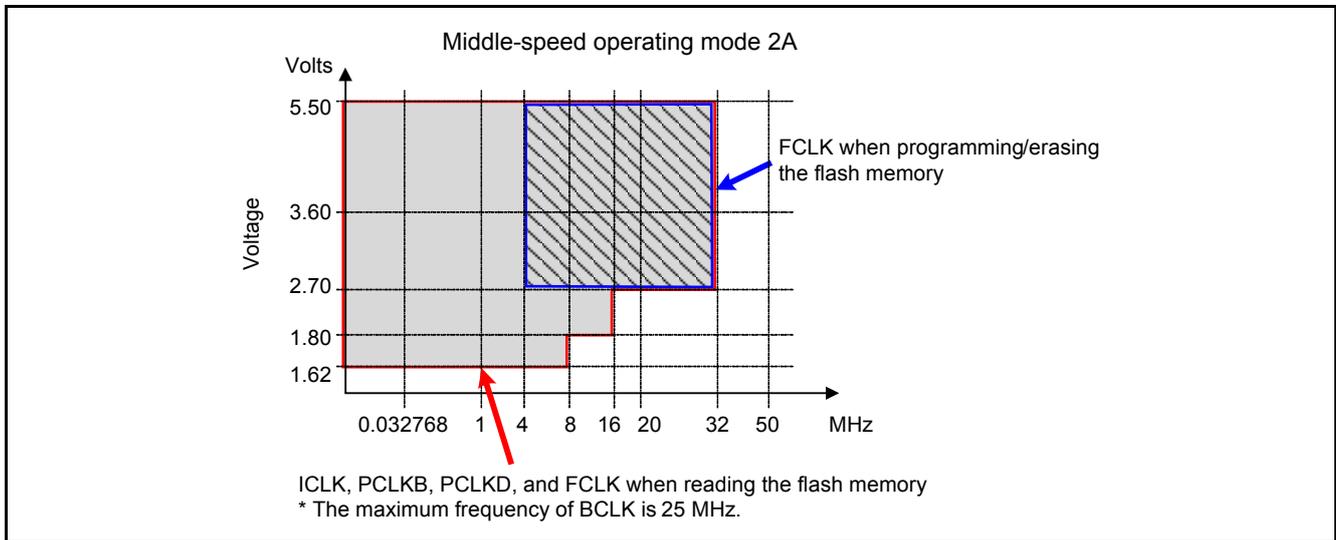### 2.1.1 Operating Power Control Modes

Middle-speed operating modes 2A and 2B are added in chip version B.

Middle-speed operating mode 2A can reduce power consumption and is more suitable for low-speed operation than middle-speed operating mode 1A or 1B. If operating in middle-speed operating mode 1A, 1B, and 2A under the same operating conditions (frequency and voltage), middle-speed operating mode 2A can reduce the power consumption the most.

Middle-speed operating mode 2B is based on middle-speed operating mode 2A and can reduce power consumption when programming/erasing the flash memory in the low-speed and low power voltage operating range.

When reading the flash memory in middle-speed operating mode 2B, the operating frequency and operating voltage ranges are the same as these in middle-speed operating mode 2A.

Figure 2.2 shows the Operating Frequency and Operating Voltage Ranges in Middle-Speed Operating Mode 2A and Figure 2.3 shows the Operating Frequency and Operating Voltage Ranges in Middle-Speed Operating Mode 2B.



**Figure 2.2  Operating Frequency and Operating Voltage Ranges in Middle-Speed Operating Mode 2A**
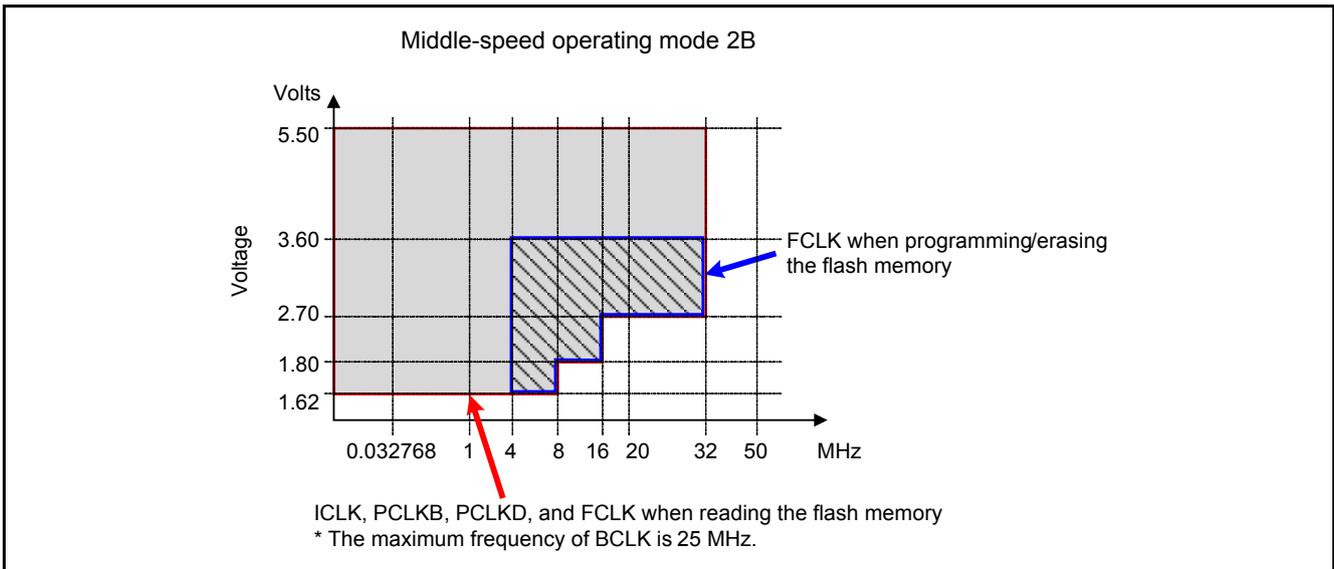
**Figure 2.3  Operating Frequency and Operating Voltage Ranges in Middle-Speed Operating Mode 2B**

### 2.1.2      PLL Power Control Register (PLLPCR)

The PLL power control register (PLLPCR) is only available in chip version B. With this register, when PLL is not used, the PLL power supply can be turned off to reduce power consumption.

### 2.1.3      16-Bit Timer Pulse Unit (TPU)

The TPU consists of six 16-bit timers and is the peripheral function which is implemented only in chip version B products with more than or equal to 144 pins.

### 2.1.4      Serial Communications Interface (SCIc)

Chip version B products with more than or equal to 144 pins can use all 12 channels (SCI0 to SCI11) of SCIc.

Table 2.2 shows the Available SCIc Channels for Each Pin Package.

**Table 2.2   Available SCIc Channels for Each Pin Package**

| Channel | Package | | | | |
|---|---|---|---|---|---|
| | 48 pins | 64 pins | 80 pins | 100 pins | 144 and 145 pins |
| SCI0 | N/A | N/A | Available | Available | Available |
| SCI1 | Available | Available | Available | Available | Available |
| SCI2 | N/A | N/A | N/A | N/A | Available |
| SCI3 | N/A | N/A | N/A | N/A | Available |
| SCI4 | N/A | N/A | N/A | N/A | Available |
| SCI5 | Available | Available | Available | Available | Available |
| SCI6 | Available | Available | Available | Available | Available |
| SCI7 | N/A | N/A | N/A | N/A | Available |
| SCI8 | Available | Available | Available | Available | Available |
| SCI9 | N/A | Available | Available | Available | Available |
| SCI10 | N/A | N/A | N/A | N/A | Available |
| SCI11 | N/A | N/A | N/A | N/A | Available |

## 2.2　Functions Improved in Chip Version B

### 2.2.1　Maximum Operating Frequency of Low-Speed Operating Mode 1

The operating frequency ranges of clocks in low-speed operating mode 1 are improved in chip version B.

Table 2.3 lists the comparison of low-speed operating mode 1 between chip versions B and C.

**Table 2.3　Comparison of Low-Speed Operating Mode 1 (VCC = 2.7 to 5.5 V)**

| Voltage | Maximum Operating Frequency | |
|---|---|---|
| | ICLK, FCLK, PCLKB, PCLKD, and BCLK when reading the flash memory | |
| | Chip version B | Chip version C |
| VCC = 2.7 to 5.5 V | 8 MHz | 1 MHz |
| VCC = 1.8 to 2.7 V | 4 MHz | |
| VCC = 1.62 to 1.8 V | 2 MHz | |

### 2.2.2　Communication Rate of the RSPI

The maximum bit rate is 16.0 Mbps in chip version B products with 768 KB or more of the flash memory, or with more than or equal to 144 pins. For other products, the maximum bit rate is 8 Mbps.

## 2.3　Function Changed in Chip Version B

### 2.3.1　Software Cut 0 Bits (SOFTCUT[2:0])

The SOFTCUT[2:0] bits are used to control the following during software standby mode:

- POR low power consumption function

- Power supply to HOCO

- Power supply to the flash memory

With chip version B, power supply to the flash memory does not need to be controlled and the same software can be used as chip version C.

## 3.   Reference Documents

User's Manual: Hardware
    RX210 Group User's Manual: Hardware Rev.1.40 (R01UH0037EJ)
    The latest version can be downloaded from the Renesas Electronics website.


Technical Update/Technical News
    The latest information can be downloaded from the Renesas Electronics website.



## Website and Support

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    http://www.renesas.com

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| REVISION HISTORY | | RX210 Group Application Note<br>Differences Between Chip Versions B and C | |
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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# RENESAS

## Renesas Electronics Corporation

http://www.renesas.com

**SALES OFFICES**

Refer to "http://www.renesas.com/" for the latest and detailed information.

**Renesas Electronics America Inc.**
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141