RX210 and RX220 Groups

Comparison of the RX210 and RX220 Group MCUs

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Abstract

This document compares chip version B and chip version C of the RX210 Group to the 100-pin package of the RX220 Group.

Products

RX210 Group, chip version B and chip version C

RX220 Group 100-pin package

Note: Items in red indicate a difference between the groups.

Contents

1. Comparison of Functions

Table 1.1 lists the comparison of the modules. For details on the modules, refer to chapter 4 Detailed Comparisons and chapter 5 Reference Documents.

Table 1.1 Module Comparison

Module	RX210	RX220
Voltage detection circuit (LVDA)	Included	Included
Clock frequency accuracy measurement circuit (CAC)	Included	Included
Low power consumption functions	Included	Included
Register write protection function	Included	Included
External bus extension	Included	Not included
DMA controller (DMACA)	Included	Included
Data transfer controller (DTC)	Included	Included
Event link controller (ELC)	Included	Included
Multi-function pin controller (MPC)	Included	Included
Multi-function timer pulse unit 2 (MTU2)	Included	Included
Port output enable 2 (POE2)	Included	Included
8-bit timer (TMR)	Included	Included
Compare match timer (CMT)	Included	Included
Realtime clock (RTC)	Included	Included
Watchdog timer (WDTA)	Included	Not included
Independent watchdog timer (IWDT)	Included	Included
Serial communications interface (SCI)	Included	Included
IrDA interface (IRDA)	Included	Included
I^2C bus interface (RIIC)	Included	Included
Serial peripheral interface (RSPI)	Included	Included
CRC calculator (CRC)	Included	Included
12-bit A/D converter (S12AD)	Included	Included
D/A converter (DA)	Included	Not included
Temperature sensor (TEMPS)	Included	Not included
Comparator A (CMPA)	Included	Included
Comparator B (CMPB)	Included	Not included
Data operation circuit (DOC)	Included	Included
E2 DataFlash memory	Included	Included
FCU RAM	Included	Not included

2. Overview Comparison

Table 2.1 to Table 2.3 list a comparison of the functions.

Table 2.1 Comparison of the Functions (1/3)

Item		RX210	RX220
CPU	Maximum operating frequency	50 MHz	32 MHz
Memory	ROM capacity	64 K, 96 K, 128 K, 256 K, 384 K, 512 K, 768 K, 1 Mbyte	32 K, 64 K, 128 K, 256 Kbytes
	RAM capacity	12 K, 16 K, 20 K, 32 K, 64 K, 96 Kbytes	4 K, 8 K, 16 Kbytes
MCU operating modes		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)	Single-chip mode
Clock generation circuit		Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator	Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, and IWDT-dedicated on-chip oscillator
System clock (ICLK)		50 MHz (max.)	32 MHz (max.)
Peripheral module clock (PCLKB)		32 MHz (max.)	32 MHz (max.)
Peripheral module clock (PCLKD)		50 MHz (max.)	32 MHz (max.)
External bus clock (BCLK)		12.5 MHz (max.)	Not applicable
Flash interface clock (FCLK)		32 MHz (max.)	32 MHz (max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset	RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Low power consumption facilities		Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode	Sleep mode, all-module clock stop mode, and software standby mode

Note:
1. These modes are only available in RX210 chip version B. They are not available in chip version C.

Table 2.2 Comparison of the Functions (2/3)

Item		RX210	RX220
Function for lower operating power consumption		High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A (1), middle-speed operating mode 2B (1), low-speed operating mode 1, low-speed operating mode 2	Middle-speed operating mode 1A, middle-speed operating mode 1B, low-speed operating mode 1, low-speed operating mode 2
Interrupt vectors		167	106
Non-maskable interrupts		NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt	NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt
External bus extension		Included	Not included
General I/O ports		Open-drain outputs: 54 ports usable	Open-drain outputs: 35 ports usable
ELC		59 types; Capable of event link operation for port B and port E	46 types; Capable of event link operation for port B
WDTA		14 bits × 1 channel	Not included
RTC		Time count	Time count or 32-bit binary count in second units basis selectable
SCI	Channels	6	5
	Detection of a start bit in asynchronous mode	Low level only	Low level or falling edge is selectable
IRDA		Not included	1 channel (SCI5 is used)
S12AD	Minimum conversion time	1.0 µs per channel (in operation with ADCLK at 50 MHz)	1.56 µs per channel (in operation with ADCLK at 32 MHz)
TEMPS		Included	Not included
DA	Channels	2	Not included
	Resolution	10-bit	
	Output voltage	0 V to VREFH	
CMPB		2 channels	Not included

Table 0.3 Comparison of the Functions (3/3)

Item		RX210	RX220
Power supply voltage/ Operating frequency	VCC = 1.62 to 1.8 V	20 MHz	8 MHz
	VCC = 1.8 to 2.7 V	32 MHz	
	VCC = 2.7 to 5.5 V	50 MHz	32 MHz

3. Comparison of Pin Functions

Table 3.1 to Table 3.5 list a Comparison of the Pin Functions.

Table 3.1 Comparison of the Pin Functions (1/5)

Port	RX210	RX220
P03	DA0	- (1)
P05	DA1	- (1)
P07	ADTRG0#	ADTRG0#
P12	TMCI1, SCL, IRQ2	TMCI1, SCL, IRQ2
P13	MTIOC0B, TMO3, SDA, IRQ3	MTIOC0B, TMO3, SDA, IRQ3
P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4
P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5
P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL-DS, IRQ6, RTCOUT, ADTRG0#	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, RTCOUT, ADTRG0#
P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA-DS, IRQ7	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA, IRQ7
P20	MTIOC1A, TMRI0, TXD0, SMOSI0, SSDA0	MTIOC1A, TMRI0
P21	MTIOC1B, TMCI0, RXD0, SMISO0, SSCL0	MTIOC1B, TMCI0
P22	MTIOC3B, MTCLKC, TMO0, SCK0	MTIOC3B, MTCLKC, TMO0
P23	MTIOC3D, MTCLKD, CTS0#, RTS0#, SS0#	MTIOC3D, MTCLKD
P24	CS0#, MTIOC4A, MTCLKA, TMRI1	MTIOC4A, MTCLKA, TMRI1
P25	CS1#, MTIOC4C, MTCLKB, ADTRG0#	MTIOC4C, MTCLKB, ADTRG0#
P26	CS2#, MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1
P27	CS3#, MTIOC2B, TMCI3, SCK1	MTIOC2B, TMCI3, SCK1

Note:
1. General I/O ports only.

Table 3.2 Comparison of the Pin Functions (2/5)

Port	RX210	RX220
P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0-DS, RTCIC0	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0
P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1-DS, RTCIC1	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1
P32	MTIOC0C, TMO3, TXD6, SMOSI6, SSDA6, IRQ2-DS, RTCOUT, RTCIC2	MTIOC0C, TMO3, TXD6, SMOSI6, SSDA6, IRQ2, RTCOUT
P33	MTIOC0D, TMRI3, POE3#, RXD6, SMISO6, SSCL6, IRQ3-DS	MTIOC0D, TMRI3, POE3#, RXD6, SMISO6, SSCL6, IRQ3
P34	MTIOC0A, TMCI3, POE2#, SCK6, IRQ4	MTIOC0A, TMCI3, POE2#, SCK6, IRQ4
P35	NMI	NMI
P36	EXTAL	EXTAL
P37	XTAL	XTAL
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P43	AN003	AN003
P44	AN004	AN004
P45	AN005	AN005
P46	AN006	AN006
P47	AN007	AN007
P50	WR0#, WR#	- (1)
P51	WR1#, BC1#, WAIT#	- (1)
P52	RD#	- (1)
P53	BCLK	- (1)
P54	ALE, MTIOC4B, TMCI1	MTIOC4B, TMCI1
P55	WAIT#, MTIOC4D, TMO3	MTIOC4D, TMO3

Note:
1. General I/O ports only.

Table 3.3 Comparison of the Pin Functions (3/5)

Port	RX210	RX220
PA0	A0, BC0#, MTIOC4A, SSLA1, CACREF	MTIOC4A, SSLA1, CACREF
PA1	A1, MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA
PA2	A2, RXD5, SMISO5, SSCL5, SSLA3	RXD5, SMISO5, SSCL5, SSLA3, IRRXD5
PA3	A3, MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6-DS, CMPB1	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRRXD5, IRQ6
PA4	A4, MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5-DS, CVREFB1	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRTXD5, IRQ5
PA5	A5, RSPCKA	RSPCKA
PA6	A6, MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA
PA7	A7, MISOA	MISOA
PB0	A8, MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA
PB1	A9, MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4-DS	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4
PB2	A10, CTS6#, RTS6#, SS6#	CTS6#, RTS6#, SS6#
PB3	A11, MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6
PB4	A12, CTS9#, RTS9#, SS9#	CTS9#, RTS9#, SS9#
PB5	A13, MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9	MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9
PB6	A14, MTIOC3D, RXD9, SMISO9, SSCL9	MTIOC3D, RXD9, SMISO9, SSCL9
PB7	A15, MTIOC3B, TXD9, SMOSI9, SSDA9	MTIOC3B, TXD9, SMOSI9, SSDA9
PC0	A16, MTIOC3C, CTS5#, RTS5#, SS5#, SSLA1	MTIOC3C, CTS5#, RTS5#, SS5#, SSLA1
PC1	A17, MTIOC3A, SCK5, SSLA2	MTIOC3A, SCK5, SSLA2
PC2	A18, MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3	MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3 , IRRXD5

Table 3.4 Comparison of the Pin Functions (4/5)

Port	RX210	RX220
PC3	A19, MTIOC4D, TXD5, SMOSI5, SSDA5	MTIOC4D, TXD5, SMOSI5, SSDA5, IRTXD5,
PC4	A20, CS3#, MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, CTS8#, RTS8#, SS8#, SSLA0	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, SSLA0
PC5	A21, CS2#, WAIT#, MTIOC3B, MTCLKD, TMRI2, SCK8, RSPCKA	MTIOC3B, MTCLKD, TMRI2, RSPCKA
PC6	A22, CS1#, MTIOC3C, MTCLKA, TMCI2, RXD8, SMISO8, SSCL8, MOSIA	MTIOC3C, MTCLKA, TMCI2, MOSIA
PC7	A23, CS0#, MTIOC3A, TMO2, MTCLKB, TXD8, SMOSI8, SSDA8, MISOA, CACREF	MTIOC3A, TMO2, MTCLKB, MISOA, CACREF
PD0	D0[A0/D0], IRQ0	IRQ0
PD1	D1[A1/D1], MTIOC4B, IRQ1	MTIOC4B, IRQ1
PD2	D2[A2/D2], MTIOC4D, IRQ2	MTIOC4D, IRQ2
PD3	D3[A3/D3], POE8#, IRQ3	POE8#, IRQ3
PD4	D4[A4/D4], POE3#, IRQ4	POE3#, IRQ4
PD5	D5[A5/D5], MTIC5W, POE2#, IRQ5	MTIC5W, POE2#, IRQ5
PD6	D6[A6/D6], MTIC5V, POE1#, IRQ6	MTIC5V, POE1#, IRQ6
PD7	D7[A7/D7], MTIC5U, POE0#, IRQ7	MTIC5U, POE0#, IRQ7
PE0	D8[A8/D8], SCK12, AN008	SCK12, AN008
PE1	D9[A9/D9], MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN009, CMPB0	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN009
PE2	D10[A10/D10], MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7-DS, AN010, CVREFB0	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN010
PE3	D11[A11/D11], MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1	MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1
PE4	D12[A12/D12], MTIOC4D, MTIOC1A, AN012, CMPA2	MTIOC4D, MTIOC1A, AN012, CMPA2
PE5	D13[A13/D13], MTIOC4C, MTIOC2B, IRQ5, AN013	MTIOC4C, MTIOC2B, IRQ5, AN013
PE6	D14[A14/D14], IRQ6, AN014	IRQ6, AN014
PE7	D15[A15/D15], IRQ7, AN015	IRQ7, AN015

Table 3.5 Comparison of the Pin Functions (5/5)

Port	RX210	RX220
PH0	CACREF	CACREF
PH1	TMO0, IRQ0	TMO0, IRQ0
PH2	TMRI0, IRQ1	TMRI0, IRQ1
PH3	TMCI0	TMCI0
PJ1	MTIOC3A	MTIOC3A
PJ3	MTIOC3C, CTS6#, RTS6#, SS6#	MTIOC3C, CTS6#, RTS6#, SS6#
—	VREFH	Non-connection
—	VREFL	Non-connection

4. Detailed Comparisons

4.1 Comparison of the Operating Modes

Table 4.1 lists a Comparison of the Operating Modes. Table 4.2 lists a Comparison of the I/O Register Associated With the Operating Modes.

Table 4.1 Comparison of the Operating Modes

RX210	RX220
Single-chip mode, boot mode, user boot mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode	Single-chip mode, boot mode, and user boot mode

Table 4.2 Comparison of the I/O Register Associated With the Operating Modes

Register Symbol	Bit Symbol	RX210	RX220
SYSCR0	-	System Control Register 0	-

4.2 Comparison of the Resets

Table 4.3 lists a Comparison of the Resets. Table 4.4 lists a Comparison of the I/O Registers Associated With the Resets.

Table 4.3 Comparison of the Resets

RX210	RX220
RES# pin reset, power-on reset, voltage monitoring 0 reset, voltage monitoring 1 reset, voltage monitoring 2 reset, deep software standby reset, independent watchdog timer reset, watchdog timer reset, and software reset	RES# pin reset, power-on reset, voltage monitoring 0 reset, voltage monitoring 1 reset, voltage monitoring 2 reset, independent watchdog timer reset, and software reset

Table 4.4 Comparison of the I/O Registers Associated With the Resets

Register Symbol	Bit Symbol	RX210	RX220
RSTSR0	DPSRSTF	Deep Software Standby Reset Detect Flag	Reserved
RSTSR2	WDTRF	Watchdog Timer Reset Detect Flag	Reserved

4.3 Comparison of the Option-Setting Memory

Table 4.5 lists a Comparison of the I/O Register Associated With the Option-Setting Memory.

Table 4.5 Comparison of the I/O Register Associated With the Option-Setting Memory

Register Symbol	Bit Symbol	RX210	RX220
OFS0	WDTSTRT	WDT Start Mode Select	Reserved
	WDTTOPS[1:0]	WDT Timeout Period Select	Reserved
	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	Reserved
	WDTRPES[1:0]	WDT Window End Position Select	Reserved
	WDTRPSS[1:0]	WDT Window Start Position Select	Reserved
	WDTRSTIRQS	WDT Reset Interrupt Request Select	Reserved

4.4 Comparison of the Voltage Detection Circuit

Table 4.6 lists a Comparison of the Voltage Detection Circuit.

Table 4.6 Comparison of the Voltage Detection Circuit

Item	RX210	RX220
Event link function	Vdet1, Vdet2 passage detection event output	Vdet1 passage detection event output

4.5 Comparison of the Clock Generation Circuit

Table 4.7 lists a Comparison of the Clock Generation Circuit. Table 4.8 lists a Comparison of I/O Registers Associated With the Clock Generation Circuit.

Table 4.7 Comparison of the Clock Generation Circuit

Item	RX210	RX220
Use	● Generates the ICLK supplied to the CPU, DMAC, DTC, ROM, and RAM. ● Generates the PCLKB and PCLKD supplied to peripheral modules. ● Generates the FCLK supplied to the flash interface. ● Generates the BCLK supplied to the external bus. ● Generates the CAC clock (CACCLK) supplied to the CAC. ● Generates the RTC-dedicated sub-clock (RTCSCLK) supplied to the RTC. ● Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.	● Generates the ICLK supplied to the CPU, DMAC, DTC, ROM, and RAM. ● Generates the PCLKB and PCLKD supplied to peripheral modules. ● Generates the FCLK supplied to the flash interface. ● Generates the CAC clock (CACCLK) supplied to the CAC. ● Generates the RTC-dedicated sub-clock (RTCSCLK) supplied to the RTC. ● Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.
Operating frequencies	● ICLK: 50 MHz ● PCLKB: 32 MHz ● PCLKD: 50 MHz ● FCLK: 4 to 32 MHz (for programming and erasing the ROM and E2 DataFlash); 32 MHz (max) (for reading from the E2 DataFlash) ● CACCLK: Same as frequency of each oscillator ● RTCSCLK: 32.768 kHz ● IWDTCLK: 125 kHz ● BCLK: 25 MHz (max.) ● BCLK pin output: 12.5 MHz (max.)	● ICLK: 32 MHz ● PCLKB: 32 MHz ● PCLKD: 32 MHz ● FCLK: 4 to 32 MHz (for programming and erasing the ROM and E2 DataFlash); 32 MHz (max) (for reading from the E2 DataFlash) ● CACCLK: Same as frequency of each oscillator ● RTCSCLK: 32.768 kHz ● IWDTCLK: 125 kHz
PLL circuit	● Input clock source: Main clock ● Input pulse frequency division ratio: Selectable from 1, 2, and 4 ● Input frequency: 4 to 12.5 MHz ● Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, and 25 ● VCO oscillation frequency: 50 to 100 MHz	Not included
Control of output on the BCLK pin	● BCLK clock output or high-level output is selectable ● BCLK or BCLK/2 is selectable	Not included

Table 4.8 Comparison of I/O Registers Associated With the Clock Generation Circuit

Register Symbol	Bit Symbol	RX210	RX220
SCKCR	PSTOP1	BCLK Pin Output Control	Reserved
SCKCR3	CKSEL[2:0]	Clock Source Select 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Only set the values listed above.	Clock Source Select 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator Only set the values listed above.
VRCR	-	Voltage Regulator Control Register	-
PLLCR	-	PLL Control Register	-
PLLCR2	-	PLL Control Register 2	-
BCKCR	-	External Bus Clock Control Register	-
PLLPCR (1)	-	PLL Power Control Register	-

Note:
1. The PLLPCR register is only present in RX210 chip version B. It is not present in chip version C.

4.6 Comparison of the Low Power Consumption Functions

Table 4.9 to Table 4.17 list comparisons of the low power consumption function. Table 4.18 to Table 4.19 list a comparison of I/O registers associated with the low power consumption functions.

Table 4.9 Comparison of the Low Power Consumption Functions

Item	RX210	RX220
Function for lower operating power consumption	● High-speed operating mode ● Middle-speed operating mode 1A ● Middle-speed operating mode 1B ● Middle-speed operating mode 2A (1) ● Middle-speed operating mode 2B (1) ● Low-speed operating mode 1 ● Low-speed operating mode 2	● Middle-speed operating mode 1A ● Middle-speed operating mode 1B ● Low-speed operating mode 1 ● Low-speed operating mode 2
Low power consumption modes	● Sleep mode ● All-module clock stop mode ● Software standby mode ● Deep software standby mode	● Sleep mode ● All-module clock stop mode ● Software standby mode
BCLK output control function	BCLK output or high-level output can be selected.	

Note:
1. This mode is only available in RX210 chip version B. It is not available in chip version C.

Table 4.10 Comparison When the Operating Voltage Range is 3.6 to 5.5 V During Flash Memory Read

Operating Power Control Mode	Clock	Maximum Operating Frequency		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	ICLK	50 MHz	50 MHz	-
	FCLK	32 MHz	32 MHz	-
	PCLKD	50 MHz	50 MHz	-
	PCLKB	32 MHz	32 MHz	-
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 1A	ICLK	32 MHz	32 MHz	32 MHz
	FCLK	32 MHz	32 MHz	32 MHz
	PCLKD	32 MHz	32 MHz	32 MHz
	PCLKB	32 MHz	32 MHz	32 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 1B	ICLK	32 MHz	32 MHz	32 MHz
	FCLK	32 MHz	32 MHz	32 MHz
	PCLKD	32 MHz	32 MHz	32 MHz
	PCLKB	32 MHz	32 MHz	32 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 2A	ICLK	32 MHz	-	-
	FCLK	32 MHz	-	-
	PCLKD	32 MHz	-	-
	PCLKB	32 MHz	-	-
	BCLK	25 MHz	-	-
Middle-speed operating mode 2B	ICLK	32 MHz	-	-
	FCLK	32 MHz	-	-
	PCLKD	32 MHz	-	-
	PCLKB	32 MHz	-	-
	BCLK	25 MHz	-	-
Low-speed operating mode 1	ICLK	8 MHz	1 MHz	8 MHz
	FCLK	8 MHz	1 MHz	8 MHz
	PCLKD	8 MHz	1 MHz	8 MHz
	PCLKB	8 MHz	1 MHz	8 MHz
	BCLK	8 MHz	1 MHz	-
Low-speed operating mode 2	ICLK	32.768 MHz	32.768 MHz	32.768 MHz
	FCLK	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKD	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKB	32.768 MHz	32.768 MHz	32.768 MHz
	BCLK	32.768 MHz	32.768 MHz	-

Table 4.11 Comparison When the Operating Voltage Range is 3.6 to 5.5 V During Flash Memory Programming/Erasure

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	FCLK	4 to 32 MHz	4 to 32 MHz	-
Middle-speed operating mode 1A	FCLK	4 to 32 MHz	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 1B	FCLK	-	-	-
Middle-speed operating mode 2A	FCLK	4 to 32 MHz	-	-
Middle-speed operating mode 2B	FCLK	-	-	-
Low-speed operating mode 1	FCLK	-	-	-
Low-speed operating mode 2	FCLK	-	-	-

Table 4.12 Comparison When the Operating Voltage Range is 2.7 to 3.6 V During Flash Memory Read

Operating Power Control Mode	Clock	Maximum Operating Frequency		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	ICLK	50 MHz	50 MHz	-
	FCLK	32 MHz	32 MHz	-
	PCLKD	50 MHz	50 MHz	-
	PCLKB	32 MHz	32 MHz	-
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 1A	ICLK	32 MHz	32 MHz	32 MHz
	FCLK	32 MHz	32 MHz	32 MHz
	PCLKD	32 MHz	32 MHz	32 MHz
	PCLKB	32 MHz	32 MHz	32 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 1B	ICLK	32 MHz	32 MHz	32 MHz
	FCLK	32 MHz	32 MHz	32 MHz
	PCLKD	32 MHz	32 MHz	32 MHz
	PCLKB	32 MHz	32 MHz	32 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 2A	ICLK	32 MHz	-	-
	FCLK	32 MHz	-	-
	PCLKD	32 MHz	-	-
	PCLKB	32 MHz	-	-
	BCLK	25 MHz	-	-
Middle-speed operating mode 2B	ICLK	32 MHz	-	-
	FCLK	32 MHz	-	-
	PCLKD	32 MHz	-	-
	PCLKB	32 MHz	-	-
	BCLK	25 MHz	-	-
Low-speed operating mode 1	ICLK	8 MHz	1 MHz	8 MHz
	FCLK	8 MHz	1 MHz	8 MHz
	PCLKD	8 MHz	1 MHz	8 MHz
	PCLKB	8 MHz	1 MHz	8 MHz
	BCLK	8 MHz	1 MHz	-
Low-speed operating mode 2	ICLK	32.768 MHz	32.768 MHz	32.768 MHz
	FCLK	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKD	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKB	32.768 MHz	32.768 MHz	32.768 MHz
	BCLK	32.768 MHz	32.768 MHz	-

Table 4.13 Comparison When the Operating Voltage Range is 2.7 to 3.6 V During Flash Memory Programming/Erasure

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	FCLK	4 to 32 MHz	4 to 32 MHz	-
Middle-speed operating mode 1A	FCLK	4 to 32 MHz	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 1B	FCLK	4 to 32 MHz	4 to 32 MHz	4 to 32 MHz
Middle-speed operating mode 2A	FCLK	4 to 32 MHz	-	-
Middle-speed operating mode 2B	FCLK	4 to 32 MHz	-	-
Low-speed operating mode 1	FCLK	-	-	-
Low-speed operating mode 2	FCLK	-	-	-

Table 4.14 Comparison When the Operating Voltage Range is 1.8 to 2.7 V During Flash Memory Read

Operating Power Control Mode	Clock	Maximum Operating Frequency		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	ICLK	-	-	-
	FCLK	-	-	-
	PCLKD	-	-	-
	PCLKB	-	-	-
	BCLK	-	-	-
Middle-speed operating mode 1A	ICLK	32 MHz	32 MHz	8 MHz
	FCLK	32 MHz	32 MHz	8 MHz
	PCLKD	32 MHz	32 MHz	8 MHz
	PCLKB	32 MHz	32 MHz	8 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 1B	ICLK	32 MHz	32 MHz	8 MHz
	FCLK	32 MHz	32 MHz	8 MHz
	PCLKD	32 MHz	32 MHz	8 MHz
	PCLKB	32 MHz	32 MHz	8 MHz
	BCLK	25 MHz	25 MHz	-
Middle-speed operating mode 2A	ICLK	16 MHz	-	-
	FCLK	16 MHz	-	-
	PCLKD	16 MHz	-	-
	PCLKB	16 MHz	-	-
	BCLK	16 MHz	-	-
Middle-speed operating mode 2B	ICLK	16 MHz	-	-
	FCLK	16 MHz	-	-
	PCLKD	16 MHz	-	-
	PCLKB	16 MHz	-	-
	BCLK	16 MHz	-	-
Low-speed operating mode 1	ICLK	4 MHz	1 MHz	4 MHz
	FCLK	4 MHz	1 MHz	4 MHz
	PCLKD	4 MHz	1 MHz	4 MHz
	PCLKB	4 MHz	1 MHz	4 MHz
	BCLK	4 MHz	1 MHz	-
Low-speed operating mode 2	ICLK	32.768 MHz	32.768 MHz	32.768 MHz
	FCLK	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKD	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKB	32.768 MHz	32.768 MHz	32.768 MHz
	BCLK	32.768 MHz	32.768 MHz	-

Table 4.15 Comparison When the Operating Voltage Range is 1.8 to 2.7 V During Flash Memory Programming/Erasure

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	FCLK	-	-	-
Middle-speed operating mode 1A	FCLK	-	-	-
Middle-speed operating mode 1B	FCLK	4 to 32 MHz	4 to 32 MHz	4 to 8 MHz
Middle-speed operating mode 2A	FCLK	-	-	-
Middle-speed operating mode 2B	FCLK	4 to 16 MHz	-	-
Low-speed operating mode 1	FCLK	-	-	-
Low-speed operating mode 2	FCLK	-	-	-

Table 4.16 Comparison When the Operating Voltage Range is 1.62 to 1.8 V During Flash Memory Read

Operating Power Control Mode	Clock	Maximum Operating Frequency		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	ICLK	-	-	-
	FCLK	-	-	-
	PCLKD	-	-	-
	PCLKB	-	-	-
	BCLK	-	-	-
Middle-speed operating mode 1A	ICLK	20 MHz	20 MHz	8 MHz
	FCLK	20 MHz	20 MHz	8 MHz
	PCLKD	20 MHz	20 MHz	8 MHz
	PCLKB	20 MHz	20 MHz	8 MHz
	BCLK	20 MHz	20 MHz	-
Middle-speed operating mode 1B	ICLK	20 MHz	20 MHz	8 MHz
	FCLK	20 MHz	20 MHz	8 MHz
	PCLKD	20 MHz	20 MHz	8 MHz
	PCLKB	20 MHz	20 MHz	8 MHz
	BCLK	20 MHz	20 MHz	-
Middle-speed operating mode 2A	ICLK	8 MHz	-	-
	FCLK	8 MHz	-	-
	PCLKD	8 MHz	-	-
	PCLKB	8 MHz	-	-
	BCLK	8 MHz	-	-
Middle-speed operating mode 2B	ICLK	8 MHz	-	-
	FCLK	8 MHz	-	-
	PCLKD	8 MHz	-	-
	PCLKB	8 MHz	-	-
	BCLK	8 MHz	-	-
Low-speed operating mode 1	ICLK	2 MHz	1 MHz	2 MHz
	FCLK	2 MHz	1 MHz	2 MHz
	PCLKD	2 MHz	1 MHz	2 MHz
	PCLKB	2 MHz	1 MHz	2 MHz
	BCLK	2 MHz	1 MHz	-
Low-speed operating mode 2	ICLK	32.768 MHz	32.768 MHz	32.768 MHz
	FCLK	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKD	32.768 MHz	32.768 MHz	32.768 MHz
	PCLKB	32.768 MHz	32.768 MHz	32.768 MHz
	BCLK	32.768 MHz	32.768 MHz	-

Table 4.17 Comparison When the Operating Voltage Range is 1.62 to 1.8 V During Flash Memory Programming/Erasure

Operating Power Control Mode	Clock	Operating Frequency Range		
		RX210 chip version B	RX210 chip version C	RX220
High-speed operating mode	FCLK	-	-	-
Middle-speed operating mode 1A	FCLK	-	-	-
Middle-speed operating mode 1B	FCLK	4 to 20 MHz	4 to 20 MHz	4 to 8 MHz
Middle-speed operating mode 2A	FCLK	-	-	-
Middle-speed operating mode 2B	FCLK	4 to 8 MHz	-	-
Low-speed operating mode 1	FCLK	-	-	-
Low-speed operating mode 2	FCLK	-	-	-

Table 4.18 Comparison of I/O Registers Associated With the Low Power Consumption Functions (1/2)

Register Symbol	Bit Symbol	RX210	RX220
SBYCR	OPE	Output Port Enable	Reserved
MSTPCRA	MSTPA19	D/A Converter Module Stop	Reserved
MSTPCRB	MSTPB8	Temperature Sensor module Stop	Reserved
	MSTPB10	Comparator B Module Stop	Reserved
	MSTPB31	Serial Communication Interface 0 Module Stop	Reserved
MSTPCRC	MSTPC1	RAM1 Module Stop	Reserved
	MSTPC27	Serial Communication Interface 0 Module Stop	Reserved
OPCCR	OPCM[2:0]	Operating Power Control Mode Select 000: High-speed operating mode 010: Middle-speed operating mode 1A 011: Middle-speed operating mode 1B 100: Middle-speed operating mode 2A (1) 101: Middle-speed operating mode 2B (1) 110: Low-speed operating mode 1 111: Low-speed operating mode 2 Only set the values listed above.	Operating Power Control Mode Select 010: Middle-speed operating mode 1A 011: Middle-speed operating mode 1B 110: Low-speed operating mode 1 111: Low-speed operating mode 2 Only set the values listed above.
PLLWTR	-	PLL Wait Control Register	-
HOCOWTCR2	RX210 HSTS2[3:0] RX220 HSTS2[4:0]	HOCO Wait Time Select 2 16 different wait times selectable from 3,072 cycles to 33,792 cycles.	HOCO Wait Time Select 2 32 different wait times selectable from 40 cycles to 33,792 cycles.
DPSBYCR	-	Deep Standby Control Register	-
DPSIER0	-	Deep Standby Interrupt Enable Register 0	-
DPSIER2	-	Deep Standby Interrupt Enable Register 2	-
DPSIFR0	-	Deep Standby Interrupt Flag Register 0	
DPSIFR2	-	Deep Standby Interrupt Flag Register 2	

Note:
1. This mode is only available in RX210 chip version B. It is not available in chip version C.

Table 4.19 Comparison of I/O Registers Associated With the Low Power Consumption Functions (2/2)

Register Symbol	Bit Symbol	RX210	RX220
DPSIEGR0	-	Deep Standby Interrupt Edge Register 0	-
DPSIEGR2	-	Deep Standby Interrupt Edge Register 2	-
DPSBKRy	-	Deep Standby Backup Register y	-

y = 0 to 31

Note:

This mode is only available in RX210 chip version B. It is not available in chip version C.

4.7 Comparison of the Register Write Protection Function

Table 4.20 lists a Comparison of Registers Protected by the PRCR Bits. Table 4.21 lists a Comparison of the I/O Register Associated With the Register Write Protection Function.

Table 4.20 Comparison of Registers Protected by the PRCR Bits

Bit Symbol	RX210	RX220
PRC0	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	Registers related to the clock generation circuit: SCKCR, SCKCR3, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2
PRC1	Registers related to the operating modes: SYSCR0, SYSCR1 Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 Registers related to clock generation circuit: MOFCR, HOCOPCR, PLLPCR Software reset register: SWRR	Register related to the operating modes: SYSCR1 Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, FHSSBYCR, HOCOWTCR2 Registers related to clock generation circuit: MOFCR, HOCOPCR Software reset register: SWRR
PRC2	VRCR	None
PRC3	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 4.21 Comparison of the I/O Register Associated With the Register Write Protection Function

Register Symbol	Bit Symbol	RX210	RX220
PRCR	PRCR2	Protect Bit 2	-

4.8 Comparison of the Interrupt Controller

Table 4.22 lists a Comparison of the Interrupt Controller. Table 4.23 lists a Comparison of I/O Registers Associated With the Interrupt Controller.

Table 4.22 Comparison of the Interrupt Controller

Item	RX210	RX220
Event link interrupt	The ELSR18I or ELSR19I interrupt is generated by an ELC event	The ELSR18I interrupt is generated by an ELC event
WDT underflow/refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error	None

Table 4.23 Comparison of I/O Registers Associated With the Interrupt Controller

Register Symbol	Bit Symbol	RX210	RX220
NMIER	WDTEN	WDT Underflow/Refresh Error Enable	Reserved
NMISR	WDTST	WDT Underflow/Refresh Error Status Flag	Reserved
NMICLR	WDTCLR	WDT Clear	Reserved

4.9 Comparison of Buses

Table 4.24 lists a Comparison of Buses. Table 4.25 lists a Comparison of I/O Registers Associated With the Buses.

Table 4.24 Comparison of Buses

Item	RX210	RX220
External bus	● Connected to the external devices ● Operates in synchronization with the BCLK	Not included

Table 4.25 Comparison of I/O Registers Associated With the Buses

Register Symbol	Bit Symbol	RX210	RX220
CSnCR (n = 0 to 3)	-	CSn Control Register	-
CSnREC	-	CSn Recovery Cycle Register	-
CSRECEN	-	CSn Recovery Cycle Insertion Enable Register	-
CSnMOD	-	CSn Mode Register	-
CSnWCR1	-	CSn Wait Control Register 1	-
CSnWCR2	-	CSn Wait Control Register 2	-
BEREN	TOEN	Timeout Detection Enable	Reserved
BERSR1	TO	Timeout	Reserved
BUSPRI	BPEB[1:0]	External Bus Priority Control	Reserved

4.10 Comparison of DMACA

Table 4.26 lists a Comparison of DMACA.

Table 4.26 Comparison of DMACA

Item	RX210	RX220
Event link function	Event link request is generated after one data transfer (for block, after one block transfer).	Not included

4.11 Comparison of the DTC

Table 4.27 lists a Comparison of the DTC. Table 4.28 lists a Comparison of the I/O Register Associated With the DTC.

Table 4.27 Comparison of the DTC

Item	RX210	RX220
DTC vector base address	Settable in 4 Kbyte units.	Settable in 1 Kbyte units.

Table 4.28 Comparison of the I/O Register Associated With the DTC

Register Symbol	Bit Symbol	RX210	RX220
DTCVBR	-	DTC Vector Base Address (Lower 12 bits) These bits are read as 0. The write value should be 0.	DTC Vector Base Address (Lower 10 bits) These bits are read as 0. The write value should be 0.
	-	DTC Vector Base Address (Upper 20 bits) The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27.	DTC Vector Base Address (Upper 22 bits) The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified by b27.

4.12 Comparison of the ELC

Table 4.29 lists a Comparison of the ELC. Table 4.30 to Table 4.33 list a comparison of I/O registers associated with the ELC.

Table 4.29 Comparison of the ELC

Item	RX210	RX220
Event link	● 59 types of event signals can be directly connected to modules. ● Event link operation is possible for port B and port E.	● 46 types of event signals can be directly connected to modules. ● Event link operation is possible for port B.

Table 4.30 Comparison of I/O Registers Associated With the ELC

Register Symbol	Bit Symbol	RX210	RX220
ELOPC	-	Event Link Option Setting Register C	-
PGR2	-	Port Group Setting Register 2	-
PGC2	-	Port Group Control Register 2	-

Table 4.31 Comparison of the ELSRn Register and Peripheral Functions

Register Symbol	Bit Symbol	RX210	RX220
		Peripheral functions that generate event signals to be linked	
ELSR1	-	MTU1	MTU1
ELSR2	-	MTU2	MTU2
ELSR3	-	MTU3	MTU3
ELSR4	-	MTU4	MTU4
ELSR7	-	CMT1	-
ELSR10	-	TMR0	TMR0
ELSR12	-	TMR2	TMR2
ELSR15	-	S12AD	S12AD
ELSR16	-	DA0	-
ELSR18	-	Interrupt 1	Interrupt 1
ELSR19	-	Interrupt 2	-
ELSR20	-	Output port group 1	Output port group 1
ELSR21	-	Output port group 2	-
ELSR22	-	Input port group 1	Input port group 1
ELSR23	-	Input port group 2	-
ELSR24	-	Single-port 0	Single-port 0
ELSR25	-	Single-port 1	Single-port 1
ELSR26	-	Single-port 2	-
ELSR27	-	Single-port 3	-
ELSR28	-	Clock source switching to LOCO	-
ELSR29	-	POE	-

Table 4.32 Comparison of the Event Signal Name Set in the ELSRn Register (1) and the Signal Numbers (1/2)

ELS[7:0] Bit Value	RX210	RX220
08h	MTU1 compare match 1A signal	MTU1 compare match 1A signal
09h	MTU1 compare match 1B signal	MTU1 compare match 1B signal
0Ah	MTU1 overflow signal	MTU1 overflow signal
0Bh	MTU1 underflow signal	MTU1 underflow signal
0Ch	MTU2 compare match 2A signal	MTU2 compare match 2A signal
0Dh	MTU2 compare match 2B signal	MTU2 compare match 2B signal
0Eh	MTU2 overflow signal	MTU2 overflow signal
0Fh	MTU2 underflow signal	MTU2 underflow signal
10h	MTU3 compare match 3A signal	MTU3 compare match 3A signal
11h	MTU3 compare match 3B signal	MTU3 compare match 3B signal
12h	MTU3 compare match 3C signal	MTU3 compare match 3C signal
13h	MTU3 compare match 3D signal	MTU3 compare match 3D signal
14h	MTU3 overflow signal	MTU3 overflow signal
15h	MTU4 compare match 4A signal	MTU4 compare match 4A signal
16h	MTU4 compare match 4B signal	MTU4 compare match 4B signal
17h	MTU4 compare match 4C signal	MTU4 compare match 4C signal
18h	MTU4 compare match 4D signal	MTU4 compare match 4D signal
19h	MTU4 overflow signal	MTU4 overflow signal
1Ah	MTU4 underflow signal	MTU4 underflow signal
1Fh	CMT1 compare match 1 signal	CMT1 compare match 1 signal
22h	TMR0 compare match A0 signal	TMR0 compare match A0 signal
23h	TMR0 compare match B0 signal	TMR0 compare match B0 signal
24h	TMR0 overflow signal	TMR0 overflow signal
28h	TMR2 compare match A2 signal	TMR2 compare match A2 signal
29h	TMR2 compare match B2 signal	TMR2 compare match B2 signal
2Ah	TMR2 overflow signal	TMR2 overflow signal
2Eh	RTC periodic signal	-
31h	IWDT underflow or refresh error signal	-
3Ah	SCI5 error (receive error or error signal detection) signal	SCI5 error (receive error or error signal detection) signal
3Bh	SCI5 receive data full signal	SCI5 receive data full signal
3Ch	SCI5 transmit data empty signal	SCI5 transmit data empty signal
3Dh	SCI5 transmit end signal	SCI5 transmit end signal
4Eh	RIIC0 communication error or event generation signal	RIIC0 communication error or event generation signal
4Fh	RIIC0 receive data full signal	RIIC0 receive data full signal
50h	RIIC0 transmit data empty signal	RIIC0 transmit data empty signal

Note:

1. For the RX210 Group, n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29.
   For the RX220 Group, n = 1 to 4, 10, 12, 15, 18, 20, 22, 24, 25.

Table 4.33 Comparison of the Event Signal Name Set in the ELSRn Register (1) and the Signal Numbers (2/2)

ELS[7:0] Bit Value	RX210	RX220
51h	RIIC0 transmit end signal	RIIC0 transmit end signal
52h	RSPI0 error (mode fault, overrun, or parity error) signal	RSPI0 error (mode fault, overrun, or parity error) signal
53h	RSPI0 idle signal	RSPI0 idle signal
54h	RSPI0 receive data full signal	RSPI0 receive data full signal
55h	RSPI0 transmit data empty signal	RSPI0 transmit data empty signal
56h	RSPI0 transmit end signal (except during clock synchronous operation in slave mode)	RSPI0 transmit end signal (except during clock synchronous operation in slave mode)
58h	A/D conversion end signal of 12-bit A/D converter	A/D conversion end signal of 12-bit A/D converter
59h	Comparator B0 comparison result change signal	-
5Ah	Comparator B0, B1 common comparison result change signal	-
5Bh	LVD1 voltage detection signal	LVD1 voltage detection signal
5Ch	LVD2 voltage detection signal	-
5Dh	DMAC0 transfer end signal	-
5Eh	DMAC1 transfer end signal	-
5Fh	DMAC2 transfer end signal	-
60h	DMAC3 transfer end signal	-
61h	DTC transfer end signal	DTC transfer end signal
62h	Oscillation stop detection signal of clock generation circuit	-
63h	Input edge detection signal of input port group 1	Input edge detection signal of input port group 1
64h	Input edge detection signal of input port group 2	-
65h	Input edge detection signal of single input port 0	Input edge detection signal of single input port 0
66h	Input edge detection signal of single input port 1	Input edge detection signal of single input port 1
67h	Input edge detection signal of single input port 2	-
68h	Input edge detection signal of single input port 3	-
69h	Software event signal	Software event signal
6Ah	-	DOC data operation condition met signal

Note:

1. For the RX210 Group, n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29.
   For the RX220 Group, n = 1 to 4, 10, 12, 15, 18, 20, 22, 24, 25.

4.13 Comparison of I/O Ports

Table 4.34 to Table 4.35 list a Comparison of . Table 4.36 lists a Comparison of I/O Registers Associated With I/O Ports.

Table 4.34 Comparison of Open Drain Output

Pin	RX210	RX220
P03, P05, P07	Not included	Not included
P12, P13, P16, P17	Included	Included
P14	Included	Not included
P15	Included	Included
P20 to P25	Included	Not included
P26, P27	Included	Included
P30, P32 to P34	Included	Included
P31, P36, P37	Included	Not included
P35	Not included	Not included
P40 to P47	Not included	Not included
P50 to P55	Not included	Not included
PA0	Included	Not included
PA1 to PA7	Included	Included
PB0, PB1, PB3, PB5 to PB7	Included	Included
PB2, PB4	Included	Not included
PC0 to PC7	Included	Included
PD0 to PD7	Not included	Not included
PE0 to PE2	Included	Included
PE3 to PE7	Included	Not included
PH0 to PH3	Not included	Not included
PJ1, PJ3	Not included	Not included

Table 4.35 Comparison of Driving Ability Switching

Pin	RX210	RX220
P03, P05, P07	Fixed to normal output	Fixed to normal output
P12, P13, P16, P17	Included	Included
P14	Included	Included
P15	Included	Included
P20 to P25	Included	Fixed to normal output
P26, P27	Included	Fixed to normal output
P30, P32 to P34	Included	Fixed to normal output
P31, P36, P37	Included	Fixed to normal output
P35	Not included	Not included
P40 to P47	Fixed to normal output	Fixed to normal output
P50 to P55	Included	Fixed to normal output
PA0	Included	Fixed to normal output
PA1 to PA7	Included	Fixed to normal output
PB0, PB1, PB3, PB5 to PB7	Included	Included
PB2, PB4	Included	Included
PC0 to PC7	Included	Included
PD0 to PD7	Included	Fixed to normal output
PE0 to PE2	Included	Fixed to normal output
PE3 to PE7	Included	Fixed to normal output
PH0 to PH3	Included	Fixed to normal output
PJ1, PJ3	Included	Fixed to normal output

Table 4.36 Comparison of I/O Registers Associated With I/O Ports

Register Symbol	Bit Symbol	RX210	RX220
ODR0	B2	P21, P31, PA1, PB1, PC1 0: CMOS Output 1: N-channel open-drain	PA1, PB1, PC1 0: CMOS Output 1: N-channel open-drain
PSRA	-	-	Port Switching Register A
PSRB	-	-	Port Switching Register B

4.14 Comparison of the MPC

Table 4.37 to Table 4.46 list a comparison of the allocation of pin functions to multiple pins. Note that pins with the "-DS" suffix can be used to initiate release from the RX210's deep software standby mode.

Table 4.37 Comparison of the Allocation of Pin Functions to Multiple Pins (1/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
Interrupt		NMI	P35	Present	Present
Interrupt	IRQ0	IRQ0-DS (input)	P30	Present	Present
		IRQ0 (input)	PD0	Present	Present
			PH1	Present	Present
	IRQ1	IRQ1-DS (input)	P31	Present	Present
		IRQ1 (input)	PD1	Present	Present
			PH2	Present	Present
	IRQ2	IRQ2-DS (input)	P32	Present	Present
		IRQ2 (input)	P12	Present	Present
			PD2	Present	Present
	IRQ3	IRQ3-DS (input)	P33	Present	Present
		IRQ3 (input)	P13	Present	Present
			PD3	Present	Present
	IRQ4	IRQ4-DS (input)	PB1	Present	Present
		IRQ4 (input)	P14	Present	Present
			P34	Present	Present
			PD4	Present	Present
	IRQ5	IRQ5-DS (input)	PA4	Present	Present
		IRQ5 (input)	P15	Present	Present
			PD5	Present	Present
			PE5	Present	Present
	IRQ6	IRQ6-DS (input)	PA3	Present	Present
		IRQ6 (input)	P16	Present	Present
			PD6	Present	Present
			PE6	Present	Present
	IRQ7	IRQ7-DS (input)	PE2	Present	Present
		IRQ7 (input)	P17	Present	Present
			PD7	Present	Present
			PE7	Present	Present

Table 4.38 Comparison of the Allocation of Pin Functions to Multiple Pins (2/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
MTU2	MTU0	MTIOC0A (I/O)	P34	Present	Present
			PB3	Present	Present
		MTIOC0B (I/O)	P13	Present	Present
			P15	Present	Present
			PA1	Present	Present
		MTIOC0C (I/O)	P32	Present	Present
			PB1	Present	Present
		MTIOC0D (I/O)	P33	Present	Present
			PA3	Present	Present
	MTU1	MTIOC1A (I/O)	P20	Present	Present
			PE4	Present	Present
		MTIOC1B (I/O)	P21	Present	Present
			PB5	Present	Present
	MTU2	MTIOC2A (I/O)	P26	Present	Present
			PB5	Present	Present
		MTIOC2B (I/O)	P27	Present	Present
			PE5	Present	Present
	MTU3	MTIOC3A (I/O)	P14	Present	Present
			P17	Present	Present
			PC1	Present	Present
			PC7	Present	Present
			PJ1	Present	Present
		MTIOC3B (I/O)	P17	Present	Present
			P22	Present	Present
			PB7	Present	Present
			PC5	Present	Present
		MTIOC3C (I/O)	P16	Present	Present
			PC0	Present	Present
			PC6	Present	Present
			PJ3	Present	Present
		MTIOC3D (I/O)	P16	Present	Present
			P23	Present	Present
			PB6	Present	Present
			PC4	Present	Present

Table 4.39 Comparison of the Allocation of Pin Functions to Multiple Pins (3/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
MTU2	MTU4	MTIOC4A (I/O)	P24	Present	Present
			PA0	Present	Present
			PB3	Present	Present
			PE2	Present	Present
		MTIOC4B (I/O)	P30	Present	Present
			P54	Present	Present
			PC2	Present	Present
			PD1	Present	Present
			PE3	Present	Present
		MTIOC4C (I/O)	P25	Present	Present
			PB1	Present	Present
			PE1	Present	Present
			PE5	Present	Present
		MTIOC4D (I/O)	P31	Present	Present
			P55	Present	Present
			PC3	Present	Present
			PD2	Present	Present
			PE4	Present	Present
	MTU5	MTIC5U (input)	PA4	Present	Present
			PD7	Present	Present
		MTIC5V (input)	PA6	Present	Present
			PD6	Present	Present
		MTIC5W (input)	PB0	Present	Present
			PD5	Present	Present
	MTU	MTCLKA (input)	P14	Present	Present
			P24	Present	Present
			PA4	Present	Present
			PC6	Present	Present
		MTCLKB (input)	P15	Present	Present
			P25	Present	Present
			PA6	Present	Present
			PC7	Present	Present
		MTCLKC (input)	P22	Present	Present
			PA1	Present	Present
			PC4	Present	Present
		MTCLKD (input)	P23	Present	Present
			PA3	Present	Present
			PC5	Present	Present

Table 4.40 Comparison of the Allocation of Pin Functions to Multiple Pins (4/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
MTU2	POE0	POE0# (input)	PC4	Present	Present
			PD7	Present	Present
	POE1	POE1# (input)	PB5	Present	Present
			PD6	Present	Present
	POE2	POE2# (input)	P34	Present	Present
			PA6	Present	Present
			PD5	Present	Present
	POE3	POE3# (input)	P33	Present	Present
			PB3	Present	Present
			PD4	Present	Present
	POE8	POE8# (input)	P17	Present	Present
			P30	Present	Present
			PD3	Present	Present
			PE3	Present	Present

Table 4.41 Comparison of the Allocation of Pin Functions to Multiple Pins (5/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
8-bit timer	TMR0	TMO0 (output)	P22	Present	Present
			PB3	Present	Present
			PH1	Present	Present
		TMCI0 (input)	P21	Present	Present
			PB1	Present	Present
			PH3	Present	Present
		TMRI0 (input)	P20	Present	Present
			PA4	Present	Present
			PH2	Present	Present
	TMR1	TMO1 (output)	P17	Present	Present
			P26	Present	Present
		TMCI1 (input)	P02	Present	Present
			P54	Present	Present
			PC4	Present	Present
		TMRI1 (input)	P24	Present	Present
			PB5	Present	Present
	TMR2	TMO2 (output)	P16	Present	Present
			PC7	Present	Present
		TMCI2 (input)	P15	Present	Present
			P31	Present	Present
			PC6	Present	Present
		TMRI2 (input)	P14	Present	Present
			PC5	Present	Present
	TMR3	TMO3 (output)	P13	Present	Present
			P32	Present	Present
			P55	Present	Present
		TMCI3 (input)	P27	Present	Present
			P34	Present	Present
		TMRI3 (input)	PA6	Present	Present
			P30	Present	Present
			P33	Present	Present

Table 4.42 Comparison of the Allocation of Pin Functions to Multiple Pins (6/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
SCI	SCI0	RXD0 (input)/SMISO0 (I/O)/SSCL0 (I/O)	P21	Present	Not present
		TXD0 (output)/SMOSI0 (I/O)/SSDA0 (I/O)	P20	Present	Not present
		SCK0 (I/O)	P22	Present	Not present
		CTS0# (input)/RTS0# (output)/SS0# (input)	P23	Present	Not present
	SCI1	RXD1 (input)/SMISO1 (I/O)/SSCL1 (I/O)	P15	Present	Present
			P30	Present	Present
		TXD1 (output)/SMOSI1 (I/O)/SSDA1 (I/O)	P16	Present	Present
			P26	Present	Present
		SCK1 (I/O)	P17	Present	Present
			P27	Present	Present
		CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	Present	Present
			P31	Present	Present
	SCI5	RXD5 (input)/SMISO5 (I/O)/SSCL5 (I/O)	PA2	Present	Present
			PA3	Present	Present
			PC2	Present	Present
		TXD5 (output)/SMOSI5 (I/O)/SSDA5 (I/O)	PA4	Present	Present
			PC3	Present	Present
		SCK5 (I/O)	PA1	Present	Present
			PC1	Present	Present
			PC4	Present	Present
		CTS5# (input)/RTS5# (output)/SS5# (input)	PA6	Present	Present
			PC0	Present	Present
	SCI6	RXD6 (input)/SMISO6 (I/O)/SSCL6 (I/O)	P33	Present	Present
			PB0	Present	Present
		TXD6 (output)/SMOSI6 (I/O)/SSDA6 (I/O)	P32	Present	Present
			PB0	Present	Present
		SCK6 (I/O)	P34	Present	Present
			PB3	Present	Present
		CTS6# (input)/RTS6# (output)/SS6# (input)	PB2	Present	Present
			PJ3	Present	Present

Table 4.43 Comparison of the Allocation of Pin Functions to Multiple Pins (7/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
SCI	SCI8	RXD8 (input)/SMISO8 (I/O)/SSCL8 (I/O)	PC6	Present	Not present
		TXD8 (output)/SMOSI8 (I/O)/SSDA8 (I/O)	PC7	Present	Not present
		SCK8 (I/O)	PC5	Present	Not present
		CTS8# (input)/RTS8# (output)/SS8# (input)	PC4	Present	Not present
	SCI9	RXD9 (input)/SMISO9 (I/O)/SSCL9 (I/O)	PB6	Present	Present
		TXD9 (output)/SMOSI9 (I/O)/SSDA9 (I/O)	PB7	Present	Present
		SCK9 (I/O)	PB5	Present	Present
		CTS9# (input)/RTS9# (output)/SS9# (input)	PB4	Present	Present
	SCI12	RXD12 (input)/SMISO12 (I/O)/ SSCL12 (I/O)/RXDX12 (input)	PE2	Present	Present
		TXD12 (output)/SMOSI12 (I/O)/SSDA12 (I/O)/ TXDX12 (output)/SIOX12 (I/O)	PE1	Present	Present
		SCK12 (I/O)	PE0	Present	Present
		CTS12# (input)/RTS12# (output)/SS12# (input)	PE3	Present	Present
IRDA		IRRXD5 (input)	PA2	Not present	Present
			PA3	Not present	Present
			PC2	Not present	Present
		IRTXD5 (output)	PA4	Not present	Present
			PC3	Not present	Present

Table 4.44 Comparison of the Allocation of Pin Functions to Multiple Pins (8/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
RIIC	RIIC0	SCL-DS (I/O)	P16	Present	Present
		SCL (I/O)	P12	Present	Present
		SDA-DS (I/O)	P17	Present	Present
		SDA (I/O)	P13	Present	Present
RSPI	RSPI0	RSPCKA (I/O)	PA5	Present	Present
			PB0	Present	Present
			PC5	Present	Present
		MOSIA (I/O)	P16	Present	Present
			PA6	Present	Present
			PC6	Present	Present
		MISOA (I/O)	P17	Present	Present
			PA7	Present	Present
			PC7	Present	Present
		SSLA0 (I/O)	PA4	Present	Present
			PC4	Present	Present
		SSLA1 (output)	PA0	Present	Present
			PC0	Present	Present
		SSLA2 (output)	PA1	Present	Present
			PC1	Present	Present
		SSLA3 (output)	PA2	Present	Present
			PC2	Present	Present
RTC		RTCOUT (output)	P16	Present	Present
			P32	Present	Present
		RTCIC0 (input)	P30	Present	Not present
		RTCIC1 (input)	P31	Present	Not present
		RTCIC2 (input)	P32	Present	Not present

Table 4.45 Comparison of the Allocation of Pin Functions to Multiple Pins (9/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
S12AD		AN000 (input)	P40	Present	Present
		AN001 (input)	P41	Present	Present
		AN002 (input)	P42	Present	Present
		AN003 (input)	P43	Present	Present
		AN004 (input)	P44	Present	Present
		AN005 (input)	P45	Present	Present
		AN006 (input)	P46	Present	Present
		AN007 (input)	P47	Present	Present
		AN008 (input)	PE0	Present	Present
		AN009 (input)	PE1	Present	Present
		AN010 (input)	PE2	Present	Present
		AN011 (input)	PE3	Present	Present
		AN012 (input)	PE4	Present	Present
		AN013 (input)	PE5	Present	Present
		AN014 (input)	PE6	Present	Present
		AN015 (input)	PE7	Present	Present
		ADTRG0# (input)	P07	Present	Present
			P16	Present	Present
			P25	Present	Present
DA		DA0 (output)	P03	Present	Not present
		DA1 (output)	P05	Present	Not present
CAC		CACREF (input)	PA0	Present	Present
			PC7	Present	Present
			PH0	Present	Present
CMPA		CMPA1 (input)	PE3	Present	Present
		CMPA2 (input)	PE4	Present	Present
		CVREFA (input)	PA1	Present	Present
CMPB		CMPB0 (input)	PE1	Present	Not present
		CVREFB0 (input)	PE2	Present	Not present
		CMPB1 (input)	PA3	Present	Not present
		CVREFB1 (input)	PA4	Present	Not present

Table 4.46 Comparison of the Allocation of Pin Functions to Multiple Pins (10/10)

Module/ Function	Channel	Pin Functions	Allocation Port	RX210	RX220
External bus		CS0# (output)	P24	Present	Not present
			PC7	Present	Not present
		CS1# (output)	P25	Present	Not present
			PC6	Present	Not present
		CS2# (output)	P26	Present	Not present
			PC5	Present	Not present
		CS3# (output)	P27	Present	Not present
			PC4	Present	Not present
		A0 to A7 (output)	PA0 to PA7	Present	Not present
		A8 to A15 (output)	PB0 to PB7	Present	Not present
		A16 to A23 (output)	PC0 to PC7	Present	Not present
		D0 to D7 (output)	PD0 to PD7	Present	Not present
		D8 to D15 (output)	PE0 to PE7	Present	Not present
		BCLK (output)	P53	Present	Not present
		RD# (output)	P52	Present	Not present
		WR# (output)	P50	Present	Not present
		WR0# (output)	P50	Present	Not present
		WR1# (output)	P51	Present	Not present
		BC0# (output)	PA0	Present	Not present
		BC1# (output)	P51	Present	Not present
		WAIT# (input)	P51	Present	Not present
			P55	Present	Not present
			PC5	Present	Not present
		ALE (output)	P54	Present	Not present

4.15 Comparison of POE2

Table 4.47 lists a Comparison of POE2.

Table 4.47 Comparison of POE2

Item	RX210	RX220
High-impedance is controlled by an event signal	Pins for complementary PWM output from the MTU and output pins for MTU0 can be placed in the high-impedance by an event signal from the ELC.	-

4.16 Comparison of the CMT

Table 4.48 lists a Comparison of the CMT.

Table 4.48 Comparison of the CMT

Item	RX210	RX220
Event link facilities (output)	An event signal is output upon a CMT1 compare match.	-
Event link facilities (input)	Linking to the specified module is possible. Count start, event count, or count restart is possible upon the specified event.	-

4.17 Comparison of the RTC

Table 4.49 lists a Comparison of the RTC. Table 4.50 lists a Comparison of I/O Registers Associated With the RTC.

Table 4.49 Comparison of the RTC

Item	RX210	RX220
Count mode	Calendar count mode	Calendar count mode, binary count mode
Time capture facility	Times when any of three event signals are input can be captured. The month, date, hour, minute, and second are captured for each event.	-
Event link function	Periodic event output	-

Table 4.50 Comparison of I/O Registers Associated With the RTC

Register Symbol	Bit Symbol	RX210	RX220
RCR2	RESET	In writing 0: Writing is invalid. 1: The prescaler and target registers are reset by RTC software reset. (R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RTCCRy, RSECCPy, RMINCPy, RHRCPy, RDAYCPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.RTCOE) In reading 0: In normal time operation, or RTC software reset has completed. 1: During a RTC software reset	In writing 0: Writing is invalid. 1: The prescaler and target registers are reset by RTC software reset. (R64CNT, RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR, RYRAREN, RADJ, RCR2.ADJ30, RCR2.AADJE, RCR2.RTCOE) In reading 0: In normal time operation, or RTC software reset has completed. 1: During a RTC software reset
	CNTMD	Reserved	Count Mode Select
RTCCRy	-	Time Capture Control Register y	
RSECCPy	-	Second Capture Register y	
RMINCPy	-	Minute Capture Register y	
RHRCPy	-	Hour Capture Register y	
RDAYCPy	-	Day Capture Register y	
ROMNCPy	-	Month Capture Register y	

4.18 Comparison of the WDTA

Table 4.51 lists a Comparison of the WDTA.

Table 4.51 Comparison of the WDTA

Item	RX210	RX220
Event link function (input)	● Down-counter underflows ● Refreshing outside the refresh-permitted period (refresh error)	-

4.19 Comparison of the SCI

Table 4.52 lists a Comparison of the SCI. Table 4.53 lists a Comparison of the I/O Register Associated With the SCI.

Table 4.52 Comparison of the SCI

Item	RX210	RX220
Detection of a start bit in asynchronous mode	Low level is selectable	Low level or falling edge is selectable

Table 4.53 Comparison of the I/O Register Associated With the SCI

Register Symbol	Bit Symbol	RX210	RX220
SEMR	RXDESEL	-	Asynchronous Start Bit Edge Detection Select

4.20 Comparison of the RSPI

Table 4.54 lists a Comparison of the RSPI.

Table 4.54 Comparison of the RSPI

Item	RX210	RX220
Maximum bit rate when PCLK is 32 MHz	● 16.0 Mbps is available for products with at least 768 Kbytes or products with at least 144 pins. ● 8.00 Mbps is available for products with less than 768 Kbytes or products with less than 144 pins.	16.0 Mbps

4.21 Comparison of the S12AD

Table 4.55 lists a Comparison of the S12AD. Table 4.56 lists a Comparison of I/O Registers Associated With the S12AD.

Table 4.55 Comparison of the S12AD

Item	RX210	RX220
Extended analog inputs	Temperature sensor output, internal reference voltage	Internal reference voltage
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 50 MHz)	1.56 µs per channel (when A/D conversion clock ADCLK = 32 MHz)
Conditions of A/D conversion start	● Software trigger ● Synchronous trigger: Trigger by MTU, ELC, or temperature sensor ● Asynchronous trigger: A/D conversion can be triggered from the ADTRG0# pin.	● Software trigger ● Synchronous trigger: Trigger by MTU or ELC ● Asynchronous trigger: A/D conversion can be triggered from the ADTRG0# pin.
Functions	● Sample-and-hold function ● Channel-dedicated sample-and-hold function ● Variable sampling state count ● Self-diagnosis of 12-bit A/D converter ● A/D-converted value addition mode ● Analog input disconnection detection assist ● Double trigger mode (duplication of A/D conversion data)	● Sample-and-hold function ● Variable sampling state count ● Self-diagnosis of 12-bit A/D converter ● A/D-converted value addition mode ● Analog input disconnection detection assist ● Double trigger mode (duplication of A/D conversion data)

Table 4.56 Comparison of I/O Registers Associated With the S12AD

Register Symbol	Bit Symbol	RX210	RX220
ADTSDR	-	A/D Temperature Sensor Data Register	-
ADCSDR	EXTRG	Trigger Select 0: A/D conversion is started by the synchronous trigger (MTU, ELC, or temperature sensor). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).	Trigger Select 0: A/D conversion is started by the synchronous trigger (MTU or ELC). 1: A/D conversion is started by the asynchronous trigger (ADTRG0#).
ADSHCR	-	A/D Sample and Hold Circuit Control Register	-
ADSTRGR	TRSA[3:0]	A/D Conversion Start Trigger Select ----: ADST 0000: ADTRG0# 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: ELC 1010: Temperature sensor	A/D Conversion Start Trigger Select ----: ADST 0000: ADTRG0# 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: ELC
ADEXICR	TSS	Temperature Sensor Output A/D Conversion Select	Reserved
ADSSTRO	-	A/D Sampling State Register O	-

4.22 Comparison of CMPA

Table 4.57 lists a Comparison of CMPA.

Table 4.57 Comparison of CMPA

Item	RX210	RX220
Event generation timing to ELC	Comparator A2 Input voltage to the CMPA2 pin has risen above or fallen below the CVREFA pin reference input voltage, or either of the two.	-
Comparison result output	Comparator A2 Comparison result can be output from a port by going through the ELC.	-

4.23 Comparison of the DOC

Table 4.58 lists a Comparison of the DOC.

Table 4.58 Comparison of the DOC

Item	RX210	RX220
Event link function (output)	-	● The condition selected by the DOCR.DCSEL bit being met ● The result of data addition being greater than FFFFh ● The result of data subtraction being less than 0000h

4.24 Comparison of the ROM

Table 4.59 lists a Comparison of the ROM. Table 4.60 lists a Comparison of I/O Registers Associated With the ROM.

Table 4.59 Comparison of the ROM

Item	RX210	RX220
Memory capacity	User area: 1 Mbyte max.	User area: 256 Kbytes max.
Off-board programming	A PROM programmer can be used to program the user area and user boot area.	-

Table 4.60 Comparison of I/O Registers Associated With the ROM

Register Symbol	Bit Symbol	RX210	RX220
FCURAME	-	FCU RAM Enable Register	-
FENTRYR	FENTRY1	ROM P/E Mode Entry 1	-

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.30 (R01UH0037EJ)

RX220 Group User's Manual: Hardware Rev.1.00 (R01UH0292EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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REVISION HISTORY	RX210 and RX220 Groups Comparison of the RX210 and RX220 Group MCUs

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 1, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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