RX111 Group, RX110 Group

Comparing the RX111 and RX110 Groups for 48-Pin Package

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Abstract

This application note is a reference document that compares the 48-pin package of the RX111 and RX110 Groups.

Products

RX111 Group and RX110 Group

Contents

1. Comparison of Functions

This chapter compares the functions incorporated in the RX111 and RX110 Groups.
For details of the functions, refer to 4. Detailed Comparison of the Specifications and 5. Reference Documents.

Table 1.1 lists the Modules Incorporated in the RX111 and RX110 Groups.

Table 1.1 Modules Incorporated in the RX111 and RX110 Groups

Function	RX111	RX110
Voltage detection circuit (LVDAa)	✓ (1)	✓
Clock frequency accuracy measurement circuit (CAC)	✓	✓
Low power consumption	✓	✓
Data transfer controller (DTCa)	✓ (1)	✓
Event link controller (ELC)	✓	—
Multi-function pin controller (MPC)	✓	✓
Multi-function timer pulse unit 2 (MTU2a: RX111)/(MTU2b: RX110)	♦ (1)	♦
Port output enable 2 (POE2a)	✓	—
Compare match timer (CMT)	✓ (1)	✓
Realtime clock (RTCA)	✓	✓
Independent watchdog timer (IWDTa)	✓	✓
USB 2.0 host/function module (USBc)	✓	—
Serial communications interface (SCIe,SCIf)	✓ (1)	✓
I^2C bus interface (RIIC)	✓ (1)	✓
Serial peripheral interface (RSPI)	✓	✓
CRC calculator (CRC)	✓	✓
12-bit A/D converter (S12ADb)	✓ (1)	✓
Temperature sensor (TEMPSa)	✓	✓
Data operation circuit (DOC)	✓ (1)	✓
E2 DataFlash (memory for data storage)	✓	—

✓: Incorporated, —: Not incorporated, ♦: Difference in the function version

Note:
1. The module has the functions to output events to or input events from the ELC.

2. Comparison of the Specification Overview

Table 2.1 and Table 2.2 list the Differences in the Specification Overview.

Table 2.1 Differences in the Specification Overview (1/2)

Item		RX111	RX110
CPU	Maximum operating frequency	32 MHz	32 MHz
Memory	ROM	16 KB, 32 KB, 64 KB, 96 KB, 128 KB	16 KB, 32 KB, 64 KB, 96 KB, 128 KB
	RAM	8 KB, 10 KB, 16 KB	8 KB, 10 KB, 16 KB
	E2 DataFlash	8 KB	—
MCU operating mode		Single-chip mode	Single-chip mode
Clock generation circuits		- Main clock oscillator - Sub-clock oscillator - Low-speed on-chip oscillator - High-speed on-chip oscillator - IWDT-dedicated on-chip oscillator - PLL frequency synthesizer	- Main clock oscillator - Sub-clock oscillator - Low-speed on-chip oscillator - High-speed on-chip oscillator - IWDT-dedicated on-chip oscillator
System clock (ICLK)		32 MHz (max.)	32 MHz (max.)
Peripheral module clock (PCLKB)		32 MHz (max.)	32 MHz (max.)
Peripheral module clock (PCLKD)		32 MHz (max.)	32 MHz (max.)
FlashIF clock (FCLK)		32 MHz (max.)	32 MHz (max.)
Resets		- RES# pin reset - Power-on reset - Voltage monitoring reset - Independent watchdog timer reset - Software reset	- RES# pin reset - Power-on reset - Voltage monitoring reset - Independent watchdog timer reset - Software reset
Low power consumption functions		- Sleep mode - Deep sleep mode - Software standby mode	- Sleep mode - Deep sleep mode - Software standby mode
Function for lower operating power consumption		- High-speed operating mode - Middle-speed operating mode - Low-speed operating mode	- High-speed operating mode - Middle-speed operating mode - Low-speed operating mode
Interrupt vectors		82	65
Non-maskable interrupts		- NMI pin - Voltage monitoring 1 interrupt - Voltage monitoring 2 interrupt - IWDT interrupt	- NMI pin - Voltage monitoring 1 interrupt - Voltage monitoring 2 interrupt - IWDT interrupt
General I/O ports		- I/O: 30 - Input: 2 - Pull-up resistor: 24 - Open-drain output: 24 - 5-V tolerance: 4	- I/O: 34 - Input: 2 - Pull-up resistor: 28 - Open-drain output: 24 - 5-V tolerance: 4
Event link controller (ELC)		Available	Not available

Red text: Difference in the function

Table 2.2 Differences in the Specification Overview (2/2)

Item	RX111	RX110
Multi-function timer pulse unit 2 (MTU2a: RX111) (MTU2b: RX110)	- 6 channels × 1 unit - Up to 16 lines of pulse input/output based on six 16-bit timer channels - Count clock: Selectable from eight or seven clocks (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four clocks are available. - Input capture function - 21 output compare/input capture registers - Pulse output mode - Complementary PWM output mode - Reset synchronous PWM mode - Phase-counting mode - Conversion start triggers for the A/D converter can be generated.	- 4 channels × 1 unit - Up to 8 lines of pulse input/output based on four 16-bit timer channels - Count clock: Selectable from eight or seven clocks (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four clocks are available. - Input capture function - 13 output compare/input capture registers - Pulse output mode - Phase-counting mode - Conversion start triggers for the A/D converter can be generated.
Port output enable 2 (POE2a)	Available	Not available
USB 2.0 host/function module (USBc)	Available	Not available
12-Bit A/D converter (S12ADb)	A/D conversion start conditions: - Software trigger - Trigger from a timer (MTU) - External trigger signal - ELC	A/D conversion start conditions: - Software trigger - Trigger from a timer (MTU) - External trigger signal
D/A converter (DA)	Available	Not available

Red text: Difference in the function

3. Comparison of Pin Functions

Table 3.1 and Table 3.2 list the Differences in Multi-Function Pins.

Table 3.1 Differences in Multi-Function Pins (1/2)

Port	RX111	RX110
P14	MTIOC0A, MTIOC3A, MTCLKA, CTS1#, RTS1#, SS1#, SSLA0, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, USB0_OVRCURA, IRQ4, UB#	MTIOC0A, MTCLKA, CTS1#, RTS1#, SS1#, SSLA0, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, IRQ4
P15	MTIOC0B, MTCLKB, RXD1, SMISO1, SSCL1, RSPCKA, IRQ5, CLKOUT	MTIOC0B, MTCLKB, RXD1, SMISO1, SSCL1, RSPCKA, IRQ5, CLKOUT
P16	MTIOC3C, MTIOC3D, RTCOUT, TXD1, SMOSI1, SSDA1, MOSIA, SCL0, USB0_VBUS, USB0_VBUSEN, USB0_OVRCURB, IRQ6, ADTRG0#	RTCOUT, TXD1, SMOSI1, SSDA1, MOSIA, SCL0, IRQ6, ADTRG0#
P17	MTIOC0C, MTIOC3A, MTIOC3B, POE8#, SCK1, MISOA, SDA0, RXD12, RXDX12, SMISO12, SSCL12, IRQ7	MTIOC0C, SCK1, MISOA, SDA0, RXD12, RXDX12, SMISO12, SSCL12, IRQ7
P26	MTIOC2A, TXD1, SMOSI1, SSDA1, USB0_VBUSEN	MTIOC2A, TXD1, SMOSI1, SSDA1
P27	MTIOC2B, SCK1, SCK12, IRQ3, CMPA2, CACREF, ADTRG0#	MTIOC2B, SCK1, SCK12, IRQ3, CMPA2, CACREF, ADTRG0#
P35	NMI, UPSEL	NMI
P40	AN000	AN000
P41	AN001	AN001
P42	AN002	AN002
P46	AN006	AN006
PA1	MTIOC0B, MTCLKC, RTCOUT, SCK5, SSLA2	MTIOC0B, MTCLKC, RTCOUT, SCK5, SSLA2
PA3	MTIOC0D, MTCLKD, MTIOC1B, POE0#, RXD5, SMISO5, SSCL5, MISOA, IRQ6	MTIOC0D, MTCLKD, MTIOC1B, RXD5, SMISO5, SSCL5, MISOA, IRQ6
PA4	MTIC5U, MTCLKA, MTIOC2B, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5	MTIC5U, MTCLKA, MTIOC2B, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5
PA6	MTIC5V, MTCLKB, MTIOC2A, POE2#, CTS5#, RTS5#, SS5#, SDA0, MOSIA, IRQ3	MTIC5V, MTCLKB, MTIOC2A, CTS5#, RTS5#, SS5#, SDA0, MOSIA, IRQ3
PB0/PC0	MTIC5W, MTIOC0C, RTCOUT, SCL0, RSPCKA, IRQ2, ADTRG0#	MTIC5W, MTIOC0C, RTCOUT, SCL0, RSPCKA, IRQ2, ADTRG0#

Red Text: Difference between the Groups

Table 3.2 Differences in Multi-Function (2/2)

Port	RX111	RX110
PB1/PC1	MTIOC0C, MTIOC4C, IRQ4	MTIOC0C, IRQ4
PB3/PC2	MTIOC0A, MTIOC3B, MTIOC4A, POE3#, USB0_OVRCURA	MTIOC0A
PB5/PC3	MTIOC2A, MTIOC1B, POE1#	MTIOC2A, MTIOC1B
PC4	MTIOC3D, MTCLKC, POE0#, SCK5, SSLA0, USB0_VBUS, USB0_VBUSEN, IRQ2, CLKOUT	MTCLKC, SCK5, SSLA0, IRQ2, CLKOUT
PC5	MTIOC3B, MTCLKD, SCK1, RSPCKA, USB0_ID	MTCLKD, SCK1, RSPCKA
PC6	MTIOC3C, MTCLKA, RXD1, SMISO1, SSCL1, MOSIA, USB0_EXICEN	MTCLKA, RXD1, SMISO1, SSCL1, MOSIA
PC7	MTIOC3A, MTCLKB, TXD1, SMOSI1, SSDA1, MISOA, USB0_OVRCURB, CACREF	MTCLKB, TXD1, SMOSI1, SSDA1, MISOA, CACREF
PE0	MTIOC2A, POE3#, SCK12, IRQ0, AN008	MTIOC2A, SCK12, IRQ0, AN008
PE1	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, IRQ1, AN009	TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, IRQ1, AN009
PE2	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN010	RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN010
PE3	MTIOC0A, MTIOC1B, MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, RSPCKA, IRQ3, AN011	MTIOC0A, MTIOC1B, CTS12#, RTS12#, SS12#, RSPCKA, IRQ3, AN011
PE4	MTIOC4D, MTIOC1A, MTIOC3A, MOSIA, IRQ4, AN012	MTIOC1A, MOSIA, IRQ4, AN012
PE7	IRQ7, AN015	IRQ7, AN015
PH0	Note 1	MTIOC1B, CACREF
PH1	Note 1	IRQ0
PH2	Note 1	IRQ1
PH3	Note 1	MTIOC1A
PH7	XCIN	XCIN
PJ6	VREFH0	VREFH0
PJ7	VREFL0	VREFL0

Red Text: Difference between the Groups

Note:

1. No pin is assigned to the port.

4. Detailed Comparison of the Specifications

This chapter describes the differences between the MCU Groups using the following expressions.

- Red text: There is a difference in the function between Groups.
- —: The MCU Group does not have the function/register.
- Reserved: The MCU Group does not have the bit.

Note if the table has its own legend underneath, the legend is prioritized.

4.1 Operating Mode

Table 4.1 lists the Difference in the Operating Mode.

Table 4.1 Difference in the Operating Mode

Item	RX111	RX110

Operating modes	- Single-chip mode
	- Boot mode:
	  - SCI interface mode
	  - USB interface mode
		- Single-chip mode
		- Boot mode:
		  - SCI interface mode

4.2 Clock Generation Circuit

Table 4.2 lists the Differences in the Clock Generation Circuit and Table 4.3 lists the Differences in I/O Registers Related to the Clock Generation Circuit.

Table 4.2 Differences in the Clock Generation Circuit

Item	RX111	RX110
Functions	- Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. - Generates the peripheral module clocks (PCLKB and PCLKD) to be supplied to peripheral modules. - Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. - Generates the CAC clock (CACCLK) to be supplied to the CAC. - Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. - Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. - Generates the USB clock (UCLK) to be supplied to the USB.	- Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. - Generates the peripheral module clocks (PCLKB and PCLKD) to be supplied to peripheral modules. - Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. - Generates the CAC clock (CACCLK) to be supplied to the CAC. - Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. - Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequencies	- ICLK: 32 MHz (max.) - PCLKB: 32 MHz (max.) - PCLKD: 32 MHz (max.) - FCLK: - 1 to 32 MHz (when programming and erasing the ROM and E2 DataFlash) - 32 MHz (max.) (when reading from the E2 DataFlash) - UCLK: 48 MHz - CACCLK: Same frequency as each oscillator - RTCSCLK: 32.768 kHz - IWDTCLK: 15 kHz	- ICLK: 32 MHz (max.) - PCLKB: 32 MHz (max.) - PCLKD: 32 MHz (max.) - FCLK: - 1 to 32 MHz (when programming and erasing the ROM) - CACCLK: Same frequency as each oscillator - RTCSCLK: 32.768 kHz - IWDTCLK: 15 kHz
PLL circuit	- Input clock source: Main clock - Input pulse frequency division ratio: Selectable from 1, 2, and 4 - Input frequency: 4 to 8 MHz - Frequency multiplication ratio: Selectable from 6 and 8 - VCO oscillation frequency: 32 to 48 MHz (VCC ≥ 2.4 V)	—

Table 4.3 Differences in I/O Registers Related to the Clock Generation Circuit

Register Symbol	Bit Symbol	RX111	RX110
SCKCR3	CKSEL[2:0]	Clock Source Select bit 000: LOCO 001: HOCO 010: Main clock oscillator 011: Sub-clock oscillator 100: PLL circuit Do not set other than above.	Clock Source Select bit 000: LOCO 001: HOCO 010: Main clock oscillator 011: Sub-clock oscillator Do not set other than above.
PLLCR	—	PLL control register	—
PLLCR2	—	PLL control register 2	—
OSCOVFSR	PLOVF	PLL clock oscillation stabilization flag	Reserved

4.3 Low Power Consumption Function

Table 4.4 lists the Differences in I/O Registers Related to the Low Power Consumption Function.

Table 4.4 Differences in I/O Registers Related to the Low Power Consumption Function

Register Symbol	Bit Symbol	RX111	RX110
MSTPCRB	MSTPB9	ELC module stop bit	Reserved
	MSTPB19	USB0 module stop bit	Reserved

4.4 Register Write Protection Function

Table 4.5 lists the Difference in the Register Write Protection Function.

Table 4.5 Difference in the Register Write Protection Function

Item	RX111	RX110
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, PLLCR, PLLCR2	Registers related to the clock generation circuit: SCKCR, SCKCR3, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR

4.5 Buses

Table 4.6 lists the Differences in Buses.

Table 4.6 Differences in Buses

Item	RX111	RX110
Internal peripheral bus 3	- Connected to peripheral modules (USB) - Operates in synchronization with the peripheral module clock (PCLKB)	—
Internal peripheral bus 6	- Connected to ROM (when programming /erasing) and E2 DataFlash - Operates in synchronization with the FlashIF clock (FCLK)	- Connected to ROM (when programming /erasing) - Operates in synchronization with the FlashIF clock (FCLK)

4.6 I/O Ports

Table 4.7 to Table 4.9 list the differences in I/O Ports. Table 4.10 lists the Differences in I/O Registers Related to the I/O Ports.

The RX111 Group does not have PH0 to PH3 listed in Table 4.7 and Table 4.8.

Table 4.7 Difference in I/O Ports

Item	Port	RX111	RX110
General I/O ports	PH0 to PH3	—	✓

Table 4.8 Difference in Input Pull-Up

Item	Port	RX111	RX110
Input pull-up	PH0 to PH3	—	✓

Table 4.9 Differences in Values Set to Reserved Bits in the PDR Registers

Port (1)	RX111								RX110							
	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
PORT0	1	1	1	1	1	1	1	1	0	0	1	0	1	0	0	0
PORT1					1	1	1	1					0	0	0	0
PORT2			1	1	1	1	1	1			0	0	0	0	0	0
PORT3	1	1	0	1	1	1	1	1	0	0	0	0	0	1	1	1
PORT4	1		1	1	1				0		0	1	1			
PORT5	1	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0
PORTA	1		1			1		1	0		0			0		1
PORTB	1	1		1		1			1	1		0		0		
PORTC																
PORTE		1	1							1	1					
PORTH	—								0	0	0	0				
PORTJ			1	1	1	1	1	1			0	0	0	0	0	0

Note:
1. Blank columns indicate I/O ports whose settings are effective.

Table 4.10 Differences in I/O Registers Related to the I/O Ports

Register Symbol	Bit Symbol	RX111	RX110
PORTH.PDR	—	—	PORTH port direction register
PORTH.PODR	—	—	PORTH port output data register
PORTH.PCR	—	—	PORTH pull-up control register

4.7 Multi-Function Pin Controller

Table 4.11 and Table 4.12 list the Differences in Pin Functions and Their Assigned Ports.

Table 4.11 Differences in Pin Functions and Their Assigned Ports (1/2)

Module/Function	Channel	Pin Function	Assigned Port	RX111	RX110
Interrupt	IRQ0	IRQ0 (input)	PE0	✓	✓
			PH1	—	✓
	IRQ1	IRQ1 (input)	PE1	✓	✓
			PH2	—	✓
Multi-function timer pulse unit 2	MTU1	MTIOC1A (I/O)	PE4	✓	✓
			PH3	—	✓
		MTIOC1B (I/O)	PA3	✓	✓
			PB5/PC3	✓	✓
			PE3	✓	✓
			PH0	—	✓
	MTU3	MTIOC3A (I/O)	P14	✓	×
			P17	✓	×
			PC7	✓	×
			PE4	✓	×
		MTIOC3B (I/O)	P17	✓	×
			PB3/PC2	✓	×
			PC5	✓	×
		MTIOC3C (I/O)	P16	✓	×
			PC6	✓	×
		MTIOC3D (I/O)	P16	✓	×
			PC4	✓	×
	MTU4	MTIOC4A (I/O)	PB3	✓	×
			PE2	✓	×
		MTIOC4B (I/O)	PE3	✓	×
		MTIOC4C (I/O)	PB1	✓	×
			PE1	✓	×
		MTIOC4D (I/O)	PE4	✓	×
Port Output Enable 2	POE0	POE0# (input)	PC4	✓	×
			PA3	✓	×
	POE1	POE1# (input)	PB5/PC3	✓	×
	POE2	POE2# (input)	PA6	✓	×
	POE3	POE3# (input)	PB3/PC2	✓	×
			PE0	✓	×
	POE8	POE8# (input)	P17	✓	×
			PE3	✓	×

✓: Pin is assigned, ×: No pin is assigned, —: No pin exists

Table 4.12 Differences in Assigned Ports to Pin Functions (2/2)

Module/Function	Channel	Pin Function	Assigned Port	RX111	RX110
USB 2.0 Host/Function Module	USB0	USB0_EXICEN (output)	PC6	✓	×
		USB0_VBUSEN (output)	P16	✓	×
			PC4	✓	×
			P26	✓	×
		USB0_OVRCURA (input)	P14	✓	×
			PB3/PC2	✓	×
		USB0_OVRCURB (input)	P16	✓	×
			PC7	✓	×
		USB0_ID (input)	PC5	✓	×
		USB0_VBUS (input) (1)	P16	✓	×
		USB0_VBUS (input) (2)	PC4	✓	×
Clock frequency accuracy measurement circuit		CACREF (input)	P27	✓	✓
			PC7	✓	✓
			PH0	—	✓

✓: Pin is assigned, ×: No pin is assigned, —: No pin exists

Notes:
1. 5 V tolerant supported.
2. 5 V tolerant not supported.

Table 4.13 Differences in I/O Registers Related to the Multi-Function Pin Controller

Register Symbol	Bit Symbol	RX111	RX110
PHn.PFS (n = 0 to 3)	—	—	PHn Pin Function Control Register

4.8 Multi-Function Timer Pulse Unit 2

Table 4.14 lists the Differences in the Multi-Function Timer Pulse Unit 2 and Table 4.15 to Table 4.17 list the Differences in I/O Registers Related to the Multi-Function Timer Pulse Unit 2.

Table 4.14 Differences in the Multi-Function Timer Pulse Unit 2

Item	RX111	RX110
Pulse input/output	16 lines (max.)	8 lines (max.)
Available operations	MTU3 and MTU4 - Buffer operation can be specified. - AC synchronous motor (brushless DC motor) drive mode with complementary PWM output/reset-synchronized PWM output can be set, and the two types of waveform output (chopping and level) can be selected. - With interlocking operation, a total of six-phase waveform which are three phases each for positive and negative complementary PWM or reset PWM can be output.	—
	MTU5 - Dead time compensation counter - Input capture function (noise filter can be set) - Counter clear operation	MTU5 - Input capture function (noise filter can be set) - Counter clear operation
Complementary PWM mode	MTU3 and MTU4 - Interrupts at the crest and trough of the counter value - A/D converter start triggers can be skipped.	—
Interrupt sources	28 sources	18 sources
A/D converter start request delaying function	MTU4 A/D converter start is requested at a match between TADCORA and TCNT or at a match between TADCORB and TCNT.	—
Interrupt skipping function	MTU3 Skips TGRA compare match interrupts. MTU4 Skips TCIV interrupts.	—

Table 4.15 Differences in I/O Registers Related to the Multi-Function Timer Pulse Unit 2 (1/3)

Register Symbol	Bit Symbol	RX111	RX110
TMDR	MD[3:0]	Mode Select bit 0000: Normal mode 0001: Do not set. 0010: PWM mode 1 0011: PWM mode 2 0100: Phase counting mode 1 0101: Phase counting mode 2 0110: Phase counting mode 3 0111: Phase counting mode 4 1000: Reset-synchronized PWM mode 1001: Do not set. 101x: Do not set. 1100: Do not set. 1101: Complementary PWM mode 1 (transfer at crest) 1110: Complementary PWM mode 2 (transfer at trough) 1111: Complementary PWM mode 3 (transfer at crest and trough) x: Don't care	Mode Select bit 0000: Normal mode 0001: Do not set. 0010: PWM mode 1 0011: PWM mode 2 0100: Phase counting mode 1 0101: Phase counting mode 2 0110: Phase counting mode 3 0111: Phase counting mode 4 1000: Do not set. 1001: Do not set. 101x: Do not set. 1100: Do not set. 1101: Do not set. 1110: Do not set. 1111: Do not set. x: Don't care
TIORU TIORV TIORW	IOC[4:0]	I/O Control C bit 00000: Compare match 00001: Do not set. 0001x: Do not set. 001xx: Do not set. 01xxx: Do not set. 10000: Do not set. 10001: Input capture at rising edge. 10010: Input capture at falling edge. 10011: Input capture at both edges. 101xx: Do not set. 11000: Do not set. 11001, 11010, 11011: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 11100: Do not set. 11101, 11110, 11111: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. x: Don't care	I/O Control C bit 00000: Compare match 00001: Do not set. 0001x: Do not set. 001xx: Do not set. 01xxx: Do not set. 10000: Do not set. 10001: Input capture at rising edge. 10010: Input capture at falling edge. 10011: Input capture at both edges. 101xx: Do not set. 11000: Do not set. 11001, 11010, 11011: Measurement of low pulse width of external input signal. 11100: Do not set. 11101, 11110, 11111: Measurement of high pulse width of external input signal. x: Don't care

Table 4.16 Differences in I/O Registers Related to the Multi-Function Timer Pulse Unit 2 (2/3)

Register Symbol	Bit Symbol	RX111	RX110
TIER	TTGE2	A/D converter start request enable 2 bit 0: A/D converter start request generation by MTU4.TCNT underflow (trough) disabled 1: A/D converter start request generation by MTU4.TCNT underflow (trough) enabled	Reserved
TADCR	—	Timer A/D converter start request control register	—
TADCORA	—	Timer A/D converter start request cycle set register A	—
TADCORB	—	Timer A/D converter start request cycle set register B	—
TADCOBRA	—	Timer A/D converter start request cycle set buffer register A	—
TADCOBRB	—	Timer A/D converter start request cycle set buffer register B	—
TSTR (MTU0 to MTU4)	CST3	Counter start 3 bit 0: MTU3.TCNT performs count stop. 1: MTU3.TCNT performs count operation.	Reserved
	CST4	Counter start 4 bit 0: MTU4.TCNT performs count stop. 1: MTU4.TCNT performs count operation.	Reserved
TSYR	SYNC3	Timer synchronous operation 3 bit 0: MTU3.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU3.TCNT performs synchronous operation. TCNT synchronous presetting/synchronous clearing is enabled.	Reserved
	SYNC4	Timer synchronous operation 4 bit 0: MTU4.TCNT operates independently (TCNT presetting/clearing is not related to other channels). 1: MTU4.TCNT performs synchronous operation. TCNT synchronous presetting/synchronous clearing is enabled.	Reserved
TRWER	—	Timer read/write enable registers	—
TOER	—	Timer output master enable registers	—
TOCR1	—	Timer output control registers 1	—
TOCR2	—	Timer output control registers 2	—
TOLBR	—	Timer output level buffer registers	—
TGCR	—	Timer gate control registers	—

Table 4.17 Differences in I/O Registers Related to the Multi-Function Timer Pulse Unit 2 (3/3)

Register Symbol	Bit Symbol	RX111	RX110
TCNTS	—	Timer subcounters	—
TDDR	—	Timer dead time data registers	—
TCDR	—	Timer cycle data registers	—
TCBR	—	Timer cycle buffer registers	—
TITCR	—	Timer interrupt skipping set registers	—
TITCNT	—	Timer interrupt skipping counters	—
TBTER	—	Timer buffer transfer set registers	—
TDER	—	Timer dead time enable registers	—
TWCR	—	Timer waveform control registers	—

4.9 12-Bit A/D Converter

Table 4.18 lists the Differences in I/O Registers Related to the 12-Bit A/D Converter.

Table 4.18 Differences in I/O Registers Related to the 12-Bit A/D Converter

Register Symbol	Bit Symbol	RX111	RX110
ADSTRGR	TRSA[3:0]	A/D conversion start trigger select bit 0000: ADTRG0# 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: ELC	A/D conversion start trigger select bit 0000: ADTRG0# 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN
	TRSB[3:0]	A/D conversion start trigger select bit 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN 0110: TRG4AN 0111: TRG4BN 1000: TRG4ABN 1001: ELC	A/D conversion start trigger select bit 0001: TRG0AN 0010: TRG0BN 0011: TRGAN 0100: TRG0EN 0101: TRG0FN

4.10 Flash Memory

Table 4.19 lists the Differences in the Flash Memory and Table 4.20 lists the Difference in I/O Registers Related to the Flash Memory.

Table 4.19 Differences in the Flash Memory

Item	RX111	RX110
Memory space	- User area: 128 KB (max.) - Data area: 8 KB	- User area: 128 KB (max.)
On-board programming	SCI mode in boot mode - Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. - The user area and data area are rewritable. USB interface mode in boot mode - Channel 0 of the USB 2.0 function (USB0) module is used. - The user area and data area are rewritable. - The flash memory can be rewritable in self-powered or bus-powered mode. - A personal computer can be connected using only a USB cable. Self-programming in single-chip mode - The user area and data area are rewritable using the self-programming library.	SCI mode in boot mode - Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. - The user area is rewritable. Self-programming in single-chip mode - The user area is rewritable using the self-programming library.
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with this MCU.	The user area is rewritable using a flash programmer compatible with this MCU.
Background Operation (BGO)	Programs on the ROM can be executed while rewriting the E2 DataFlash.	—

Table 4.20 Difference in I/O Registers Related to the Flash Memory

Register Symbol	Bit Symbol	RX111	RX110
DFLCTL	—	E2 DataFlash control register	—

5. Reference Documents

User's Manual: Hardware

RX111 Group User's Manual: Hardware Rev.1.10 (R01UH0365EJ)
RX110 Group User's Manual: Hardware Rev.1.00 (R01UH0421EJ)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RX111 Group, RX110 Group Application Note Comparing the RX111 and RX110 Groups for 48-Pin Package

Rev.	Date	Description	
		Page	Summary
1.00	July 1, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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