RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RG

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Introduction

This document describes how to migrate from timer RG in R8C/36M Group to timer RG in RL78/G14 (This document describes the 64-pin package product as an example).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (timer mode (input capture function and output compare function), PWM mode and phase counting mode) in timer RG of R8C/36M using RL78/G14.
Table 1.1 shows the mode in timer RG of R8C/36M Group, and Table 1.2 shows the mode in timer RG of RL78/G14.

Timer RG is a 16-bit timer and supports three modes: timer mode (input capture function and output compare function), PWM mode and phase counting mode.

In timer mode (input capture function), the value of the TRG register can be transferred to registers TRGGRA and TRGGRB upon detecting the input edge (the rising edge/falling edge/both the rising and falling edges) of the input capture/output compare pins (TRGIOA and TRGIOB).
In timer mode (output compare function), when a compare match of the TRG register and the TRGGRA or TRGGRB register occurs, a signal is output from the TRGIOA or TRGIOB pin at a given level ("L" output/"H" output/toggle output).

In PWM mode, registers TRGGRA and TRGGRB are used as a pair and a PWM waveform is output from the TRGIOA output pin. By setting the compare match with either the TRGGRA or TRGGRB register as the counter clear source for the TRG register, a PWM waveform with duty 0% to 100% can be output from the TRGIOA pin.

In phase counting mode, automatic measurement is available for the counts of the two-phase encoder. A phase difference between external input signals from two pins TRGCLKA and TRGCLKB is detected and the TRG register is incremented/decremented.

Timer RG in R8C/36M and timer RG in RL78/G14 have the same operation mode, so the migration is possible.

About the detailed differences of timer RG, please refer to "2. Differences between RL78/G14 and R8C/36M Group" in this application note.

Additionally, for the sample programs of "timer mode (input capture function)" and "timer mode (output compare function)", please refer to "5. Example of Migration from Timer Mode (Input Capture Function)" ~ "6. Example of Migration from Timer Mode (Output Compare Function)".

For the sample programs of "PWM mode" and "phase counting mode", please refer to the application notes that are introduced in "8. Reference Application Notes".

Table 1.1 Operation Mode of Timer RG in R8C/36M

Timer RG in R8C/36M		
Mode		**Function**
Timer mode	- Input capture function	Count at the rising edge, falling edge, or both rising/falling edges
	- Output compare function	"L" output / "H" output / toggle output
PWM mode		PWM output available with any duty
Phase counting mode		Automatic measurement available for the counts of the two-phase encoder

Table 1.2 Corresponding Mode of Timer RG in RL78/G14

Timer RG in RL78/G14		
Mode		**Function**
Timer mode	- Input capture function	Count at the rising edge, falling edge, or both rising/falling edges
	- Output compare function	Low output / high output / toggle output
PWM mode		PWM output available with any duty cycle
Phase counting mode		Automatic measurement available for the counts of the two-phase encoder

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Function Overview

Table 2.1 lists the differences between timer RG in R8C/36M Group and timer RG in RL78/G14.

Table 2.1 Differences

Item	R8C/36M Group Timer RG	RL78/G14 Timer RG
Count source	• f1 • f2 • f4 • f8 • f32 • fOCO40M • TRGCLKA • TRGCLKB	• f_{CLK} • $f_{CLK}/2$ • $f_{CLK}/4$ • $f_{CLK}/8$ • $f_{CLK}/32$ • TRGCLKA • TRGCLKB
Timer RG pins	P3_0, P3_2, P5_6, P5_7 Note	P00, P01, P50, P51 Note
Event input signal from event link controller (ELC)	No	Yes

Note: For details, refer to Table 2.7.

2.2 Differences in Timer Mode (Input Capture Function)

The operation of timer mode (input capture function) in timer RG in R8C/36M Group corresponds to timer mode (input capture function) in timer RG in RL78/G14.
Table 2.2 lists the differences between timer mode (input capture function) in timer RG of R8C/36M Group and timer mode (input capture function) in timer RG in RL78/G14.

Table 2.2 Differences between Timer RG (Timer Mode (Input Capture Function))

Item	R8C/36M Group (Timer mode (Input Capture Function))	RL78/G14 (Timer mode (Input Capture Function))
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (valid edge selectable by a program)	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRGCLKA or TRGCLKB pin (valid edge selectable by a program)
Count operation	Increment	Increment
Count period	When bits CCLR1 to CCLR0 in the TRGCR register are set to 00b (free - running operation) 1/fk × 65,536 fk: Frequency of count source	When bits TRGCCLR1 to TRGCCLR0 in the TRGCR register are set to 00B (free - running operation) 1/fk × 65,536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.	1 (count starts) is written to the TRGSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.	0 (count stops) is written to the TRGSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (valid edge of the TRGIOj input) • TRG register overflow	• Input capture (valid edge of the TRGIOA and TRGIOB pin input) • TRG register overflow
TRGIOA, TRGIOB pin functions	Programmable I/O port or input - capture input (selectable for each individual pin)	I/O port or input - capture input (selectable for each pin)
TRGCLKA, TRGCLKB pin functions	Programmable I/O port or external clock input	I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.	The TRG register can be written to.
Selectable functions	• Input-capture input pin selection Either one or both of pins TRGIOA and TRGIOB • Valid edge selection for input-capture input Rising edge, falling edge, or both rising and falling edges • Timing for setting the TRG register to 0000h At overflow or input capture • Buffer operation • Digital filter	• Input-capture input pin selection Either one or both of pins TRGIOA and TRGIOB • Valid edge selection for input-capture input Rising edge, falling edge, or both rising and falling edges • Timing for setting the TRG register to 0000H At overflow or input capture • Buffer operation • Digital filter • Input capture operation by event input signal (input capture) from ELC

Remark: j = A or B

2.3 Differences in Timer Mode (Output Compare Function)

The operation of timer mode (output compare function) in timer RG in R8C/36M Group corresponds to timer mode (output compare function) in timer RG in RL78/G14.
Table 2.3 and Table 2.4 list the differences between timer mode (output compare function) in timer RG in R8C/36M Group and timer mode (output compare function) in timer RG in RL78/G14.

Table 2.3 Differences between Timer RG (Timer Mode (Output Compare Function)) (1/2)

Item	R8C/36M Group (Timer mode (Output Compare Function))	RL78/G14 (Timer mode (Output Compare Function))
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (valid edge selected by a program)	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRGCLKj pin (valid edge selected by a program)
Count operation	Increment	Increment
Count periods	• When bits CCLR1 to CCLR0 in the TRGCR register are set to 00b (free-running operation) 1/fk × 65,536 fk: Frequency of count source • When bits CCLR1 to CCLR0 in the TRGCR register are set to 01b or 10b (TRG is set to 0000h by the compare match with TRGGRj) 1/fk × (n+1) n: Value set in the TRGGRj register	• When bits TRGCCLR1 and TRGCCLR0 in the TRGCR register are set to 00B (free-running operation) 1/fk × 65,536 fk: Frequency of count source • When bits TRGCCLR1 and TRGCCLR0 in the TRGCR register are set to 01B or 10B (TRG is set to 0000H by the compare match with TRGGRj) 1/fk × (n + 1) n: Value set in the TRGGRj register
Waveform output timing	Compare match	Compare match (the content of the TRG register matches the content of the TRGGRj register)
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.	1 (count starts) is written to the TRGSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.	0 (count stops) is written to the TRGSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the content of the TRG register matches the content of the TRGGRj register) • TRG register overflows	• Compare match (the contents of TRG register matches TRGGRj register) • TRG register overflows
TRGIOA, TRGIOB pin functions	Programmable I/O port or output-compare output (selectable for each individual pin)	I/O port or output-compare output (selectable for each pin)
TRGCLKA, TRGCLKB pin functions	Programmable I/O port or external clock input	I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.	The TRG register can be written to.

Remark: j = A or B

Table 2.4 Differences between Timer RG (Timer Mode (Output Compare Function)) (2/2)

Item	R8C/36M Group (Timer mode (Output Compare Function))	RL78/G14 (Timer mode (Output Compare Function))
Selectable functions	• Output-compare output pin selection Either one or both of pins TRGIOA and TRGIOB • Output level selection at compare match "L" output, "H" output, or inverted output level • Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation	• Output-compare output pin selection Either one or both of pins TRGIOA and TRGIOB • Output level selection at compare match Low output, high output, or inverted output level • Timing for setting the TRG register to 0000H Overflow or compare match with the TRGGRj register • Buffer operation

Remark: j = A or B

2.4 Differences in PWM Mode

The operation of PWM mode in timer RG in R8C/36M Group corresponds to PWM mode in timer RG in RL78/G14. Table 2.5 lists the differences between PWM mode in timer RG in R8C/36M Group and PWM mode in timer RG in RL78/G14.

Table 2.5 Differences between Timer RG (PWM Mode)

Item	R8C/36M Group (PWM Mode)	RL78/G14 (PWM Mode)
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (valid edge selected by a program)	f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/32$ External signal input to the TRGCLKj pin (valid edge selected by a program)
Count operation	Increment	Increment
PWM waveform	• The "H" output timing of a PWM waveform is set into the TRGGRA register. • The "L" output timing of a PWM waveform is set into the TRGGRB register.	• The high output timing of a PWM waveform is set into the TRGGRA register. • The low output timing of a PWM waveform is set into the TRGGRB register.
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.	1 (count starts) is written to the TRGSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.	0 (count stops) is written to the TRGSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the content of the TRG register matches the content of the TRGGRj register) • TRG register overflows	• Compare match (the content of TRG register matches the content of TRGGRj register) • TRG register overflows
TRGIOA pin function	PWM output	PWM output
TRGIOB pin function	Programmable I/O port	I/O port
TRGCLKA, TRGCLKB pin functions	Programmable I/O port or external clock input	I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.	The TRG register can be written to.
Selectable functions	• Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation	• Timing for setting the TRG register to 0000H Overflow or compare match with the TRGGRj register • Buffer operation

Remark: j = A or B

2.5 Differences in Phase Counting Mode

The operation of phase counting mode in timer RG in R8C/36M Group corresponds to phase counting mode in timer RG in RL78/G14.
Table 2.6 lists the differences between phase counting mode in timer RG in R8C/36M Group and phase counting mode in timer RG in RL78/G14.

Table 2.6 Differences between Timer RG (Phase Counting Mode)

Item	R8C/36M Group (Phase Counting Mode)	RL78/G14 (Phase Counting Mode)
Count source	External signal input to the TRGCLKj pin	External signal input to the TRGCLKj pin
Count operations	Increment/decrement	Increment/decrement
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.	1 (count starts) is written to the TRGSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.	0 (count stops) is written to the TRGSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (valid edge of the TRGIOj input) • Compare match (the content of the TRG register matches the content of TRGGRj register) • TRG register underflows • TRG register overflows	• Input capture (valid edge of TRGIOj input) • Compare match (the contents of TRG register matches the content of TRGGRj register) • TRG register overflows • TRG register underflows
TRGIOA pin function	Programmable I/O port, input-capture input, output-compare output, or PWM output	I/O port, input-capture input, output-compare output, or PWM output
TRGIOB pin function	Programmable I/O port, input-capture input, or output-compare output	I/O port, input-capture input, or output-compare output
TRGCLKA, TRGCLKB pin functions	External clock input	External clock input
Read from timer	The count value can be read by reading the TRG register.	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.	The TRG register can be written to.
Selectable functions	• Selection of counter addition/substitution conditions Selected by bits CNTEN0 to CNTEN7 bits in the TRGCNTC register. • Input capture/output compare functions and PWM functions can be used.	• Selection of counter increment/decrement conditions Selected by bits CNTEN0 to CNTEN7 in the TRGCNTC register. • Input capture/output compare functions and PWM function can be used.

Remark: j = A or B

2.6 Assigned I/O Pins

Table 2.7 lists the assigned I/O pins used in timer RG in R8C/36M Group and timer RG in RL78/G14.

Table 2.7 I/O Pins

Pin Name	R8C/36M Group	RL78/G14	I/O	Function
TRGCLKA	P3_0	P00	Input	• In phase counting mode A-phase input • When not in phase counting mode External clock A input
TRGCLKB	P3_2	P01	Input	• In phase counting mode B-phase input • When not in phase counting mode External clock B input
TRGIOA	P5_6	P50	I/O	• In timer mode (output compare function) TRGGRA output compare output • In timer mode (input capture function) TRGGRA input capture input • In PWM mode PWM output
TRGIOB	P5_7	P51	I/O	• In timer mode (output compare function) TRGGRB output compare output • In timer mode (input capture function) TRGGRB input capture input

2.7 Event Input Signal from the ELC

When using the RL78/G14 in timer mode or phase counting mode with the input capture function selected, input capture operation B can be executed by an event input signal from the ELC.

2.8 Register Compatibilities

Register compatibilities between timer RG in R8C/36M Group and timer RG in RL78/G14 are listed in Table 2.8 and Table 2.9.

Table 2.8 Register Compatibilities (1/2)

Item	R8C/36M Group	RL78/G14
Module standby control	• MSTCR register MSTTRG bit	• PER1 register TRGEN bit
PWM mode select	• TRGMR register PWM bit	• TRGMR register TRGPWM bit
Phase counting mode select	• TRGMR register MDF bit	• TRGMR register TRGMDF bit
Count control in phase counting mode	• TRGCNTC register	• TRGCNTC register
TRGIOA pin digital filter function select	• TRGMR register DFA bit	• TRGMR register TRGDFA bit
TRGIOB pin digital filter function select	• TRGMR register DFB bit	• TRGMR register TRGDFB bit
Digital filter function clock select	• TRGMR register Bits DFCK0 and DFCK1	• TRGMR register Bits TRGDFCK0 and TRGDFCK1
TRG count start	• TRGMR register TSTART bit	• TRGMR register TRGSTART bit
Count source select	• TRGCR register Bits TCK0 to TCK2	• TRGCR register Bits TRGTCK0 to TRGTCK2
External clock valid edge select	• TRGCR register Bits CKEG0 and CKEG1	• TRGCR register Bits TRGCKEG0 and TRGCKEG1
TRG register clear source select	• TRGCR register Bits CCLR0 and CCLR1	• TRGCR register Bits TRGCCLR0 and TRGCCLR1
Interrupt enable	• TRGIER register Bits IMIEA, IMIEB, UDIE and OVIE	• TRGIER register Bits TRGIMIEA, TRGIMIEB, TRGUDIE, and TRGOVIE
Status flag	• TRGSR register Bits IMFA, IMFB, UDF, OVF, and DIRF	• TRGSR register Bits TRGIMFA, TRGIMFB, TRGUDF, TRGOVF, and TRGDIRF

Table 2.9 Register Compatibilities (2/2)

Item	R8C/36M Group	RL78/G14
TRGGRA control	• TRGIOR register Bits IOA0 and IOA1	• TRGIOR register Bits TRGIOA0 and TRGIOA1
TRGGRA mode select	• TRGIOR register IOA2 bit	• TRGIOR register TRGIOA2 bit
TRGGRC register function select	• TRGIOR register BUFA bit	• TRGIOR register TRGBUFA bit
TRGGRB control	• TRGIOR register Bits IOB0 and IOB1	• TRGIOR register Bits TRGIOB0 and TRGIOB1
TRGGRB mode select	• TRGIOR register IOB2 bit	• TRGIOR register TRGIOB2 bit
TRGGRD register function select	• TRGIOR register BUFB bit	• TRGIOR register TRGBUFB bit
I/O pin select	• TIMSR register Bits TRGIOASEL, TRGIOBSEL, TRGCLKASEL, and TRGCLKBSEL	N/A
Setting of pins to be used for timer I/O	N/A	• Registers PM0 and PM5 • Registers P0 and P5
Interrupt priority level select	• TRGIC register Bits ILVL0 to ILVL2	• PR02H register TRGPR0 bit • PR12H register TRGPR1 bit
Interrupt request bit	• TRGIC register IR bit	• IF2H register TRGIF bit
Interrupt enable/disable	N/A	• MK2H register TRGMK bit
ELC input capture request select	N/A	• TRGMR register TRGELCICE bit

2.9 Changes in Registers

2.9.1 Timer RG Mode Register (TRGMR)

Clocks that can be specified for the digital filter function vary between R8C/36M Group and RL78/G14. Table 2.10 lists the comparison of digital filter function clocks.

Table 2.10 Comparison of Digital Filter Function Clocks

R8C/36M Group			RL78/G14		
DFCK1 Bit	DFCK0 Bit	Function	TRGDFCK1 Bit	TRGDFCK0 Bit	Function
0	0	f32	0	0	$f_{CLK}/32$
0	1	f8	0	1	$f_{CLK}/8$
1	0	f1	1	0	f_{CLK}
1	1	Clock specified by bits TCK0 to TCK2 in TRGCR register	1	1	Clock specified by bits TRGTCK0 to TRGTCK2 in TRGCR register

The TRGELCICE bit is newly added to the RL78/G14 to select the input capture operation by an event input signal from the ELC.

2.9.2 Timer RG Control Register (TRGCR)

Count source which can be specified is different between R8C/36M Group and RL78/G14. Table 2.11 lists the comparison of count sources.

Table 2.11 Comparison of Count Sources

R8C/36M Group				RL78/G14			
TCK2 Bit	TCK1 Bit	TCK0 Bit	Function	TRGTCK2 Bit	TRGTCK1 Bit	TRGTCK0 Bit	Function
0	0	0	f1	0	0	0	f_{CLK}
0	0	1	f2	0	0	1	$f_{CLK}/2$
0	1	0	f4	0	1	0	$f_{CLK}/4$
0	1	1	f8	0	1	1	$f_{CLK}/8$
1	0	0	f32	1	0	0	$f_{CLK}/32$
1	0	1	TRGCLKA input	1	0	1	TRGCLKA input
1	1	0	fOCO40M	1	1	0	Do not set.
1	1	1	TRGCLKB input	1	1	1	TRGCLKB input

2.9.3 Timer Pin Select Register (TIMSR, R8C/36M Group Only)

In R8C/36M Group, set the TIMSR register to specify whether to use pins assigned to timer RG I/O as I/O ports or timer RG I/O pins.
Set registers P0, P5, PM0, and PM5 in the RL78/G14 to use ports as timer RG I/O pins.

3. Notes

3.1 I/O Pin Settings

3.1.1 R8C/36M Group

To use the I/O pins in R8C/36M Group, make sure to set the TIMSR register before setting registers associated with timer RG. Do not change the setting value in the TIMSR register while timer RG is operating.

3.1.2 RL78/G14

In the RL78/G14, I/O ports which are multiplexed with pins TRGIOA and TRGIOB function as input ports after the MCU is reset.

To use pins TRGIOA and TRGIOB for output, perform the following steps:
(1) Set the mode, initial value, and enable the output in order to set the initial value and enable output by an SFR (Special Function Register).
(2) Set bits P50 and P51 in the P5 register which correspond to pins TRGIOA and TRGIOB to 0.
(3) Set bits PM50 and PM51 in the PM5 register which correspond to pins TRGIOA and TRGIOB to 0 in output mode (output is started from pins TRGIOA and TRGIOB).
(4) Start timer RG (set the TRGSTART bit in the TRGMR register to 1).

To change bits PM50 and PM51 in the PM5 register which correspond to pins TRGIOA and TRGIOB from output mode to input mode, perform the following steps:
(1) Set bits PM50 and PM51 in the PM5 register which correspond to pins TRGIOA and TRGIOB to 1 in input mode (output is started from pins TRGIOA and TRGIOB).
(2) Set the input capture function.
(3) Start timer RG (set the TRGSTART bit in the TRGMR register to 1).

When pins TRGIOA and TRGIOB are changed from output mode to input mode, timer RG may capture the input signals depending on the pin state. When the digital filter is not used, timer RG detects an edge after two or more CPU clock cycles elapsed. Timer RG detects an edge after five or more sampling clock cycles of the digital filter elapsed if the digital filter is used.

3.2 SFR Read/Write Access

3.2.1 R8C/36M Group

In R8C/36M Group, set the MSTTRG bit in the MSTCR register to 0 (active) before setting other registers. When the MSTTRG bit is set to 1 (standby), access to the timer associated registers (addresses 0170h to 017Fh) is disabled.

3.2.2 RL78/G14

To set timer RG in the RL78/G14, set the TRGEN bit in the PER1 register to 1 (enable reading or writing the SFR used in timer RG) before setting other registers. When the TRGEN bit is 1 (disable reading or writing the SFR used in timer RG), writing to timer RG associated registers is ignored and all values read become the default values (except port registers and port mode registers).

(1) TRGMR register

To switch the digital filter clock, perform the following steps:

(a) When the TRGSTART bit in the TRGMR register is 0 (stop counting), set bits TRGDFA and TRGDFB (bits to select the digital filter function of pins TRGIOA and TRGIOB) in the TRGMR register, and bits TRGDFCK0 and TRGDFCK1 (bits to select the clock used in the digital filter function) in the TRGMR register.

(b) Set the TRGSTART bit to 1 (start counting).

When not using the digital filter, if the reset values of bits TRGDFCK1 and TRGDFCK0 (00B, $f_{CLK}/32$) have not been changed, the TRGMR register can be set using just step (b).

In addition to external input pins (TRGIOA and TRGIOB), an event input signal from the ELC can also be selected as an operating source for input capture. To use this function, set the TRGELCICE bit in the TRGMR register to 1, and set the input capture function (set bits TRGIOB2 to TRGIOB0 to 100B to set an valid edge of the input capture as the rising edge). This function is disabled in PWM mode (the TRGPWM bit in the TRGMR register is 1) or the output compare function in timer mode is used (the TRGIOB2 bit in the TRGIOR register is 0).

(2) TRG register

Writing to the TRGMR register has priority over count reset operations generated by timer RG operating conditions.

4. How to Migrate Timer RG in this Sample Code

In this sample program, the operation of timer RG in R8C/36M Group is realized with RL78/G14 by the method shown in Table 4.1.

For the sample program of "PWM mode" and "phase counting mode", please refer to the application notes that are introduced in "8. Reference Application Notes".

In this application note, we only detail the sample program for the timer mode (input capture function) and timer mode (output compare function).
For detailed content of the sample program, please refer to "5. Example of Migration from Timer Mode (Input Capture Function)" ~ "6. Example of Migration from Timer Mode (Output Compare Function)".

Table 4.1 How to Migrate from R8C/36M Group to RL78/G14 in This Sample Program

Timer RG in R8C/36M Group	Timer RG in RL78/G14
Mode	**Mode**
Timer mode (Input capture function)	Timer mode (Input capture function)
Timer mode (Output compare function)	Timer mode (Output compare function)

5. Example of Migration from Timer Mode (Input Capture Function)

5.1 Specifications

The same operation as that in timer mode (input capture function) in timer RG of R8C/36M can be realized by using timer RG of RL78/G14.
In timer mode (input capture function), the value of the TRG register can be transferred to registers TRGGRA and TRGGRB upon detecting the input edge of the input capture/output compare pins (TRGIOA and TRGIOB). The detection edge can be selected from the rising edge/falling edge/both rising and falling edges.
The input capture function can be used for measuring pulse widths and periods.

Table 5.1 lists the peripheral function to be used and its use (an example of migration from timer mode (input capture function)), and Figure 5.1 shows the operation overview (an example of migration from timer mode (input capture function)).

Table 5.1 Peripheral Function to be Used and Its Use

(An Example of Migration from Timer Mode (Input Capture Function))

Peripheral Function	Use
Timer RG (Timer Mode (Input Capture Function))	Pulse width measurement

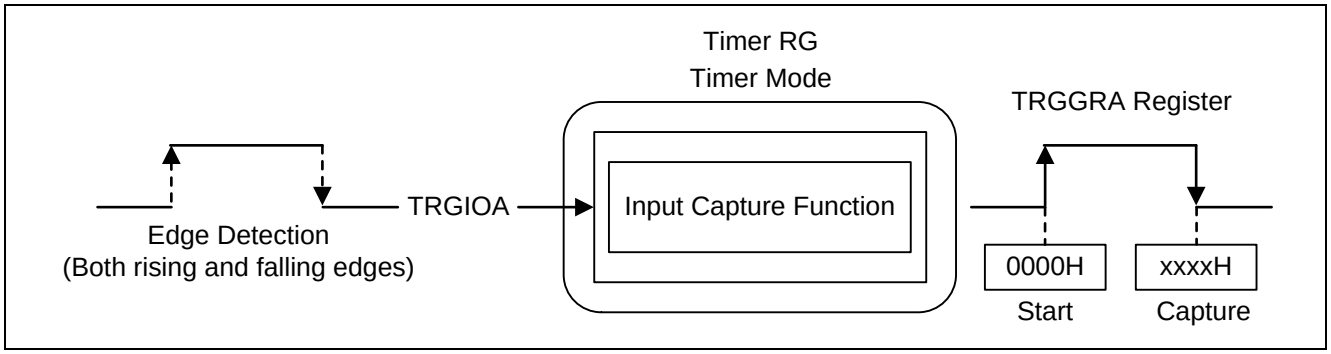


Figure 5.1 Operation Overview (An Example of Migration from Timer Mode (Input Capture Function))

Note: Figure 5.1 shows an operation example with bits TRGIOA1 and TRGIOA0 set to 10B (edge Detection: both edges of TRGIOA).

5.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 5.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.7 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode TYP. 2.75 V Rising edge 2.81 V (2.76 V to 2.87 V) Falling edge 2.75 V (2.70 V to 2.81 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

5.3 Description of Hardware

5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of the hardware configuration that is used for this chapter.

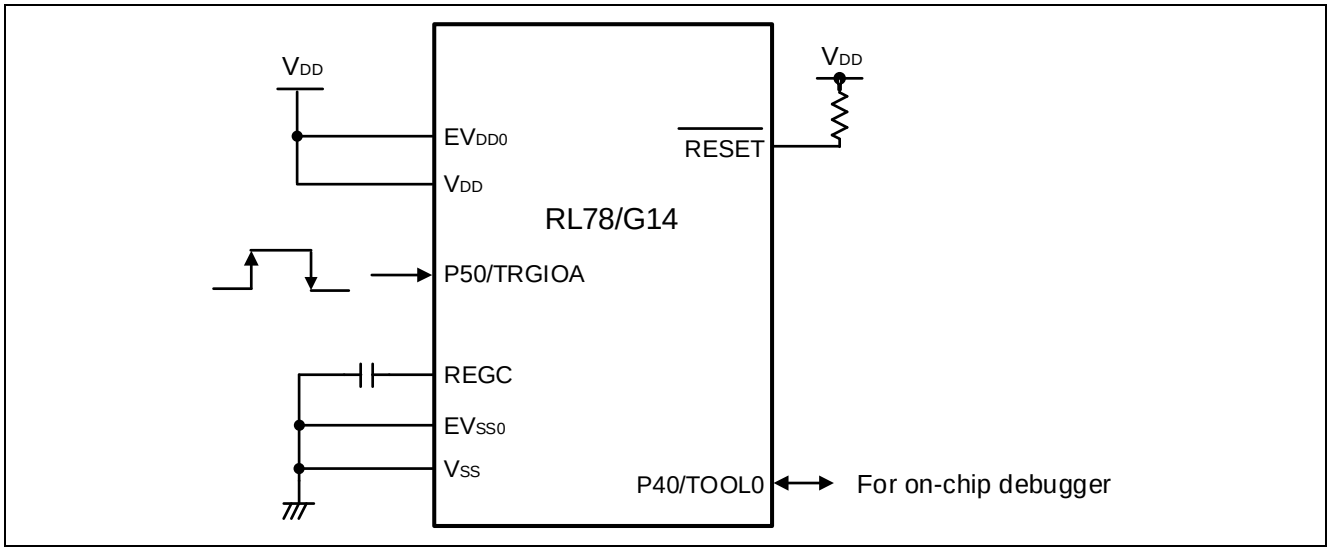


Figure 5.2 Hardware Configuration (Timer Mode (Input Capture Function))

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

5.3.2 List of Pin to be Used

Table 5.3 lists the pin to be used and its function.

Table 5.3 Pin to be Used and Its Function

Pin Name	I/O	Description
P50/TRGIOA	Input	TRGGRA input-capture input

5.4 Description of Software

5.4.1 Operation Outline

This chapter describes how to set up the timer mode (input capture function) of timer RG.
Each time a valid edge is detected on the timer input pin (TRGIOA), the MCU captures the count value of the timer and measures the time interval between pulses which arrive at the timer input pin (TRGIOA). When a timer interrupt (INTTRG) occurs upon completion of the capture, the sample code calculates the pulse interval and stores the calculation result in the on-chip RAM.

Table 5.4 lists the peripheral function to be used and its use. Figure 5.3 shows the timer mode and its interrupt operation.

(1) Initialize the timer RG.
<Conditions for setting>
Use the input capture function as the timer RG operation mode.
Select f_{CLK} as the count source of timer RG.
Use both edges to detect the input capture to the TRGIOA pin.
Use the digital filter function.
Enable an interrupt when timer RG counter overflows.
Enable an interrupt when an valid edge is detected.
Set TRGIOA pin as input mode.

(2) Sets "1" (starts counter operation) to TRGSTART bit of TRGMR register to start the count of timer RG.

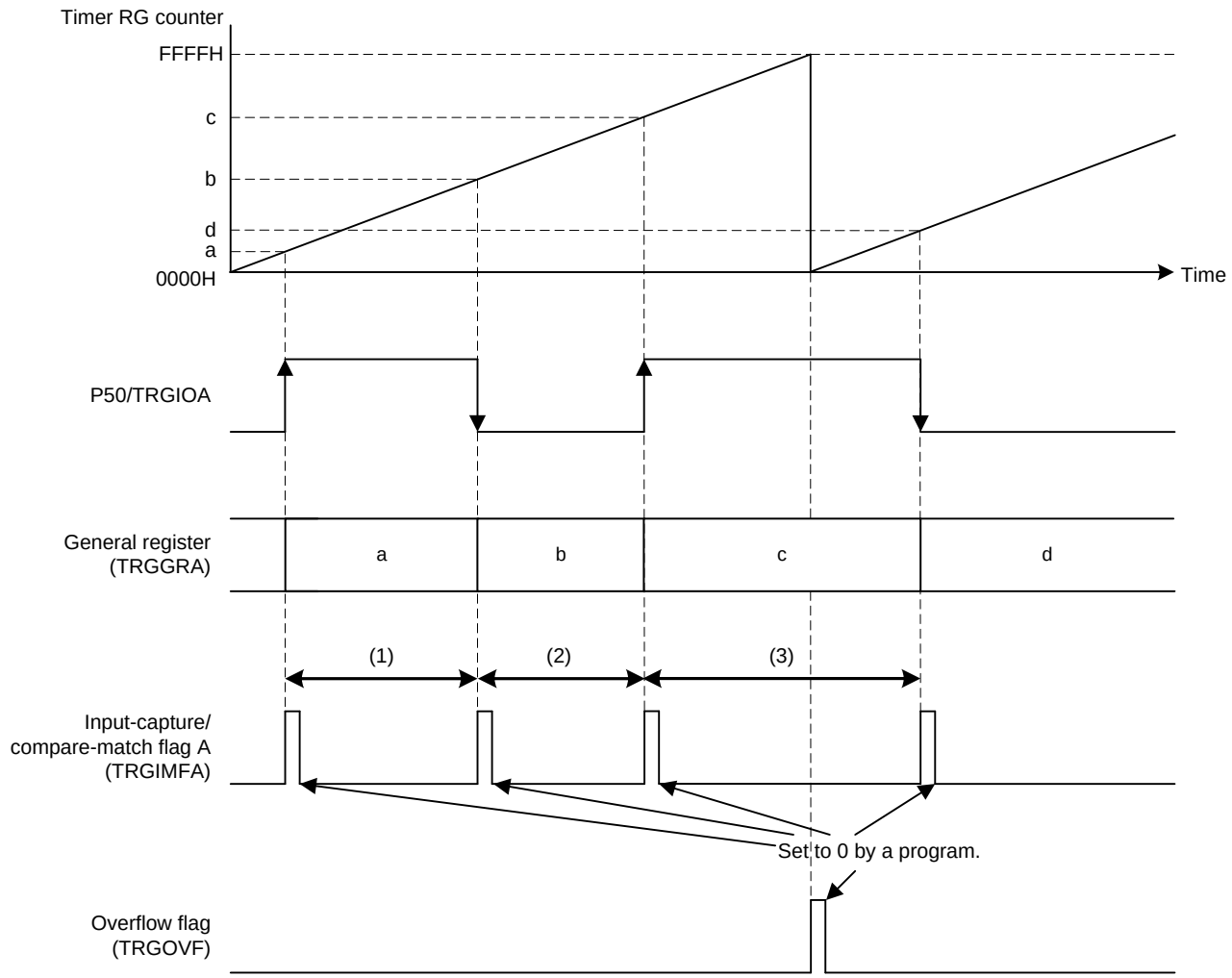
(3) Execute a HALT instruction to wait for timer interrupts (INTTRG).

(4) When the overflow interrupt is generated, increment the value of the overflow counter.
When the input-capture interrupt is generated, calculates the pulse width and stores the calculation result in the on-chip RAM.

(5) The sample code returns to step (3) to execute HALT instruction and waits for the next timer interrupt (INTTRG) from timer RG.

Table 5.4 Peripheral Function to be Used and Its Use

Peripheral Function	Use
Timer RG	Measure the pulse width of TRGIOA pin.



(1): b - a (No overflow)
(2): c - b (No overflow)
(3): 10000h - c + d (One overflow)

The width of actual pulse (high or low) obtained by the above calculation
Pulse width = Calculated value x Time for each count (Time for each count = 1/32 MHz (typ) = 31.25 ns)

Example 1: The width of high when the result of (1) is 16000.
Width of high = 16000 x 31.25 ns = 500 µs

Example 2: The width of high when the result of (3) is 64000.
Width of high = 64000 x 31.25 ns = 2 ms

Figure 5.3 Overview of Timer RG Operation and Interrupts (Input Capture Function)

5.4.2 List of Option Byte Settings

Table 5.5 summarizes the settings of the option bytes.

Table 5.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disable the watchdog timer. (Stop counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD operation (V_{LVD}): Reset mode TYP. 2.75 V Rising edge 2.81 V (2.76 V to 2.87 V) Falling edge 2.75 V (2.70 V to 2.81 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enable the on-chip debugger.

5.4.3 List of Functions

Table 5.6 lists the functions that are used in this sample program.

Table 5.6 Functions

Function Name	Outline
R_TMR_RG0_Create()	Initialize timer RG.
R_TMR_RG0_Start()	Start timer RG operation.
r_tmr_rg0_interrupt()	Process timer interrupts of timer RG.

5.4.4 Function Specifications

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RG0_Create()

Synopsis	Initialize timer RG
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RG0_Create(void)
Explanation	This function initializes timer RG.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RG0_Start()

Synopsis	Start timer RG operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RG0_Start(void)
Explanation	This function enables timer RG interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tmr_rg0_interrupt ()

Synopsis	Timer RG interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tmr_rg0_interrupt(void)
Explanation	This function measures the pulse width of the waveform from TRGIOA.
Arguments	None
Return value	None
Remarks	None

5.4.5 Flowcharts

5.4.5.1 Overall Flow

Figure 5.4 shows the overall flow of the sample program described in this chapter.

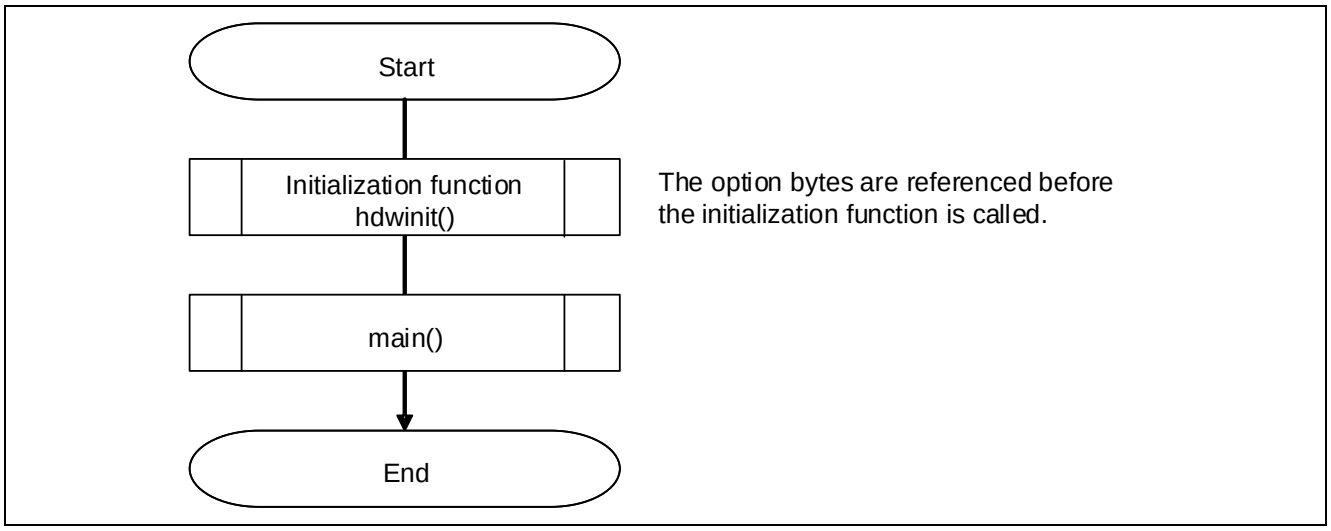


Figure 5.4 Overall Flow

5.4.5.2 Initialization Function

Figure 5.5 shows the flowchart for the initialization function.

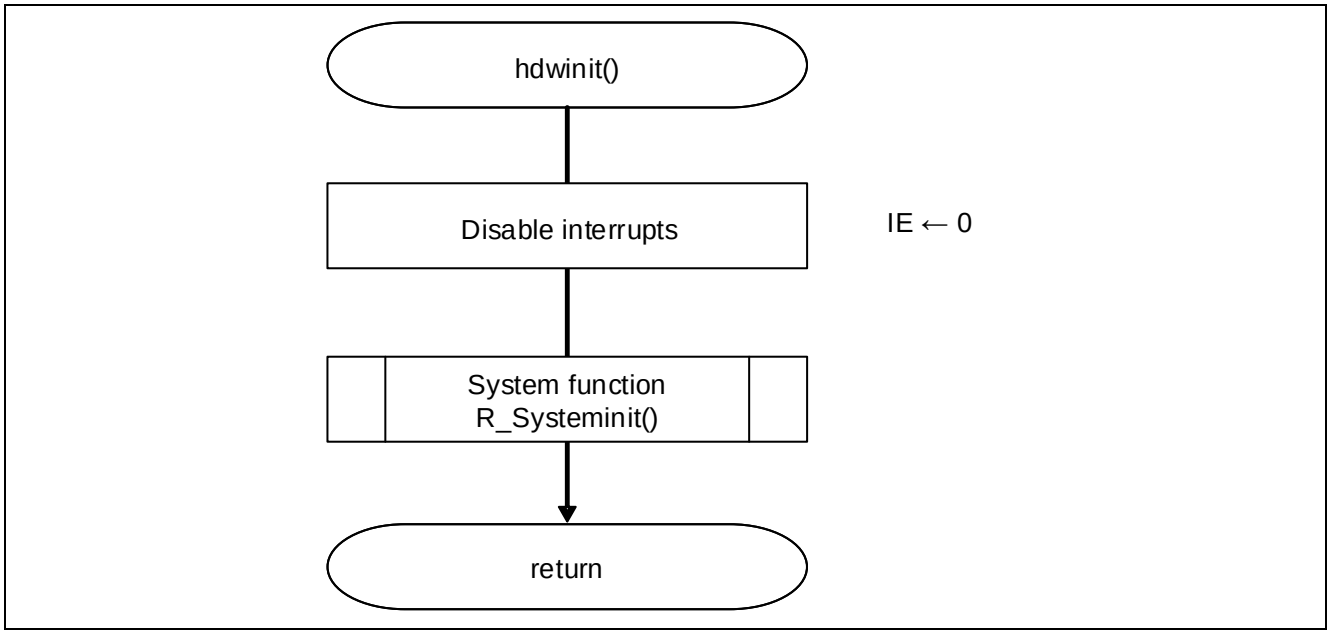


Figure 5.5 Initialization Function

5.4.5.3 System Function

Figure 5.6 shows the flowchart for the system function.

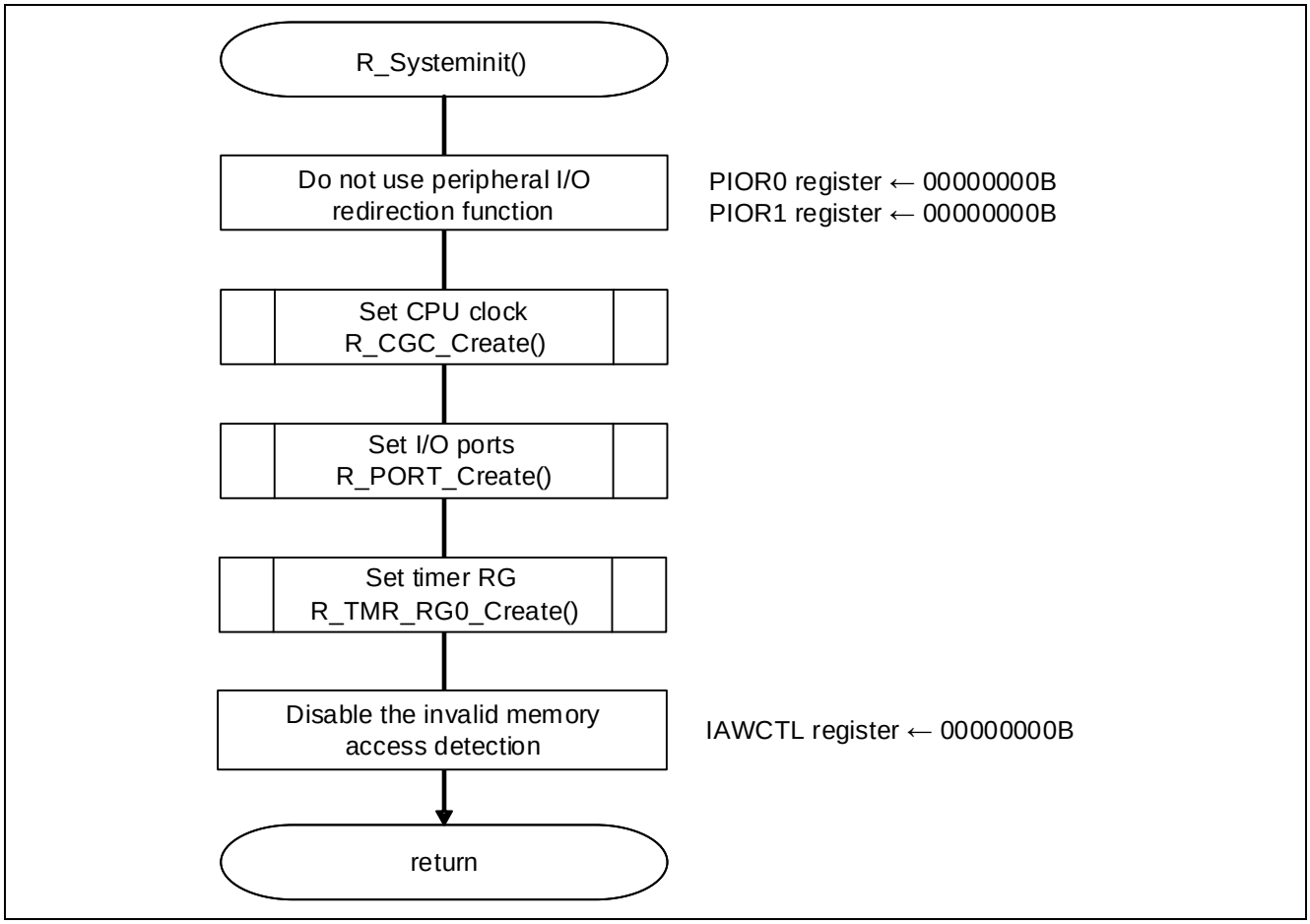


Figure 5.6 System Function

5.4.5.4 CPU Clock Setting

Figure 5.7 shows the flowchart for setting the CPU clock.

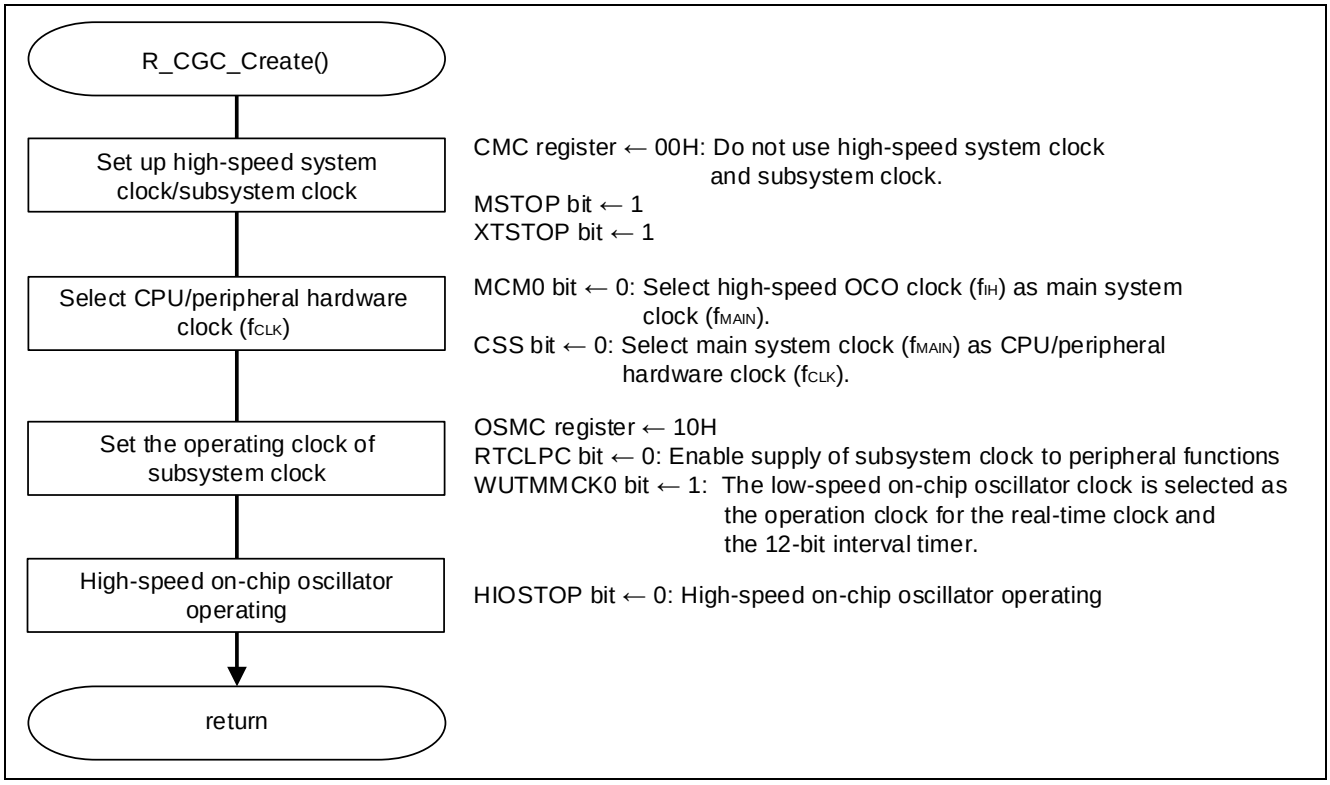


Figure 5.7 CPU Clock Setting

5.4.5.5 I/O Port Setting

Figure 5.8 shows the flowchart for setting the I/O ports.

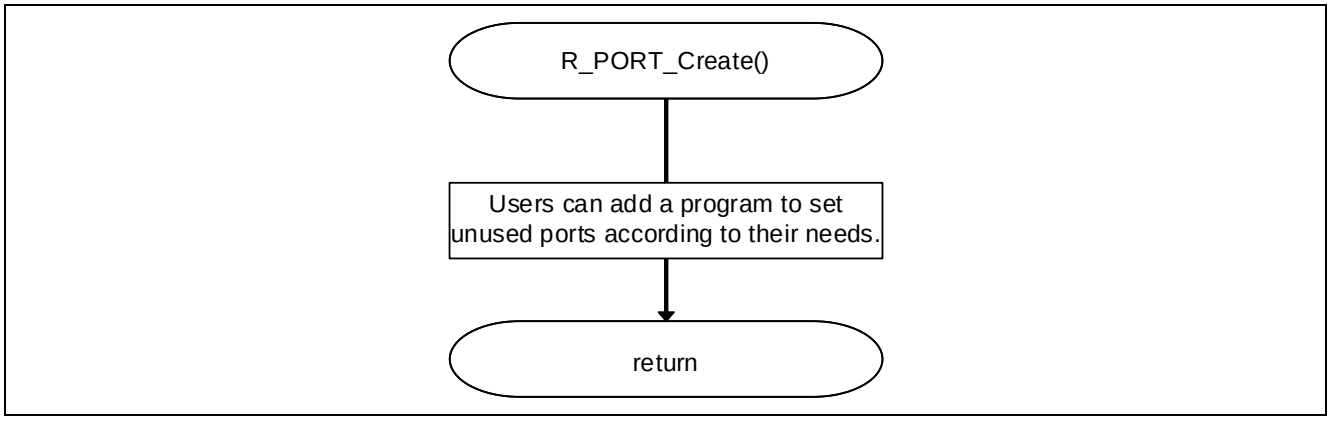


Figure 5.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.4.5.6 Timer RG Setting

Figure 5.9 shows the flowchart for setting timer RG.

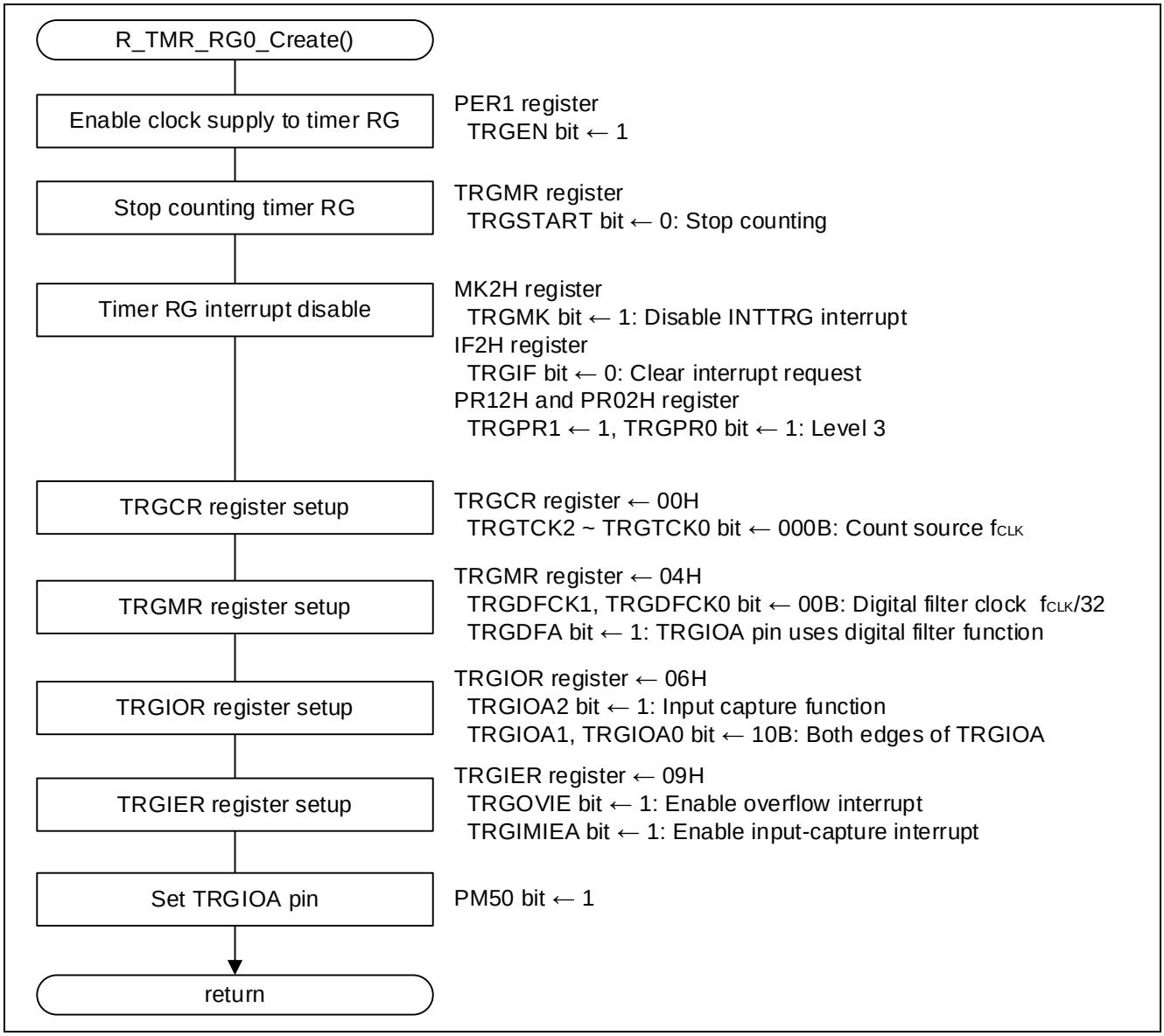


Figure 5.9 Timer RG Setting

Start to supply the clock to timer RG
• Peripheral enable register 1 (PER1)
Start to supply the clock to timer RG.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	**1**	x	x	x	0	0	x

Bit 6

TRGEN	Control of timer RG input clock supply
0	Stop input clock supply. • SFR used by timer RG cannot be written. • Timer RG is in the reset status.
1	**Enable input clock supply.** **• SFR used by timer RG can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RG operation and interrupt level

• Timer RG mode register (TRGMR)
Stop timer RG counter operation.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
0	x	x	x	x	x	x	x

Bit 7

TRGSTART	Timer RG count start
0	Count stops
1	Count starts

Disabling timer RG interrupt
• Interrupt mask flag register (MK2H)
Disable interrupt processing.
• Interrupt request flag register (IF2H)
Clear the interrupt request flag.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
x	x	1	x	1	x	x	x

Bit 3

TRGMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
x	x	0	x	0	x	x	x

Bit 3

TRGIF	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting timer RG interrupt priority level
• Priority specification flag register (PR12H, PR02H)
Specifies level 3 (low priority level).

Symbol: PR12H

7	6	5	4	3	2	1	0
FLPR1	IICAPR11	1	SREPR13 TMPR113H	TRGPR1	TRDPR11	TRDPR10	PPR111 CMPPR11
x	x	1	x	**1**	x	x	x

Symbol: PR02H

7	6	5	4	3	2	1	0
FLPR0	IICAPR01	1	SREPR03 TMPR013H	TRGPR0	TRDPR01	TRDPR00	PPR011 CMPPR01
x	x	1	x	**1**	x	x	x

Bit 3

TRGPR1	TRGPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RG operation

• Timer RG control register (TRGCR)
Count source selection.

Symbol: TRGCR

7	6	5	4	3	2	1	0
0	TRGCCLR1	TRGCCLR0	TRGCKEG1	TRGCKEG0	TRGTCK2	TRGTCK1	TRGTCK0
0	x	x	x	x	0	0	0

Bit 2 to 0

TRGTCK2	TRGTCK1	TRGTCK0	Timer RG count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/2$
0	1	0	$f_{CLK}/4$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/32$
1	0	1	TRGCLKA input
1	1	1	TRGCLKB input
Other than above			Setting prohibited

• Timer RG mode register (TRGMR)
Select digital filter.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
x	x	0	0	x	1	x	x

Bit 5 and 4

TRGDFCK1	TRGDFCK0	Digital filter function clock select [Note]
0	0	$f_{CLK}/32$
0	1	$f_{CLK}/8$
1	0	f_{CLK}
1	1	Clock selected by bits TRGTCK0 to TRGTCK2 in TRGCR register

Bit 2

TRGDFA	Digital filer function select for TRGIOA pin
0	Digital filter function not used
1	Digital filter function used
When the digital filter is used, edge detection is performed after up to five cycles of the sampling clock.	

Note: Set this bit while the TRGSTART bit is 0 (count stops).

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RG I/O control register (TRGIOR)
Set the mode and select the valid edge.

Symbol: TRGIOR

7	6	5	4	3	2	1	0
TRGBUFB	**TRGIOB2**	**TRGIOB1**	**TRGIOB0**	**TRGBUFA**	**TRGIOA2**	**TRGIOA1**	**TRGIOA0**
x	x	x	x	x	**1**	**1**	**0**

Bit 2

TRGIOA2	TRGGRA mode select Notes 1, 2
0	Output compare function
1	**Input capture function**

Bit 1 and 0

TRGIOA1	TRGIOA0	TRGGRA control
0	0	Rising edge of TRGIOA
0	1	Falling edge of TRGIOA
1	**0**	**Both edges of TRGIOA**
Other than above		Setting prohibited
In the input capture function, input the capture content of TRG register to TRGGRA register		

Note 1:When the TRGIOj2 (j = A or B) bit is 1 (input capture function), the TRGGRj register functions as an input capture register.

Note 2:When the TRGIOj2 (j = A or B) bit is 0 (output compare function), the TRGGRj register functions as a compare match register. After a reset, the TRGIOj pin outputs as follows until bits TRGIOj0 and TRGIOj1 are set and the first compare match occurs.

TRGIOj1 and TRGIOj0 = 01B: High output
10B: Low output
11B: Low output

This TRGIOR register controls I/O pins in timer mode. It is disabled in PWM mode. It is disabled in PWM mode.

Set the TRGIOR register while the count is stopped (TRGSTART in TRGMR register = 0).

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RG interrupt enable register (TRGIER)
Enable/Disable interrupt.

Symbol: TRGIER

7	6	5	4	3	2	1	0
0	0	0	0	TRGOVIE	TRGUDIE	TRGIMIEB	TRGIMIEA
0	0	0	0	1	0	0	1

Bit 3

TRGOVIE	Overflow interrupt enable
0	Interrupt by TRGOVF bit disabled
1	**Interrupt by TRGOVF bit enabled**

Bit 2

TRGUDIE	Underflow interrupt enable
0	**Interrupt by TRGUDF bit disabled**
1	Interrupt by TRGUDF bit enabled

Bit 1

TRGIMIEB	Input-capture/compare-match interrupt enable B
0	**Interrupt by TRGIMFB bit disabled**
1	Interrupt by TRGIMFB bit enabled

Bit 0

TRGIMIEA	Input-capture/compare-match interrupt enable A
0	Interrupt by TRGIMFA bit disabled
1	**Interrupt by TRGIMFA bit enabled**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.4.5.7 Main Processing

Figure 5.10 shows the flowchart for the main processing.

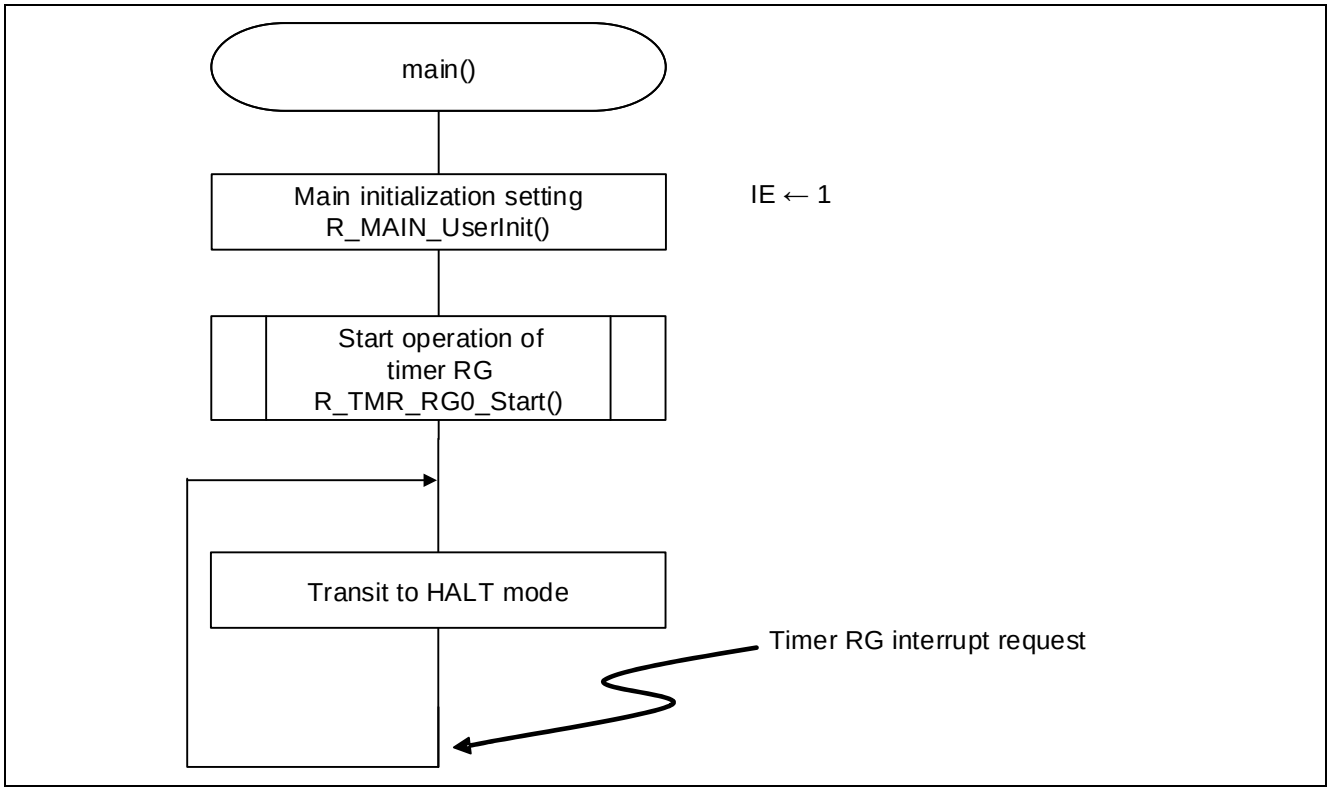


Figure 5.10 Main Processing

5.4.5.8 Timer RG Operation Start

Figure 5.11 shows the flowchart for starting timer RG operation.

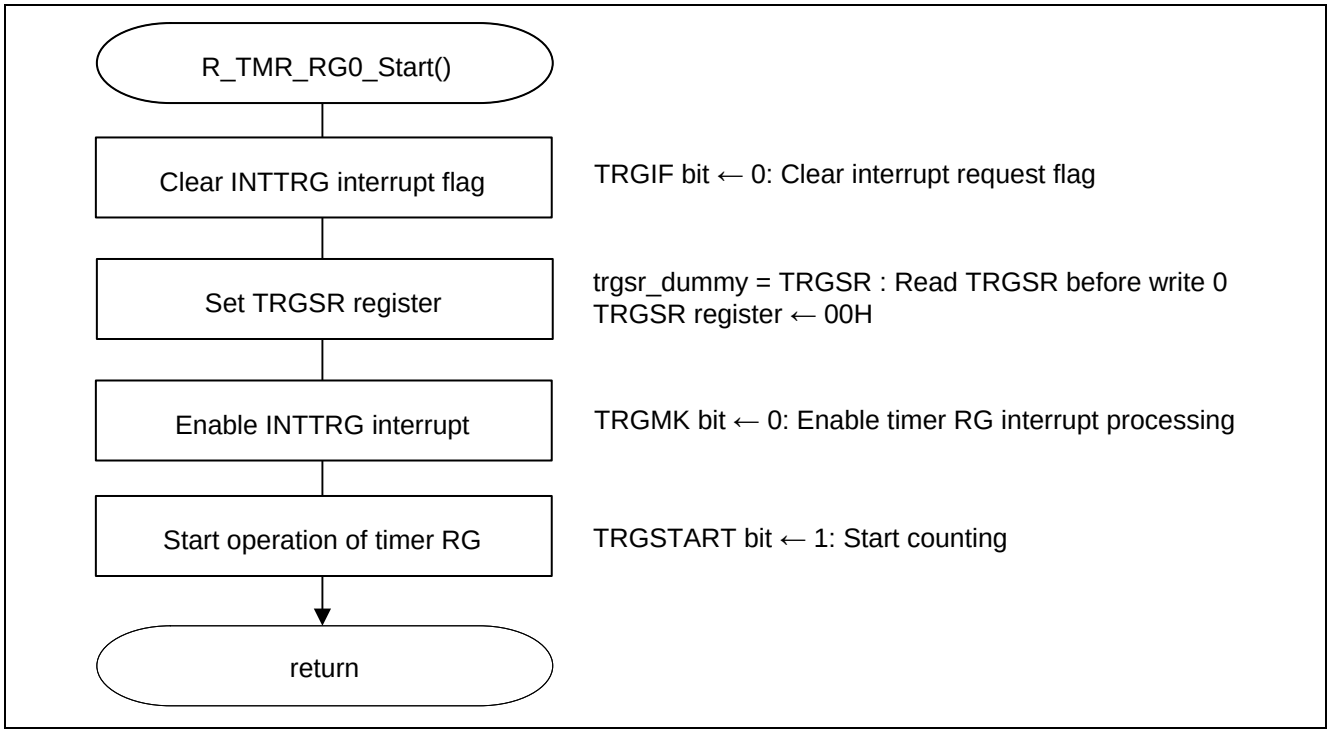


Figure 5.11 Timer RG Operation Start

Configuring the timer interrupt
• Interrupt request flag register (IF2H)
Clear the interrupt request flag.

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
x	x	0	x	**0**	x	x	x

Bit 3

TRGIF	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status.

• Interrupt mask flag register (MK2H)
Enable interrupt processing.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
x	x	1	x	**0**	x	x	x

Bit 3

TRGMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Starting timer RG counter operation
• Timer RG mode register (TRGMR)
Start timer RG counter operation.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
1	x	x	x	x	x	x	x

Bit 7

TRGSTART	Timer RG count start
0	Count stops
1	**Count starts**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

5.4.5.9 INTTRG Interrupt Processing

Figure 5.12 shows the flowchart for INTTRG interrupt processing.

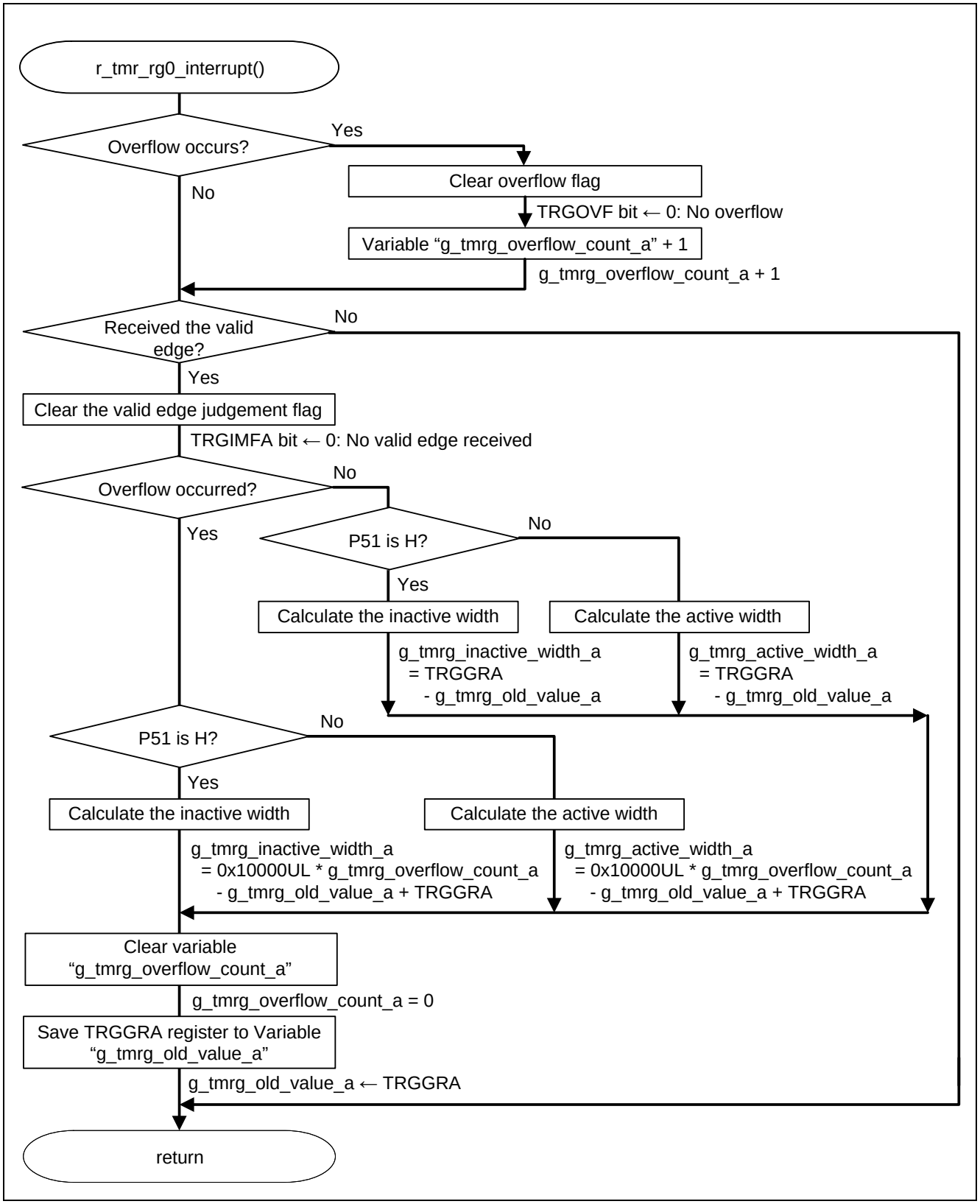


Figure 5.12 INTTRG Interrupt Processing

6. Example of Migration from Timer Mode (Output Compare Function)

6.1 Specifications

The same operation as that in timer mode (output compare function) in timer RG of R8C/36M can be realized by using timer RG of RL78/G14.
This mode (output compare function) detects when the content of the TRG register matches the content of the TRGGRA register or the TRGGRB register (compare match). When a match occurs, a signal is output from the TRGIOA or TRGIOB pin at a given level.

Table 6.1 lists the peripheral function to be used and its use (an example of migration from timer mode (output compare function)), and Figure 6.1 shows the operation overview (an example of migration from timer mode (output compare function)).

Table 6.1 Peripheral Function to be Used and Its Use

(An Example of Migration from Timer Mode (Output Compare Function))

Peripheral Function	Use
Timer RG (Timer Mode (Output Compare Function))	Output the pulse by a compare match between the TRG register and TRGGRB register.

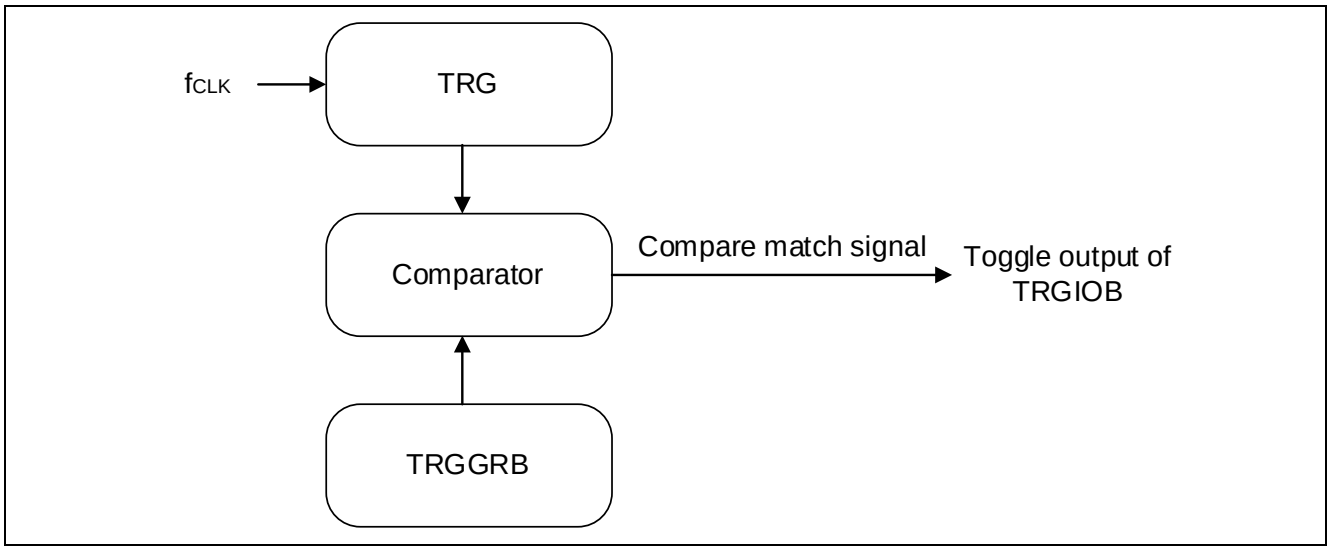


Figure 6.1 Operation Overview

(An Example of Migration from Timer Mode (Output Compare Function))

6.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

Table 6.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.7 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode TYP. 2.75 V Rising edge 2.81 V (2.76 V to 2.87 V) Falling edge 2.75 V (2.70 V to 2.81 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V6.0.0 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

6.3 Description of Hardware

6.3.1 Hardware Configuration Example

Figure 6.2 shows an example of the hardware configuration that is used for this chapter.

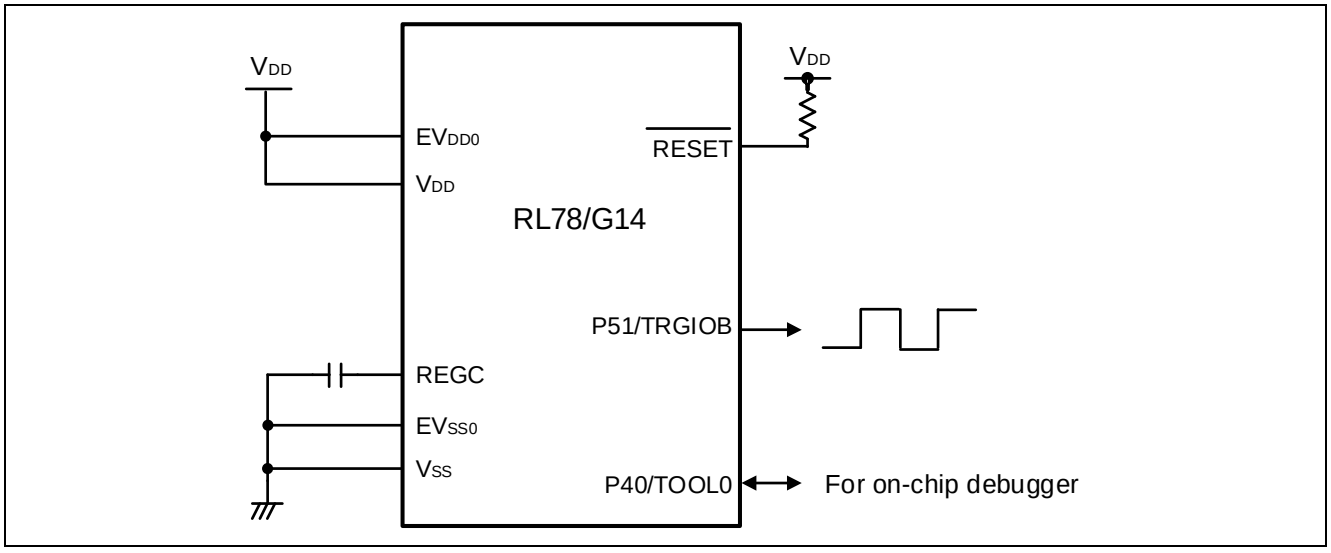


Figure 6.2 Hardware Configuration (Timer Mode (Output Compare Function))

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

6.3.2 List of Pin to be Used

Table 6.3 lists the pin to be used and its function.

Table 6.3 Pin to be Used and Its Function

Pin Name	I/O	Description
P51/TRGIOB	Output	TRGGRB output compare output.

6.4 Description of Software

6.4.1 Operation Outline

This chapter describes how to set up the timer mode (output compare function) of timer RG.

In this sample program, set the TRGGRB as an output compare function. When the content of the TRG register matches the content of the TRGGRB register, the output from the TRGIOB pin will be inverted every 1 ms.

Timer RG interrupt is not used in this sample program.

Table 6.4 lists the peripheral function to be used and its use. Figure 6.3 shows the timer mode and its interrupt operation.

(1) Initialize the timer RG.
<Conditions for setting>
Use the output compare function as the timer RG operation mode.
Select f_{CLK} as the count source of timer RG.
Set TRGGRB register.
Disable interrupts INTTRG.
Set TRGIOB pin as output mode.

(2) Set "1" (start counter operation) to TRGSTART bit of TRGMR register to start the count of timer RG.

(3) Execute a HALT instruction.

(4) When the compare occurs, the output of TRGIOB pin is inverted automatically.

Table 6.4 Peripheral Function to be Used and Its Use

Peripheral Function	Use
Timer RG	P51/TRGIOB output pulse (period is 2 ms, duty ratio is 50%).

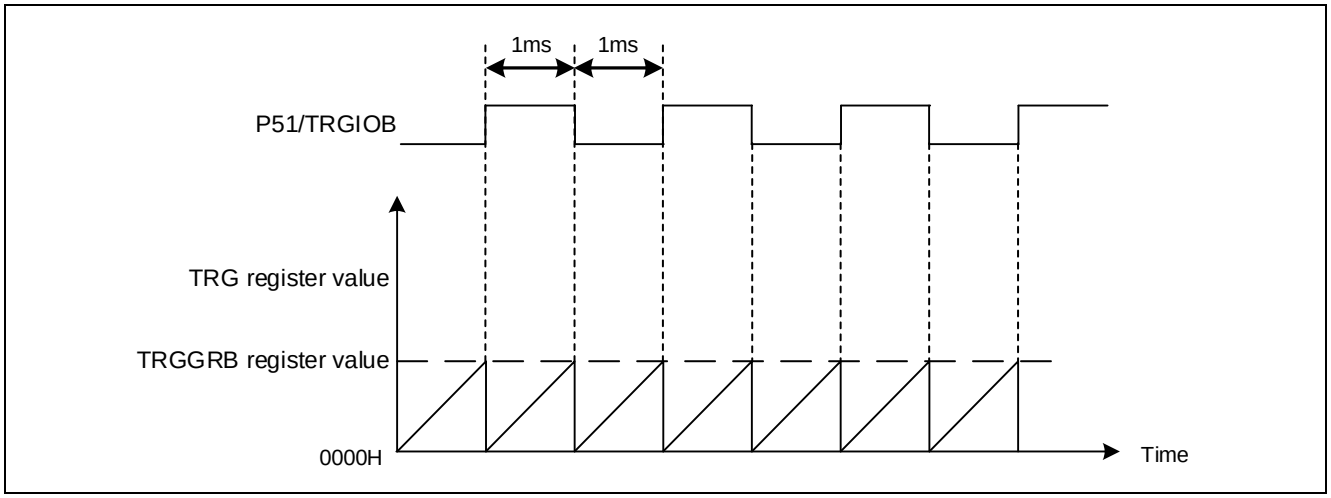


Figure 6.3 Overview of Timer RG Operation (Timer Mode (Output Compare Function))

6.4.2 List of Option Byte Settings

Table 6.5 summarizes the settings of the option bytes.

Table 6.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disable the watchdog timer. (Stop counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD operation (V_{LVD}): Reset mode TYP. 2.75 V Rising edge 2.81 V (2.76 V to 2.87 V) Falling edge 2.75 V (2.70 V to 2.81 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enable the on-chip debugger.

6.4.3 List of Functions

Table 6.6 lists the functions that are used in this sample program.

Table 6.6 Functions

Function Name	Outline
R_TMR_RG0_Create()	Initialize timer RG.
R_TMR_RG0_Start()	Start timer RG operation.

6.4.4 Function Specifications

The followings are the functions that are used in this sample program.

[Function Name] R_TMR_RG0_Create()

Synopsis	Initialize timer RG
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RG0_Create(void)
Explanation	This function initializes timer RG.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TMR_RG0_Start()

Synopsis	Start timer RG operation
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TMR_RG0_Start(void)
Explanation	This function starts count operation.
Arguments	None
Return value	None
Remarks	None

6.4.5 Flowcharts

6.4.5.1 Overall Flow

Figure 6.4 shows the overall flow of the sample program described in this chapter.

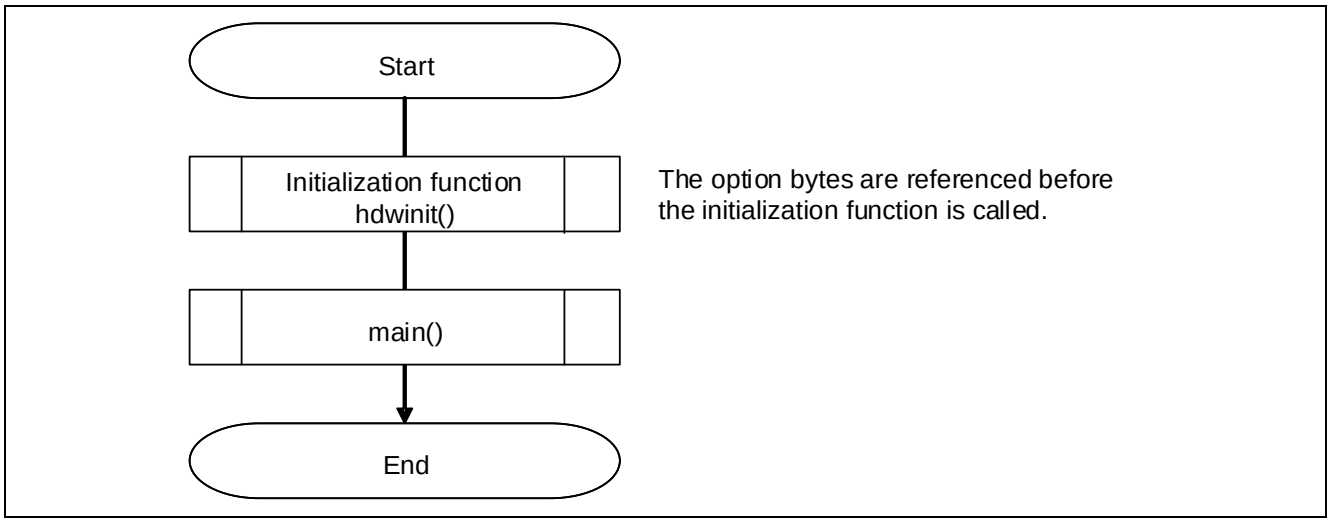


Figure 6.4 Overall Flow

6.4.5.2 Initialization Function

Figure 6.5 shows the flowchart for the initialization function.

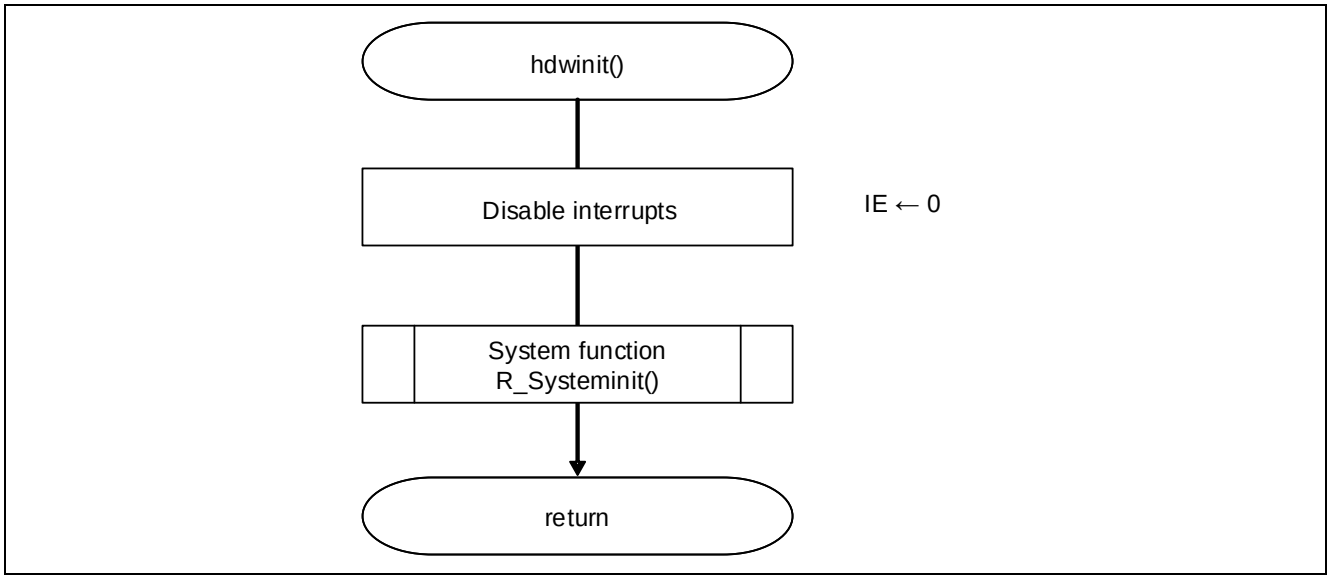


Figure 6.5 Initialization Function

6.4.5.3 System Function

Figure 6.6 shows the flowchart for the system function.

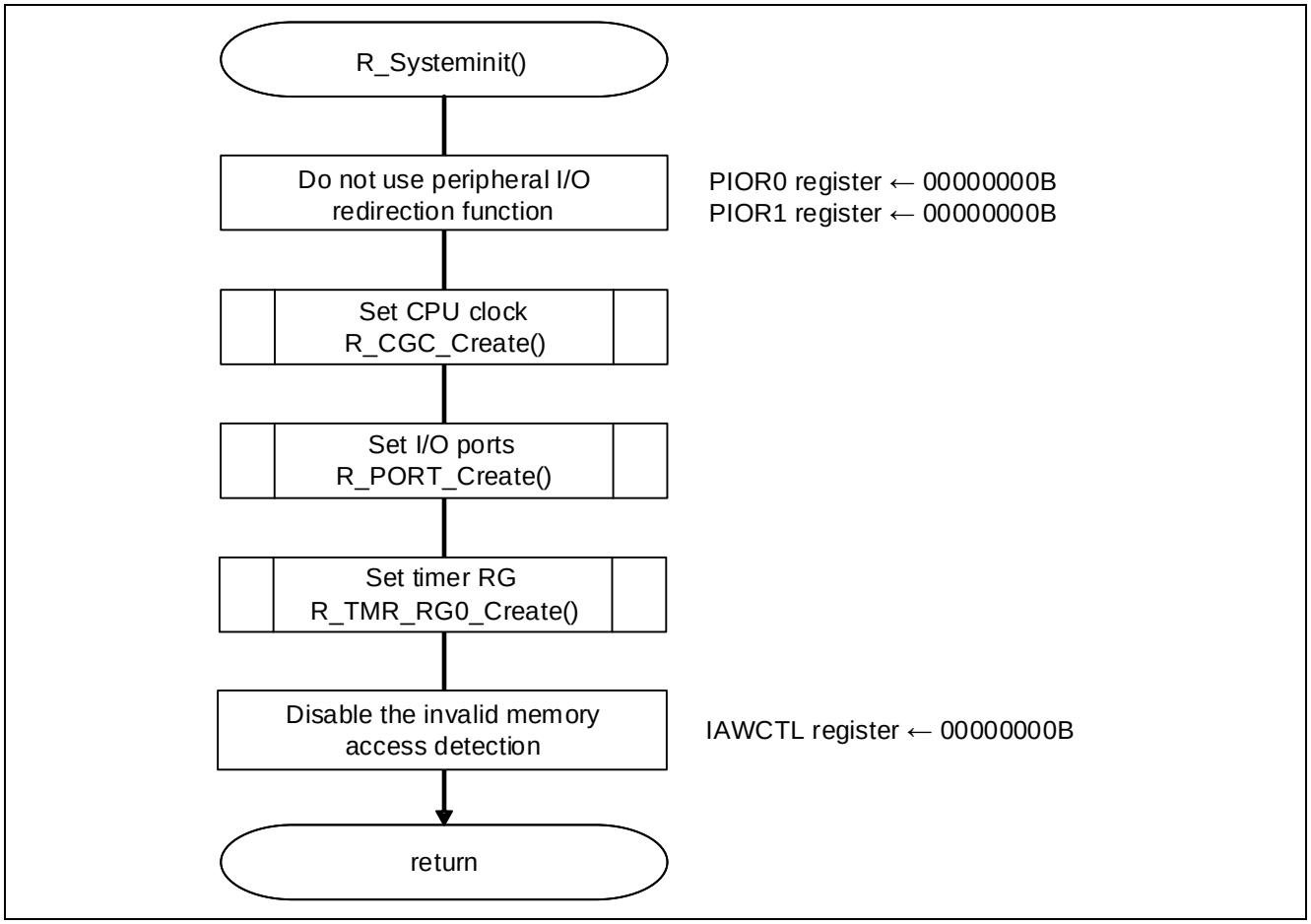


Figure 6.6 System Function

6.4.5.4 CPU Clock Setting

Figure 6.7 shows the flowchart for setting the CPU clock.

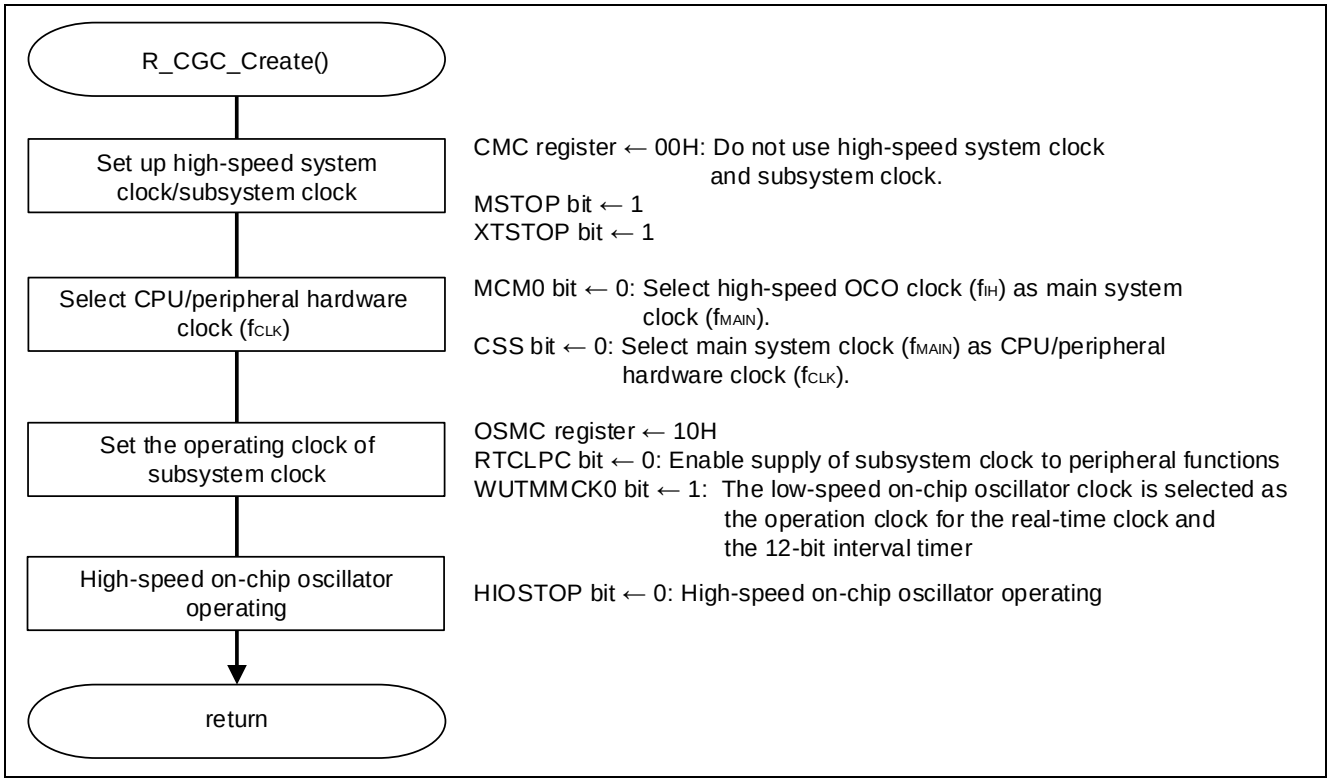


Figure 6.7 CPU Clock Setting

6.4.5.5 I/O Port Setting

Figure 6.8 shows the flowchart for setting the I/O ports.

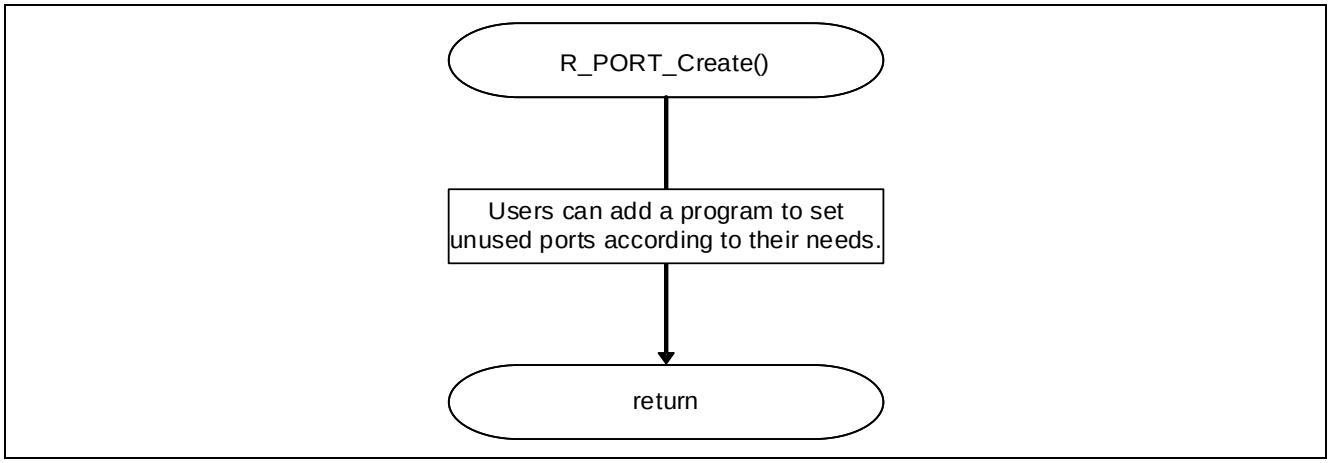


Figure 6.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

6.4.5.6 Timer RG Setting

Figure 6.9 shows the flowchart for setting timer RG.

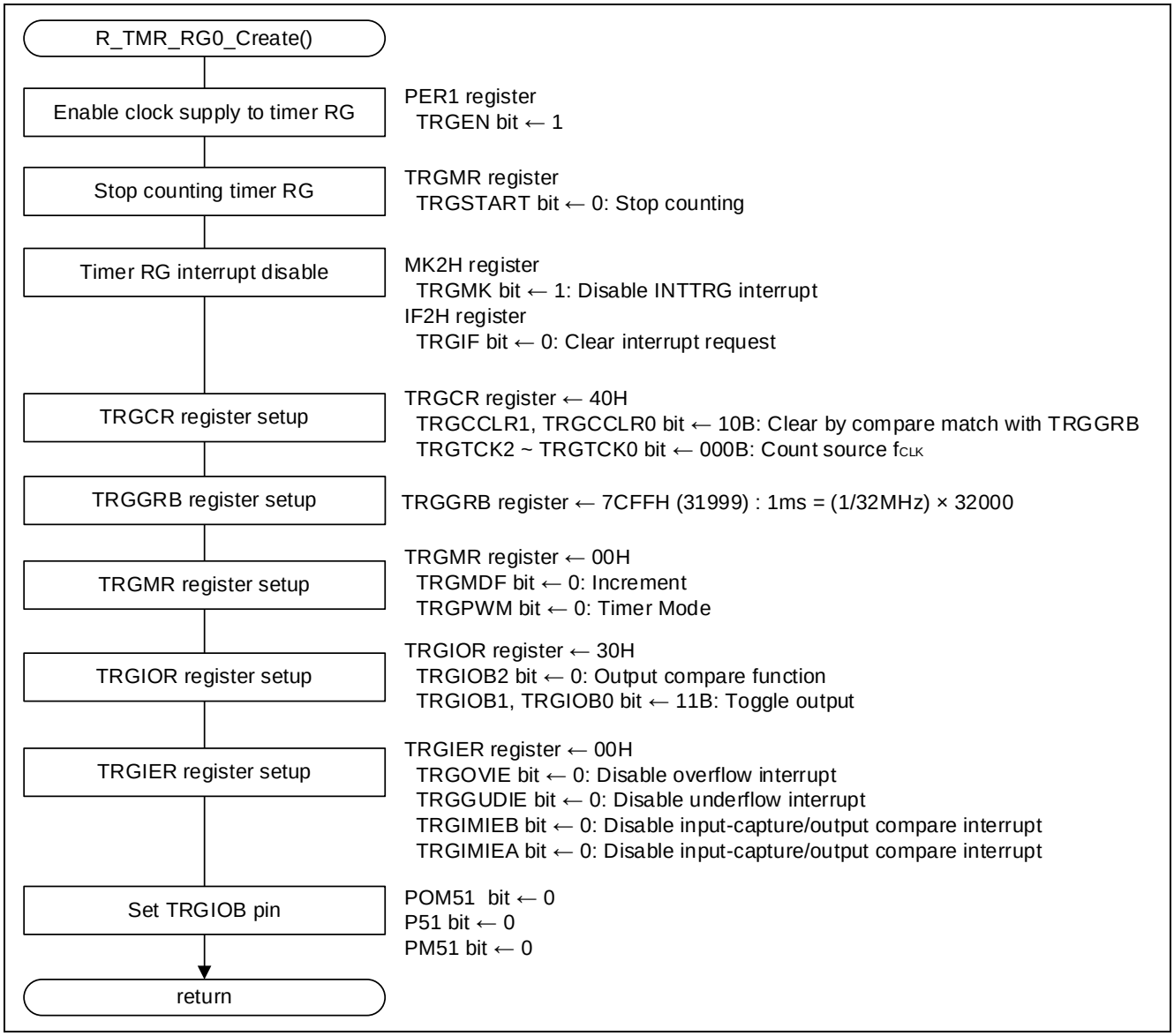


Figure 6.9 Timer RG Setting

Start to supply clock to timer RG
• Peripheral enable register 1 (PER1)
Start to supply the clock to timer RG.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	CMPEN	TRD0EN	DTCEN	0	0	TRJ0EN
x	**1**	x	x	x	0	0	x

Bit 6

TRGEN	Control of timer RG input clock supply
0	Stop input clock supply. • SFR used by timer RG cannot be written. • Timer RG is in the reset status.
1	**Enable input clock supply.** **• SFR used by timer RG can be read/written.**

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setup of timer RG operation and interrupt level

• Timer RG mode register (TRGMR)
Stop timer RG counter operation.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
0	x	x	x	x	x	x	x

Bit 7

TRGSTART	Timer RG count start
0	Count stops
1	Count starts

Disabling timer RG interrupt
• Interrupt mask flag register (MK2H)
Disable interrupt processing.
• Interrupt request flag register (IF2H)
Clear the interrupt request flag.

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	IICAMK1	1	SREMK3 TMMK13H	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
x	x	1	x	1	x	x	x

Bit 3

TRGMK	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	IICAIF1	0	SREIF3 TMIF13H	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
x	x	0	x	0	x	x	x

Bit 3

TRGIF	Interrupt request flag
0	No interrupt request signal is generated.
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the timer RG operation
• Timer RG control register (TRGCR)
Count source selection.

Symbol: TRGCR

7	6	5	4	3	2	1	0
0	TRGCCLR1	TRGCCLR0	TRGCKEG1	TRGCKEG0	TRGTCK2	TRGTCK1	TRGTCK0
0	1	0	x	x	0	0	0

Bit 6 and 5

TRGCCLR1	TRGCCLR0	TRG register clear source select
0	0	Clear disabled
0	1	Clear by input capture or compare match with TRGGRA
1	0	Clear by input capture or compare match with TRGGRB
Other than above		Setting prohibited

Bit 2 to 0

TRGTCK2	TRGTCK1	TRGTCK0	Timer RG count source select
0	0	0	f_{CLK}
0	0	1	$f_{CLK}/2$
0	1	0	$f_{CLK}/4$
0	1	1	$f_{CLK}/8$
1	0	0	$f_{CLK}/32$
1	0	1	TRGCLKA input
1	1	1	TRGCLKB input
Other than above			Setting prohibited

Setting TRGGRB register
• Timer RG general register (TRGGRB)
Setup the pulse width.

Symbol: TRGGRB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RG mode register (TRGMR)
Operation mode selection.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
x	x	x	x	x	x	0	0

Bit 1

TRGMDF	Phase counting mode select
0	Increment
1	Phase counting mode
When the TRGMDF bit is set to 0, the counter counts the count source set by bits TRGTCK0 to TRGTCK2 in the TRGCR register.	

Bit 0

TRGPWM	PWM mode select
0	Timer Mode
1	PWM mode

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RG I/O control register (TRGIOR)
Set the mode.

Symbol: TRGIOR

7	6	5	4	3	2	1	0
TRGBUFB	**TRGIOB2**	**TRGIOB1**	**TRGIOB0**	**TRGBUFA**	**TRGIOA2**	**TRGIOA1**	**TRGIOA0**
x	**0**	**1**	**1**	x	x	x	x

Bit 6

TRGIOB2	TRGGRB mode select Notes 1, 2
0	**Output compare function**
1	Input capture function

Bit 5 and 4

TRGIOB1	TRGIOB0	TRGGRB control
0	0	Pin output by compare match is disabled
0	1	Low output
1	0	High output
1	**1**	**Toggle output**
In the output compare function, output the compare match between registers TRG and TRGGRB		

Note 1:When the TRGIOj2 (j = A or B) bit is 1 (input capture function), the TRGGRj register functions as an input capture register.

Note 2:When the TRGIOj2 (j = A or B) bit is 0 (output compare function), the TRGGRj register functions as a compare match register. After a reset, the TRGIOj pin outputs as follows until bits TRGIOj0 and TRGIOj1 are set and the first compare match occurs.

TRGIOj1 and TRGIOj0 = 01B: High output
10B: Low output
11B: Low output

This TRGIOR register controls I/O pins in timer mode. It is disabled in PWM mode. It is disabled in PWM mode. Set the TRGIOR register while the count is stopped (TRGSTART in TRGMR register = 0).

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

• Timer RG interrupt enable register (TRGIER)
Disable interrupt.

Symbol: TRGIER

7	6	5	4	3	2	1	0
0	0	0	0	TRGOVIE	TRGUDIE	TRGIMIEB	TRGIMIEA
0	0	0	0	0	0	0	0

Bit 3

TRGOVIE	Overflow interrupt enable
0	Interrupt by TRGOVF bit disabled
1	Interrupt by TRGOVF bit enabled

Bit 2

TRGUDIE	Underflow interrupt enable
0	Interrupt by TRGUDF bit disabled
1	Interrupt by TRGUDF bit enabled

Bit 1

TRGIMIEB	Input-capture/compare-match interrupt enable B
0	Interrupt by TRGIMFB bit disabled
1	Interrupt by TRGIMFB bit enabled

Bit 0

TRGIMIEA	Input-capture/compare-match interrupt enable A
0	Interrupt by TRGIMFA bit disabled
1	Interrupt by TRGIMFA bit enabled

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

6.4.5.7 Main Processing

Figure 6.10 shows the flowchart for the main processing.

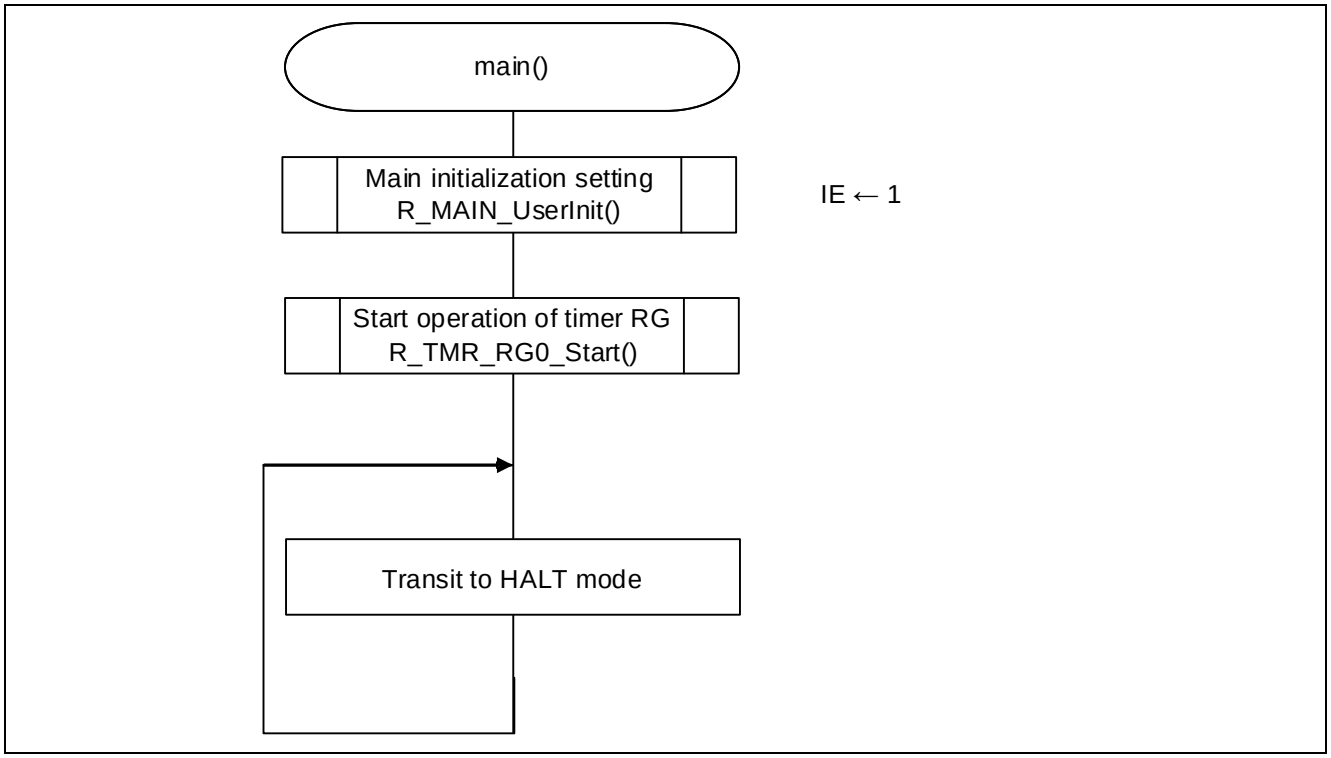


Figure 6.10 Main Processing

6.4.5.8 Timer RG Operation Start

Figure 6.11 shows the flowchart for starting timer RG operation.

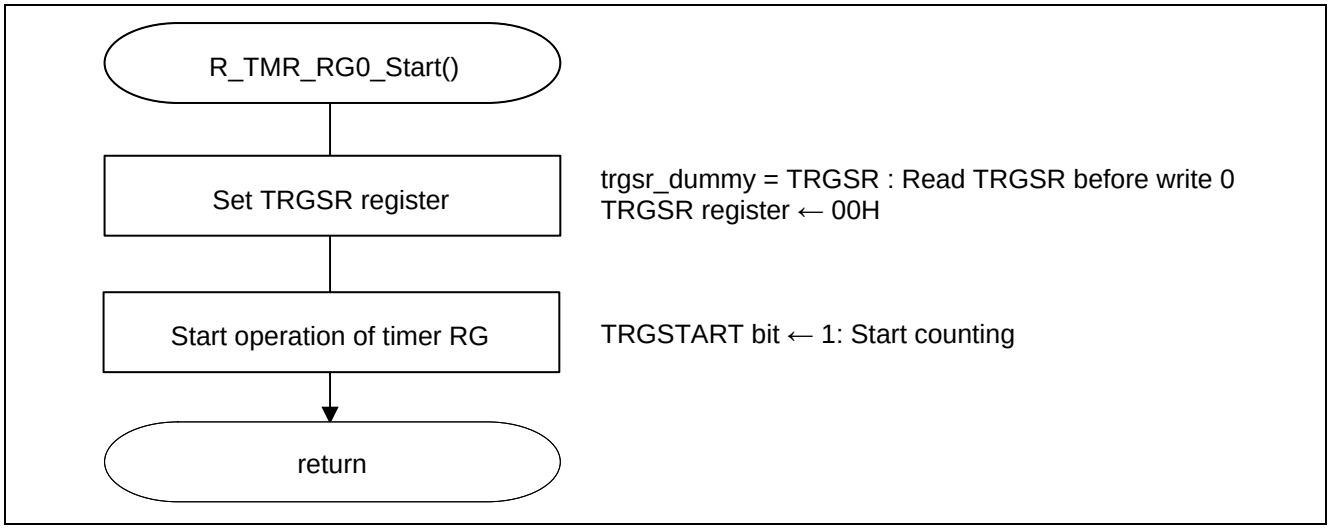


Figure 6.11 Timer RG Operation Start

Starting timer RG counter operation
• Timer RG mode register (TRGMR)
Start timer RG counter operation.

Symbol: TRGMR

7	6	5	4	3	2	1	0
TRGSTART	TRGELCICE	TRGDFCK1	TRGDFCK0	TRGDFB	TRGDFA	TRGMDF	TRGPWM
1	x	x	x	x	x	x	x

Bit 7

TRGSTART	Timer RG count start
0	Count stops
1	Count starts

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Application Notes

RL78/G14 Timer RG Buffer Operation in PWM Mode CC-RL (R01AN2853)
RL78/G14 Timer RG in Phase Counting Mode CC-RL (R01AN2573)
The latest versions can be downloaded from the Renesas Electronics website.

9. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Nov. 30, 2018	-	First edition issued

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