RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Power-on Reset and Voltage Detector

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Abstract

This document describes how to migrate from the power-on reset (POR) and voltage detector (LVD) in the R8C/36M Group to the POR and LVD in RL78/G14.

Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences between RL78/G14 and the R8C/36M Group

Table 1.1 lists the differences in the POR when used in combination with the LVD at power-on.

Table 1.1 Differences in the POR When Used in Combination with the LVD at Power-on (1)

Item	R8C/36M Group	RL78/G14
CPU clock after reset	Low-speed on-chip oscillator	High-speed on-chip oscillator
Time from when the release reset voltage is detected (note) until CPU operation starts (Note: R8C/36M Group: Vdet0, RL78/G14: V_{LVD} or V_{LVDH})	1.408 ms (typical) Start time of flash memory (CPU clock × 148 cycles) + (CPU clock × 28 cycles) CPU clock: low-speed on-chip oscillator (no division)	0 to 0.0701 ms (max.) The above time applies only when the time from when V_{DD} passes through V_{POR} until V_{DD} reaches V_{LVD} or V_{LVDH} is shorter than the "voltage stabilization wait time + POR reset processing time"
Condition to enable reset	Maintain V_{CC} for 1 ms or more at 0.5 V or lower before powering-on the MCU	Maintain V_{DD} for 300 µs or more at 0.7 V or lower before powering-on the MCU
Handling when a voltage is detected (Reset)	Voltage monitor 0	Reset mode
Handling when a voltage is detected (Interrupt)	• Voltage monitor 1 • Voltage monitor 2 (2)	Interrupt mode (3, 4)
Handling when a voltage is detected (Interrupt and reset)	• Combination of voltage monitor 0 and 1 • Combination of voltage monitor 0 and 2 • Combination of voltage monitor 0, 1, and 2	Interrupt & reset mode
Voltage to monitor	• Vdet0 (voltage monitor 0) • Vdet1 (voltage monitor 1) • Vdet2 (voltage monitor 2)	• V_{LVDH}, V_{LVDL} (interrupt & reset mode) • V_{LVD} (reset mode, interrupt mode)
Selectable detection voltage	• 4 levels (voltage monitor 0) • 16 levels (voltage monitor 1) • Fixed (voltage monitor 2)	• 12 stages (interrupt & reset mode) • 14 stages (reset mode, interrupt mode)
Detection voltage level setting	• OFS register (voltage monitor 0, FFFFh) • VD1LS register (voltage monitor 1, 0036h) • VCA2 register (voltage monitor 2, 0034h)	User option byte (000C1H)
Setting to enable LVD	OFS register (set by the LVDAS bit)	User option byte (set by the VPOC2 bit)
Necessary functions enabled by software	• Voltage monitor 1 • Voltage monitor 2	N/A

Notes: 1. For more information and electrical specifications, refer to the RL78/G14 User's Manual: Hardware.
2. Make sure to use voltage monitor 2 either with voltage monitor 0 or hardware reset.
3. Before the operation voltage falls below the specified range, RL78/G14 should be placed in STOP mode or in the reset state by the external input reset signal.
4. RL78/G14 releases an internal reset by detecting $V_{DD} \geq V_{LVD}$ at power-on after the first release of the POR. It generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ at power-on after the second release of the POR.

2. POR and LVD Operation

2.1 Relationship between POR and LVD

When using the POR, it must be used in conjunction with the LVD (voltage monitor 0 for R8C/36M Group).

To use RL78/G14 in LVD interrupt mode, before the operation voltage falls below the specified range, RL78/G14 should be placed in STOP mode or in the reset state by the external input reset signal. Otherwise, use RL78/G14 either in interrupt & reset mode or in reset mode.

2.2 Interrupt & Reset Mode

The reset is released when the supply voltage rises to reach the reset detection voltage. When the supply voltage falls to reach the reset detection voltage, the reset is generated.

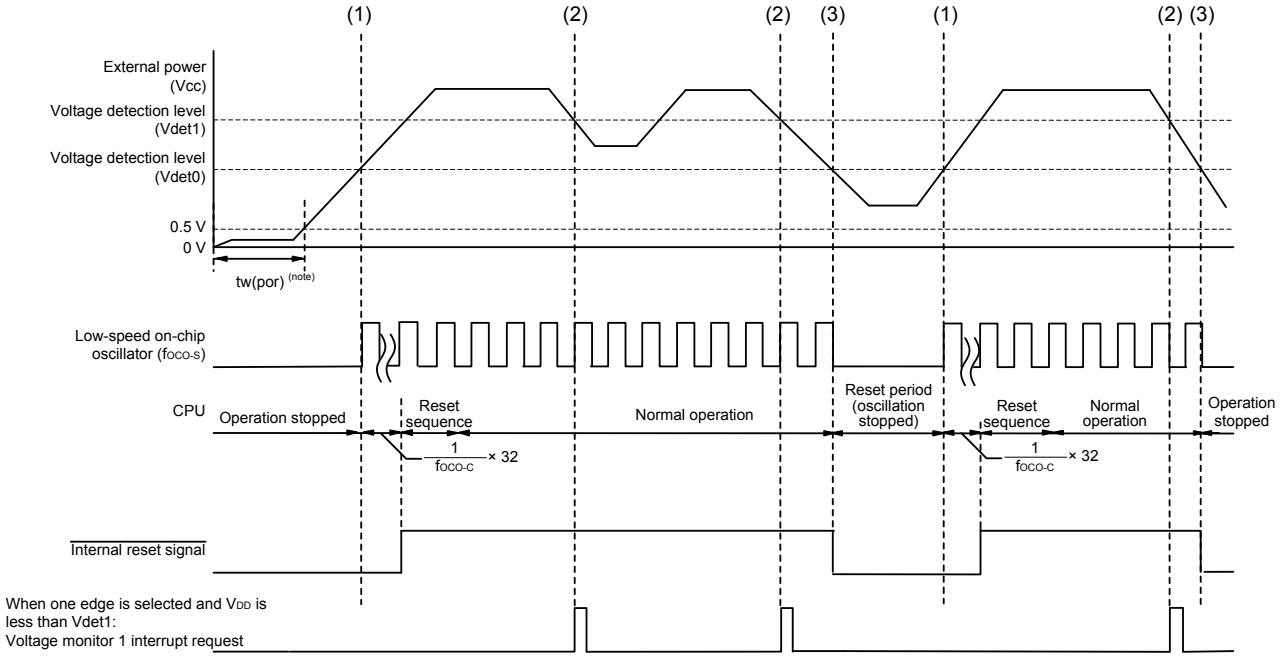
When the supply voltage reaches the interrupt detection voltage, an interrupt request is generated.

2.2.1 Interrupt & Reset Mode Operation Using the R8C/36M Group

Use a combination of voltage monitor 0 and 1, voltage monitor 0 and 2, or voltage monitor 0, 1, and 2 to enable the R8C/36M Group interrupt and reset mode operation.

Figure 2.1 shows the timing diagram when using voltage monitor 0 and 1.

(1) When the external power (V_{CC}) reaches the voltage detection level (Vdet0), the low-speed on-chip oscillator clock starts counting. When the count reaches 32, an internal reset signal is released at high level.
(2) When the external power (V_{CC}) falls below the voltage detection level (Vdet1), the voltage monitor 1 interrupt request is generated.
(3) When the external power (V_{CC}) falls below the voltage detection level (Vdet0), an internal reset signal is generated at low level.



Vdet0: Voltage monitor 0 detection voltage
Vdet1: Voltage monitor 1 detection voltage

Note: tw(por) indicates the duration the external power V_{CC} must be held below the valid edge (0.5 V) to enable a power-on reset. To turn on the power after it falls with voltage monitor 0 reset disabled, hold tw(por) for at least 1 ms.

Figure 2.1 Timing Diagram When Voltage Monitor 0 and Voltage Monitor 1 in the R8C/36M Group are Enabled

2.2.2 Interrupt & Reset Mode Operation Using RL78/G14

Figure 2.2 shows the timing diagram when the LVD is in interrupt & reset mode.

(1) When the supply voltage (V_{DD}) reaches the high-voltage detection level (V_{LVDH}), an internal reset signal is released at high level.
(2) When the supply voltage (V_{DD}) falls below the high-voltage detection level (V_{LVDH}), an interrupt request is generated (note).
(3) When the supply voltage (V_{DD}) falls below the low-voltage detection level (V_{LVDL}), an internal reset signal is generated at low level.

Note: When the LVD detects that the supply voltage (V_{DD}) falls below the high-voltage detection level (V_{LVDH}), the LVIMD bit in the LVIS register is automatically set to 1 (reset mode), and the LVILV bit in the LVIS register is automatically set to 1 (low-voltage detection level, V_{LVDL} or V_{LVD}). When the internal reset signal is not generated at high level, set the LVIMD bit in the LVIS register to 0 (interrupt mode) and the LVILV bit in the LVIMD register to 0 (high-voltage detection level, V_{LVDH}) by software.

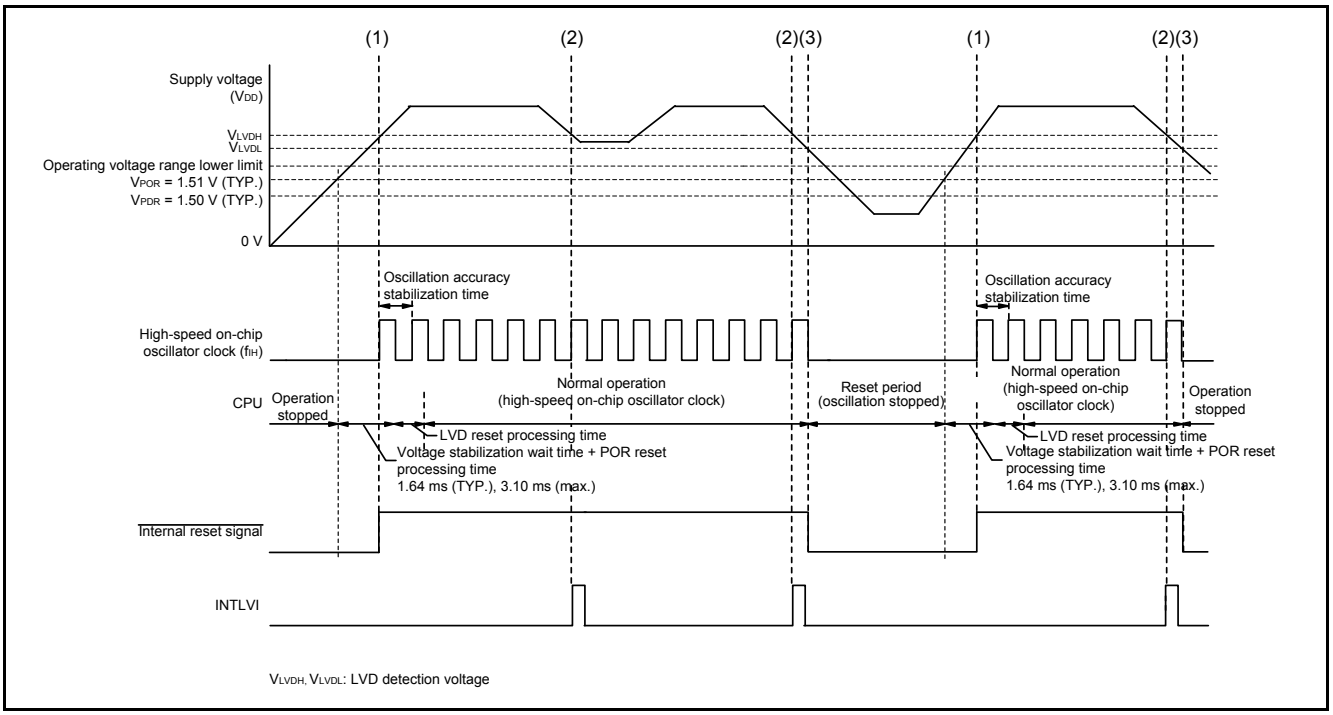


Figure 2.2 Timing Diagram When the RL78/G14 LVD is in Interrupt & Reset Mode

2.3 Reset Mode

In reset mode, the reset is released when the supply voltage rises to reach the detection voltage. When the supply voltage falls to reach the detection voltage, the reset is generated.

2.3.1 Reset Mode Operation Using the R8C/36M Group

Enable voltage monitor 0 to use the R8C/36M Group in reset mode.

Figure 2.3 shows the timing diagram when voltage monitor 0 is enabled.

(1) When the external supply (V_{CC}) reaches the voltage detection level (Vdet0), the low-speed on-chip oscillator clock starts counting. When the count reaches 32, an internal reset signal is released at high level.
(2) When the external power (V_{CC}) falls below the voltage detection level (Vdet0), an internal reset signal is generated at low level.

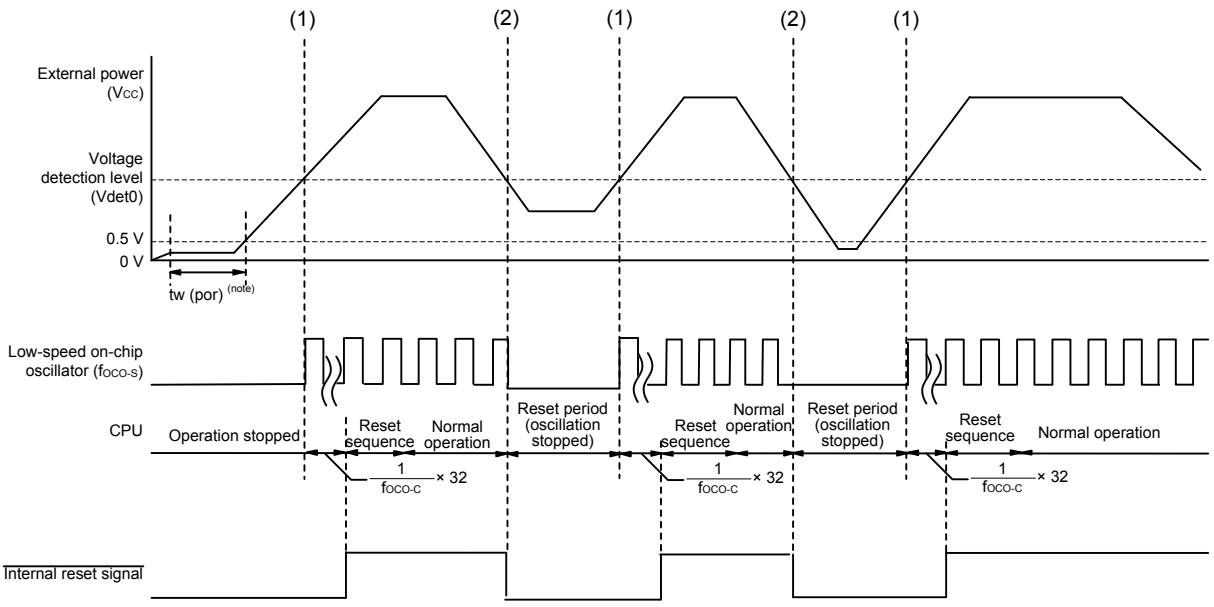


Figure 2.3 Timing Diagram When Voltage Monitor 0 in the R8C/36M Group is Enabled

2.3.2 Reset Mode Operation Using RL78/G14

Figure 2.4 shows the timing diagram when the RL78/G14 LVD is in reset mode.

(1) When the supply voltage (V_{DD}) reaches the LVD detection voltage (V_{LVD}), an internal reset signal is released at high level.
(2) When the supply voltage (V_{DD}) falls below the LVD detection voltage (V_{LVD}), an internal reset signal is generated at low level.

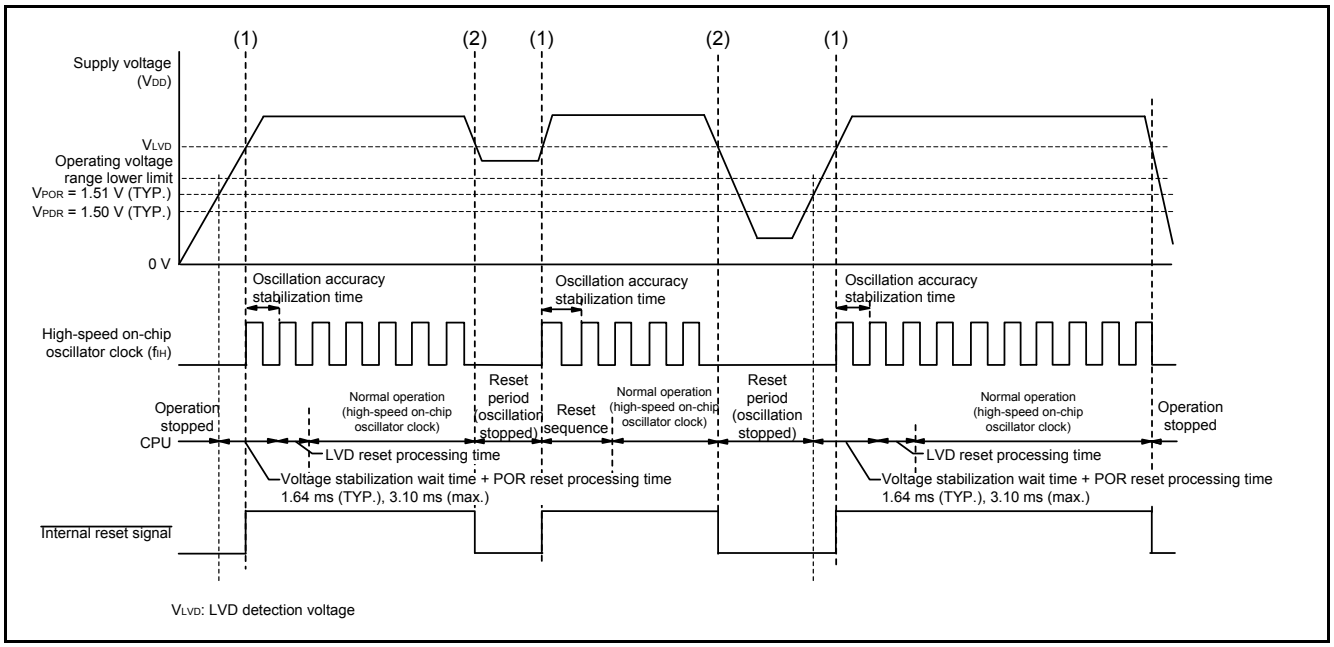


Figure 2.4 Timing Diagram When the RL78/G14 LVD is in Reset Mode

2.4 Interrupt Mode

In interrupt mode, an interrupt request is generated when the supply voltage reaches the detection voltage.

2.4.1 Interrupt Mode Operation Using the R8C/36M Group

Enable voltage monitor 1 or 2 to use the R8C/36M Group in reset mode.

This example uses the hardware reset. The POR cannot be used since voltage monitor 0 is not enabled.

Figure 2.5 shows the timing diagram when voltage monitor 1 is enabled.

(1) When the external supply (VCC) falls below the voltage detection level (Vdet1), the voltage monitor 1 interrupt request is generated.
(2) When the external supply (VCC) reaches the voltage detection level (Vdet1), the voltage monitor 1 interrupt request is generated.

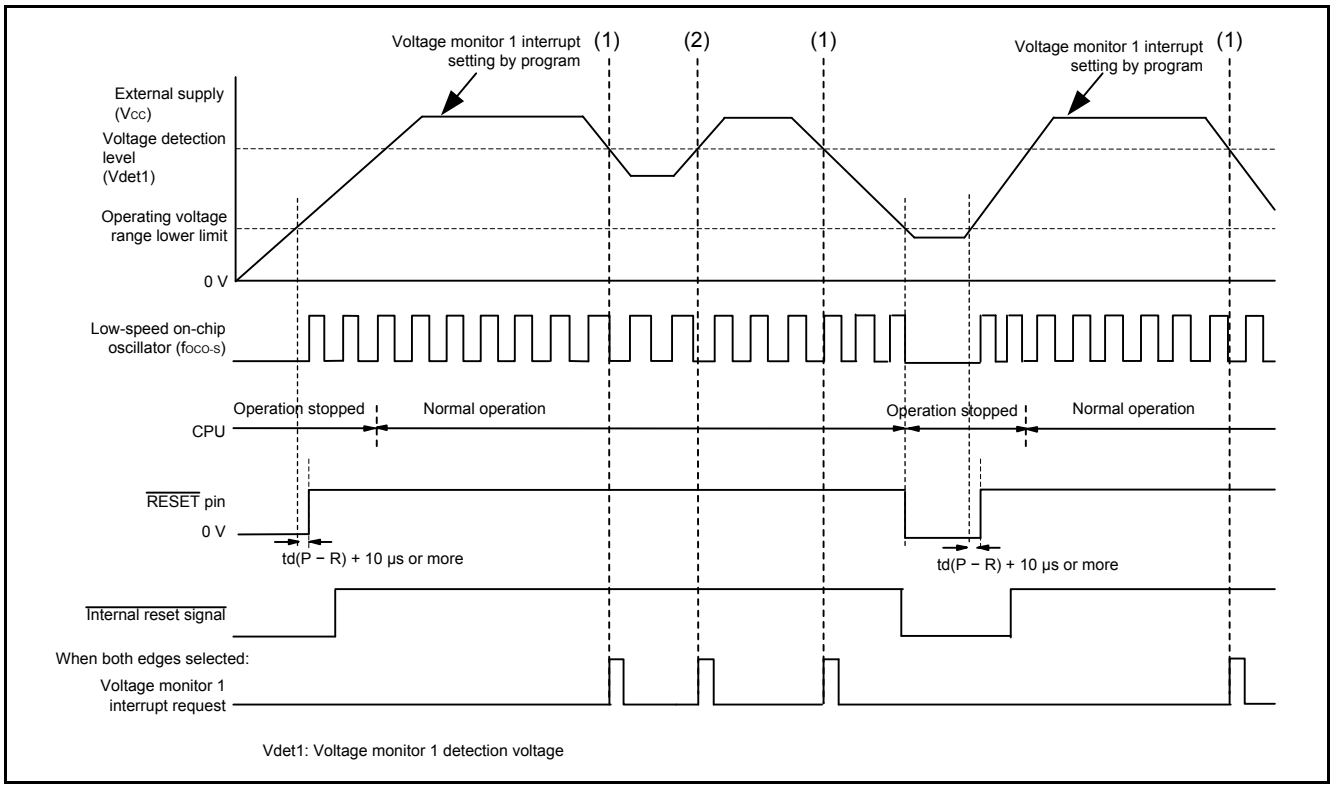


Figure 2.5 Timing Diagram When Voltage Monitor 1 in the R8C/36M Group is Enabled

2.4.2 Interrupt Mode Operation Using RL78/G14

This example uses the hardware reset. When the supply voltage (V_{DD}) passes through the LVD detection voltage (V_{LVD}), the voltage detection interrupt request is generated.

Figure 2.6 shows the timing diagram when the LVD is in interrupt mode.

(1) When the supply voltage (V_{DD}) falls below the LVD detection voltage (V_{LVD}), the voltage detection interrupt request is generated.
(2) When the supply voltage (V_{DD}) reaches the LVD detection voltage (V_{LVD}), the voltage detection interrupt request is generated.

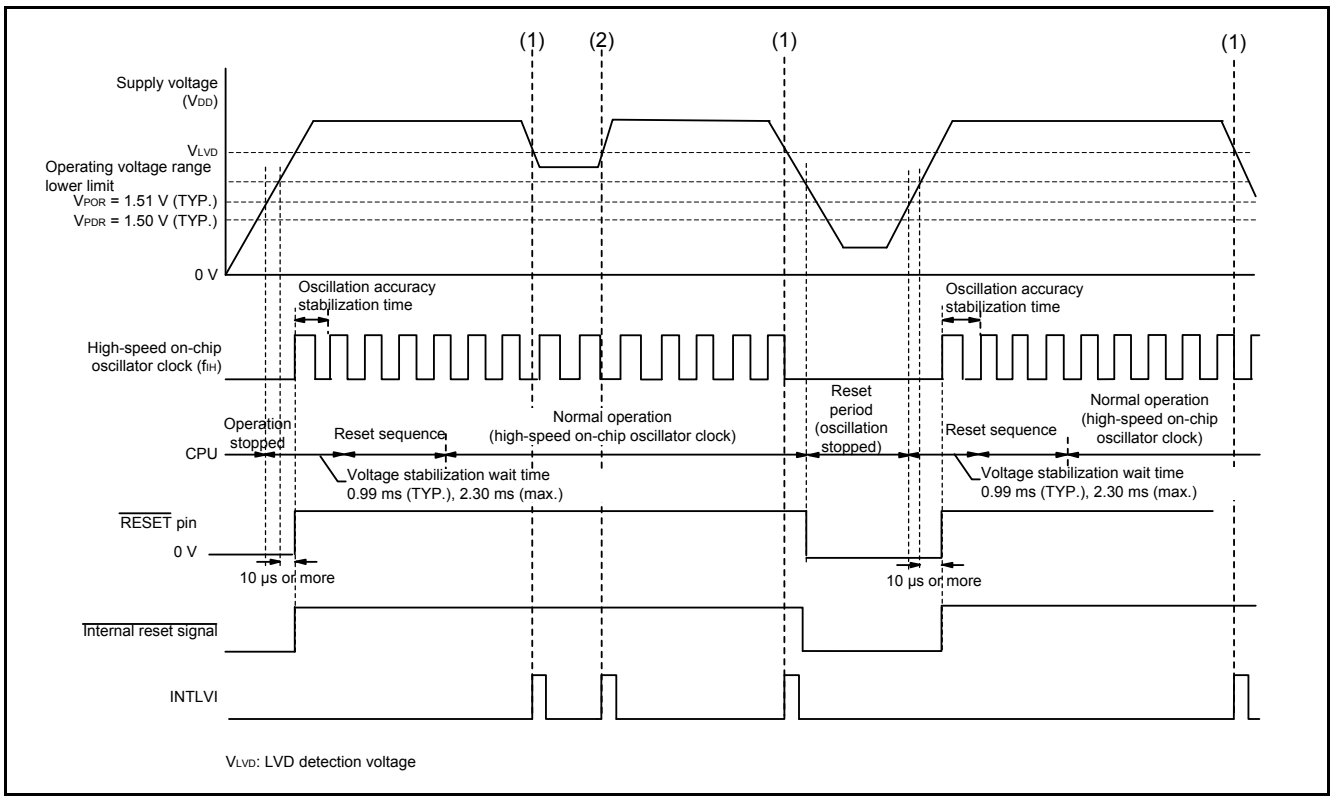


Figure 2.6 Timing Diagram When the RL78/G14 LVD is in Interrupt Mode

3. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware (R01UH0186EJ)

R8C/36M Group User's Manual: Hardware (R01UH0259EJ)

The latest versions can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Power-on Reset and Voltage Detector

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		Page	Summary
1.00	Feb. 14, 2014	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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