APPLICATION NOTE

RL78/G13 and RX62N/RX621

Digital Stethoscope Reference Design

R01AN0715EU0100
Rev.1.00
November 15, 2011

Introduction

The practice of ***auscultation*** (the **art** of listening to body sounds) has been used by physicians since the days of Hippocratic medicine. A stethoscope is used to transmit heart and lung sounds from chest wall to human ear. A digital stethoscope combines the simplicity of acoustic stethoscope with advanced electronics and information technology to facilitate better performance, recording of the heart and lung sounds and analysis of the recorded signals. It also sends the data to a computer either wirelessly or with a wired connection. Most of these stethoscopes are intended for observation and recording of heart sounds and murmurs as well as lung and airway sounds. There are other types of digital stethoscopes which can be used for monitoring heart and lung sounds during anesthesia and some even combine with synchronous ECG monitoring. Digital stethoscope is a good tool for medical education also. Heart sounds recorded with digital stethoscope can be visually observed and listened to. These recording can be used to build multimedia tools to improve the quality of physical exam and education.

By providing connectivity solutions either wired or wireless, a digital stethoscope can be used in telemedicine applications facilitating remote diagnosis by specialists. The recorded signals can further be spectrally analyzed and used for automated cardiac auscultation and interpretation.

Digital stethoscopes coupled to a lap top computer / tablet with suitable software and connected to internet for automated or remote diagnosis by a specialist, will be the future trend.

Contents

List of Figures

1. Digital Stethoscope

1.1 Theory of Operation

A stethoscope should be able to capture both high frequency and low frequency sounds from heart and lungs. In classical acoustic stethoscope the chest piece contains two parts, a diaphragm part provided by a stiff membrane and a bell part. When the diaphragm part is firmly applied, high frequency signals are picked up and bell part facilitates the capture of low frequency signals. The signal filtering action is facilitated by a specific shape and mechanical coupling to the chest wall.

A digital stethoscope has the following essential components to capture process and play back the heart sounds. The sounds are captured by a microphone built within the chest piece, with adjustable amplification and filtering. The electronic chest piece also allows for easy switching between diaphragm and bell modes. The captured audio signals can be processed by a microcontroller to eliminate artifacts and disturbances and can be stored locally or sent wirelessly to a computer. The processed signals will be played back by miniature speakers to the air tips for the physician.

Figure 1 Example of a Digital Stethoscope

The microcontroller in the digital stethoscope greatly improves the performance as well add many capabilities the instrument. It can facilitate the recording, display, printing of the signals locally and can use the connectivity solutions like USB, Wi-Fi and Zigbee to send data to a computer for further analysis and study of the signals. The micro controller can also facilitate the synchronous recording of the heart and lung sounds along with ECG signal to provide vital information for diagnostics. The recording of the data feature is very useful from the training purpose also.

The digital stethoscope receives signals of the amplitude of few millivolts in the frequency range of 20 Hz to 1000 Hz. The signal is further amplified and filtered before converting to digital samples. The sampling rate of the ADC should be at least 2 kHz to satisfy niquest criteria. In practice a sampling rate of 8 kHz is used. The sampled data can be recorded directly as raw data or can further be processed by micro controller using DSP techniques before recording. The processed signal will be reproduced by using DAC block of the microcontroller, which in turn filtered by a analog low pass filter before driving miniature speakers. The DSP techniques required to process the signals consist of digital filtering, scaling and frequency analysis.

Not all techniques can be done in real-time by the micro controller so the essential processing required for elimination of artifacts and disturbances before reconstructing the signal should be performed. This processing will be controlled by the user interface to improve the performance during auscultation.

1.2 Signal Processing

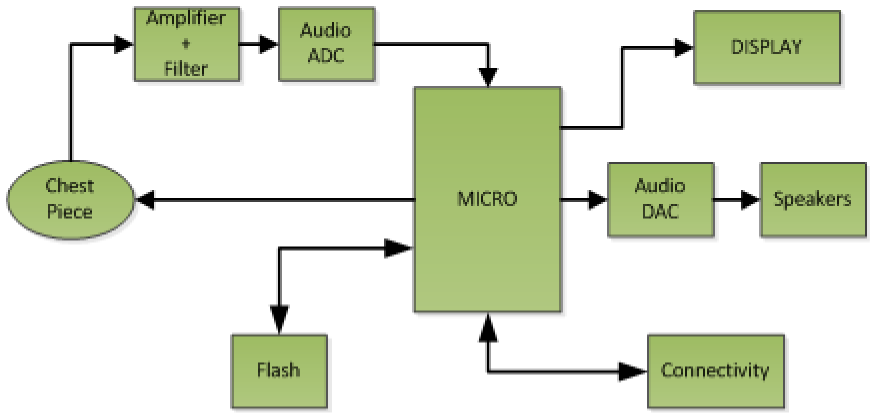

Figure 2 Signal Flow diagram of Digital Stethoscope

The main limitation of conventional stethoscopes is that the intensity of some body sounds is below the threshold of audibility. An electronic stethoscope overcomes this by electronically amplifying body sounds. Although electronic stethoscopes have many advantages, it suffers from noises because sound detection is achieved by a microphone which is sensitive to any sounds. So the signals picked by the microphone need to be processed to hear the useful heart and lung sounds using various signal processing techniques. The spectral intensity of heart sounds is shown in Figure 3.

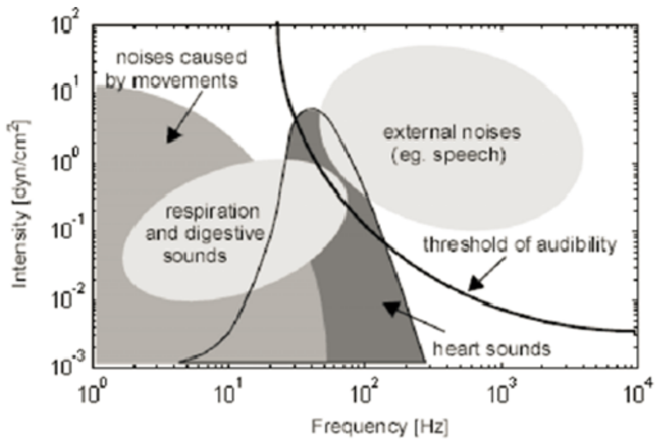

Figure 3 Spectral intensity of heart sound record [[3]

A number of filtering schemes with signal processing implemented in both analog and digital domains are described in the literature. They can be used to extract the useful information from the signal picked by the microphone. Newer techniques like adaptive filtering implemented using a low resource dsp microcontroller are published [[3]. These filtering schemes need to be implemented to process the signal in real-time assist the Physician.

There is an increasing need for automatic system capable of aiding the physician in the diagnosis of the heart condition by analyzing the sounds and murmurs present in the cardiac cycle. The signals captured by the chest piece are amplified and filtered by the analog electronics and digitized using Analog to digital converter before processing can be done by microcontroller. Simple digital stethoscope can process these signals in the digital domain and reproduce the enhanced signal through digital to analog converter and an audio filter to tiny speakers.

The input signal from the chest piece has amplitude in tens of millivolts in 20 Hz to 1000 Hz frequency range. This signal need to be amplified and low pass filtered before giving it to the ADC. The ADC can be a 8-12 bit. Various DSP algorithms can be used to process the raw signal to enhance it. The enhanced signal will be sent to a DAC for reproduction.

Many implementations for the signal processing are presented in the literature. One implementation uses Field Programmable Analog Array (FPAA) for analog part of the system. It contains analog modules to process two input channels and provide a conditioned analog signal to the AD converter for the digital processing unit. Each channel comprises three elements: a high pass filter, to remove the low frequencies recorded due mainly to muscle movements, a controlled gain stage and finally a low pass filter to remove the high frequencies due to ambient noise and interferences. The high pass filter is a second order filter and the low pass is a third order one. Both are based on Butterworth functions. These filters are necessary in the analog stage to have reliable signal information, although digital filters have been also used later in the digital stage. The controlled gain stage is indispensable since the amplitude of the sound acquired by the stethoscope is conditioned both by the patient physical shape and by the auscultation position [[4].

In another approach an oversampled filter bank technique is implemented on a low resource DSP system. The stethoscope incorporates multiple filtering modes as well as audio record and playback (full and half speed) functionality [[5].

1.3 System Description

A digital stethoscope with connectivity becomes a powerful tool when combined with signal processing software on a computer. There are many commercial software applications available which can process the sound signals captured by the digital stethoscope and assist physicians in diagnosing heart and lung problems. One example of signal processing software is shown in Figure 4 and another software which can detect heart murmur is shown in Figure 5. Most of the commercial software support Bluetooth or USB connectivity with digital stethoscope.

Figure 4 Example of commercial signal processing software running on a Laptop

Figure 5 Example of Heart Murmur Detection Software

1.4 Block Diagram of Digital Stethoscope

The block diagram for typical digital stethoscope is shown in Figure 6 and Figure 7. It consists of microcontroller capable of audio signal processing with necessary amplifier and filter hardware to process signals generated from the chest piece. In addition it needs to have an audio reproduction circuit to play back the processed audio signals. A connectivity solution is required to communicate and transfer the data to a computer for further offline processing.

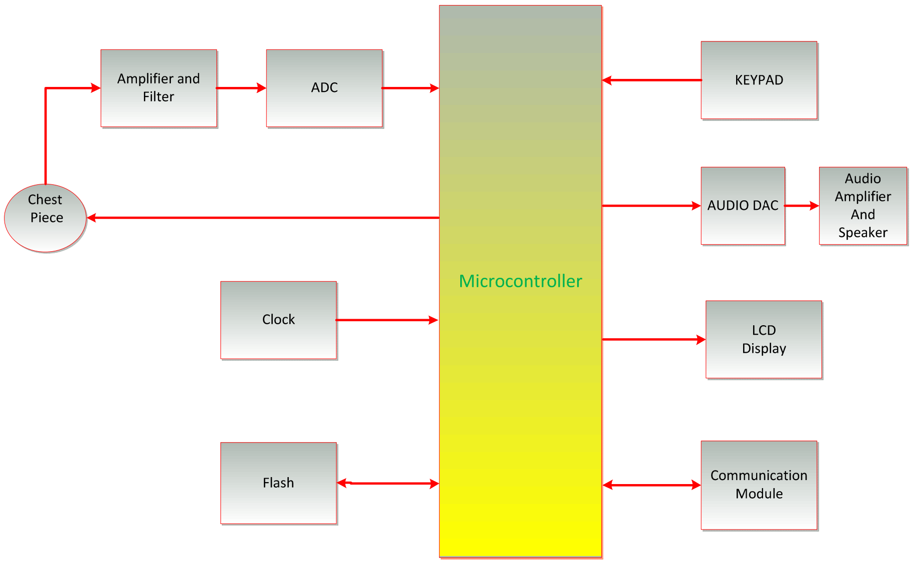

Figure 6 Block diagram of Simple Digital Stethoscope

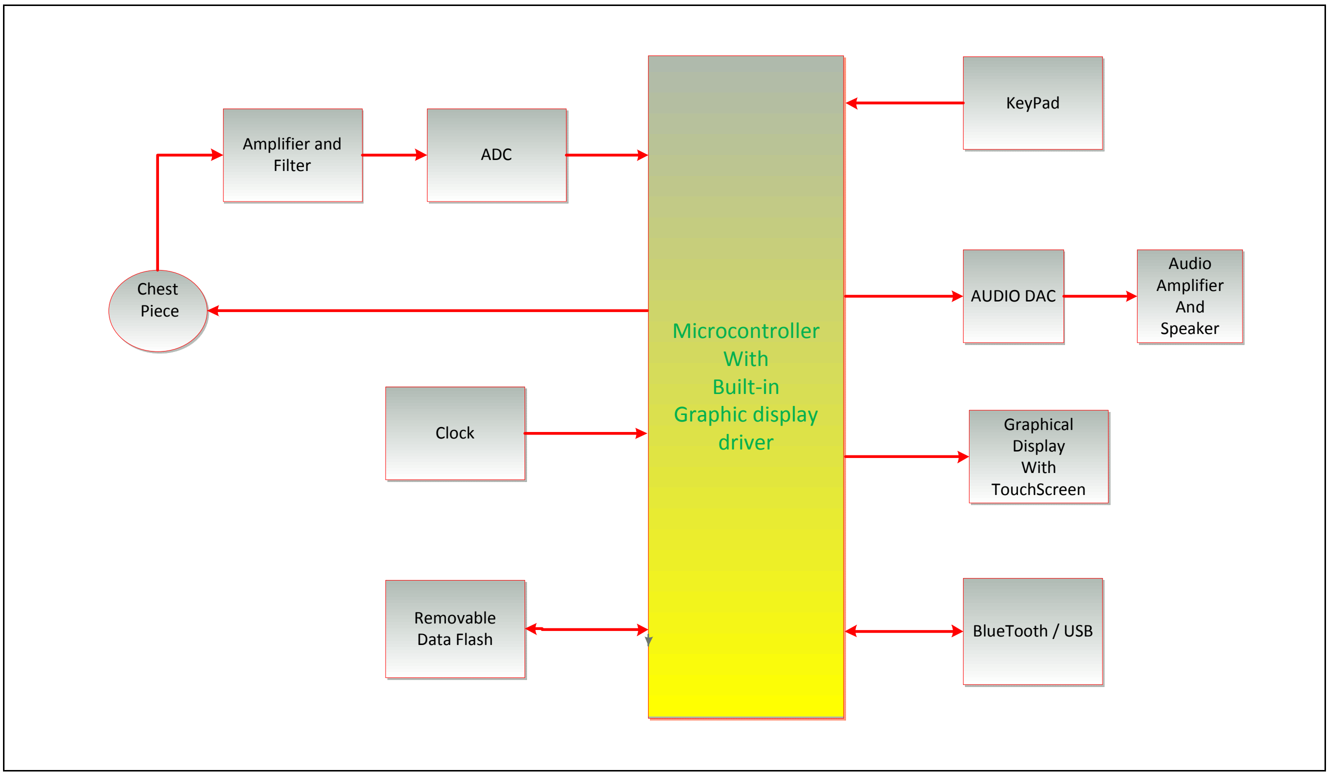

Figure 7 Block diagram of Digital Stethoscope with built in Graphic Display

2. Digital Stethoscope Requirements

2.1 Sensor requirements

The chest piece is required to capture both high frequency and low frequency signals from the heart and lungs. The mode should be physician selectable.

2.2 Signal Processing Requirements

One of the major problems with recording heart sounds is noise corruption. Various signal processing algorithms such as averaging, adaptive filtering and wavelet decomposition need to be used to remove certain types of noises using the microcontroller and the front end analog hardware. Selectable digital and analog filter combination should allow selective hearing of lung (high frequency) or heart sounds (low frequency) in the frequency spectrum.

2.3 Computational requirements

Microcontroller should be capable of implementing digital signal processing of audio signals from the chest sensor in real time. The Microcontroller should have built in LCD interface and touch keypad interface. For higher end models, the microcontroller should support floating point and digital signal functionality to process the signals in the device itself. It should be able to process the signals as well display them on a graphical display using built in display controller.

2.4 Storage requirements

An onboard non-volatile memory to store at least 120 secs of audio data is required. This data can be transferred to a computer using connectivity port or can be played back later by the Physician while making notes. For higher end models , a removable storage can be supported.

2.5 Display requirements

Digital stethoscope should have an easily readable local LCD display with user interface. This display will be used by user interface software to assist the user to configure measurement parameters, modes and show diagnostic information. For higher end stethoscope, a graphical display with touchpad is required. The display should support display of both pre and post processed signals for the physician.

2.6 Audio output requirements

The stethoscope should have an audio amplifier to reproduce the sound signal using tiny speaker or headphones. It should provide an adjustable volume control to allow physicians to hear a clear signal at a comfortable level, and permit auscultation of low-amplitude sounds in a noisy environment.

2.7 Power requirements

The stethoscope needs to be powered by battery for long term use. The battery can be a rechargeable or non-rechargeable alkaline or Lithium type. The hardware implementation should provide re-charge capability from a wall outlet and /or through USB port. For higher end models, the power can be provided from the mains to be able to supply the power required for the graphic display.

2.8 Communication requirements

Blue tooth is preferred communication channel required to transfer the real time secure data. Most of the commercial heart signal analysis software running on a PC or PDA uses Bluetooth to communicate to the digital stethoscope to get the data in real time. However an USB port with Continua ™ also can be used to communicate to the computer.

2.9 User interface requirements

An LCD display along with touch keypad will be required for the stethoscope. An optional audio output port should be available to connect to the PC sound card for stethoscopes without Bluetooth connection. For higher end models, elaborate user interface can be provided using the graphic display with touchscreen functionality.

2.10 Future Trends:

The future trend of the electronic stethoscope would be a multifunctional auscultatory device with graphical display, wireless data transmission, real-time signal processing for noise removal, and selectable frequency response. Microcontrollers should be able permit the incorporation of analysis software in to the stethoscope for heart sound analysis. For higher end models, all signal processing and display job is done locally by the microcontroller without the need of an external computer. The software can be enhanced to support various diagnostics and provide the physician with relevant data. These highly powerful microcontrollers help to make this device multifunctional.

3. Renesas RL78/G13 Device Specifications

3.1 Renesas RL78/G13 Device Architecture Overview

The following are some of the highlights of Renesas RL78/G13 device architecture.

- Minimum instruction execution time can be changed from high speed (0.03125 µs: @ 32 MHz operation with internal high-speed oscillation clock) to ultralow-speed (61 µs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits X 32 registers (8 bits X 8 registers X 4 banks)
- ROM: 16 to 512 KB, RAM: 1 to 32 KB, Data flash memory: −/4/8 KB
- On-chip internal high-speed oscillation clocks
- On-chip single-power-supply flash memory (with prohibition of chip erase/block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip multiplier and divider/multiply-accumulator
  - 16 bits × 16 bits = 32 bits (Unsigned or signed)
  - 32 bits ÷ 32 bits = 32 bits (Unsigned)
  - 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 16 to 120 (N-ch open drain: 0 to 4)
- Timer
  - 16-bit timer: 8 to 16 channels
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel
  - Interval timer: 1 channel
- Serial interface
  - CSI
  - UART/UART (LIN-bus supported)
  - I2C/Simplified I2C communication
- 8/10-bit resolution A/D converter (VDD = EVDD =1.6 to 5.5 V): 6 to 26 channels
- Power supply voltage: VDD = 1.6 to 5.5 V

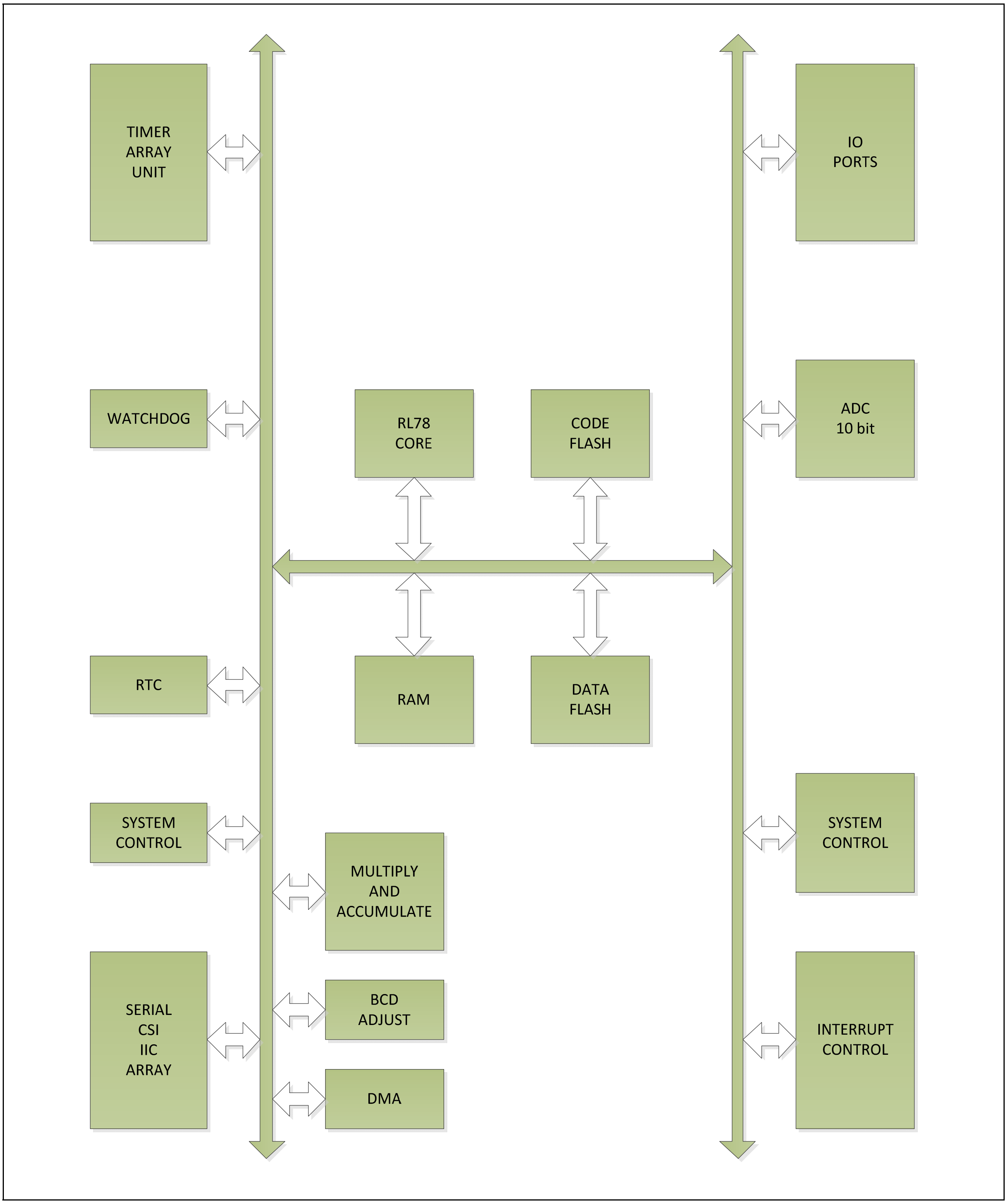

Figure 8 RL78/G13 Device Architecture Diagram

Processor

The processor core is 16 bit and supports 78K0R microcontroller instruction set.

Memory

RL78/G13 architecture can access a 1 MB memory space. It supports up to 32 KB of internal RAM. The internal RAM can be used as a data area and a program area where instructions are written and executed. The internal RAM is also used as a stack memory.

Flash Memory

The RL78/G13 incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board. The flash memory includes the "code flash memory", in which programs can be executed, and the "data flash memory", an area for storing data. RL78/G13 supports 16-64 KB of program flash and up to 8 KB of data flash. Data can be written to flash memory using any of the following methods.

- Writing to flash memory by using flash memory programmer
- Writing to flash memory by using external device (that Incorporates UART)
- Self-programming

The RL78/G13 supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person

Data Flash

The following are the main features of data flash supported in RL78/G13 architecture.

- The data flash memory can be written to by using the flash memory programmer, an external device, or through self- programming.
- Programming is performed in 8-bit units (half-word writing) and blocks can be deleted in 1 KB units.
- Because the data flash memory is an area exclusively used for data, it cannot be used to execute instructions (code fetching) and CPU can only access data flash in byte unit (needs four clock cycles)
- Instructions can be executed from the code flash memory while rewriting the data flash memory (That is, dual operation is supported)
- Accessing the data flash memory is not possible while rewriting the code flash memory (such as during self- programming)
- Because the data flash memory is stopped after a reset ends, the data flash control register (DFLCTL) must be set up in order to use the data flash memory
- Manipulating the DFLCTL register is not possible while rewriting the data flash memory

Timers

The timer array unit has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more "channels" can be used to create a high-accuracy timer. Timer array unit has the following functions. By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

1. Interval timer
   Each timer of a unit can be used as a reference timer that generates an interrupt (INTTM0n) at fixed intervals.
2. Square wave output
   A toggle operation is performed each time INTTM0n interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TO0n).
3. External event counter
   Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TI0n) has reached a specific value.
4. Divider function (channel 0 only)
   A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).
5. Input pulse interval measurement
   Counting is started by the valid edge of a pulse signal input to a timer input pin (TI0n). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.
6. Measurement of high-/low-level width of input signal
   Counting is started by a single edge of the signal input to the timer input pin (TI0n), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.
7. Delay counter
   Counting is started at the valid edge of the signal input to the timer input pin (TI0n), and an interrupt is generated after any delay period.

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

1. One-shot pulse output
   Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
2. PWM (Pulse Width Modulation) output
   Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.
3. Multiple PWM (Pulse Width Modulation) output
   By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

Ports

The RL78/G13 microcontrollers are provided with digital I/O ports, which enable variety of control operations. Pin I/O buffer power supplies depend on the product. The power supply can be VDD or EVDD0 or EVDD1 or EVDD1E. In addition to the function as digital I/O ports, these ports have several alternate functions.

Serial Interfaces

Serial array unit 0 has four serial channels, and serial array unit 1 has two. Each channel can achieve 3-wire serial (CSI), UART, and simplified I2C communication. Simplified I2C does not support slave mode, arbitration loss detection and wait detection

Clock Output/Buzzer Output Controller USB

Buzzer output is a function to output a square wave of buzzer frequency. One pin can be used to output a clock or buzzer sound. This can be used for adding audio alarm facility for the product.

BCD correction circuit

The result of addition/subtraction of the BCD (binary-coded decimal) code and BCD code can be obtained as BCD code with this circuit.

Multiplier And Divider/Multiply-Accumulator

The multiplier and divider/multiply-accumulator has the following functions.

- 16 bits × 16 bits = 32 bits (Unsigned)
- 16 bits × 16 bits = 32 bits (Signed)
- 16 bits × 16 bits + 32 bits = 32 bits (Unsigned)
- 16 bits × 16 bits + 32 bits = 32 bits (Signed)
- 32 bits ÷ 32 bits = 32 bits, 32-bits remainder (Unsigned)

4. Renesas RX62N/RX621 Device Specifications

4.1 Renesas RX62N/RX621 Device Architecture Overview

The following are some of the highlights of Renesas RX62N/RX621 device architecture.

32-bit RX CPU Core

- Delivers 165 DMIPS at a maximum operating frequency of 100 MHz
- Single Precision 32-bit IEEE-754 Floating Point
- Accumulator: 32 × 32 to 64-bit result, one instruction
- Mult/Divide Unit, 32 × 32 Multiply in one CPU clock for multiple instructions
- Interrupt response in as few as 5 CPU clock cycles
- CISC-Harvard Architecture with 5-stage pipeline
- Variable length instructions, ultra compact code
- Supports the Memory Protection Unit (MPU)
- Background JTAG debug plus high-speed trace

Low Power Design and Architecture

- 2.7V to 3.6V operation from a single supply
- 480 µA/MHz Run Mode with all peripherals on
- Deep Software Standby Mode with RTC
- Four low power modes

Main Flash Memory, no Wait-State

- 100 MHz operation, 10 nS read cycle and No wait states for read at full CPU speed
- 256K, 384K, 512K Byte size options
- For Instructions or Operands
- Programming from USB, SCI, JTAG, user code

Data Flash Memory

- Up to 32K Bytes with 30K Erase Cycles, Background Erase/Program does not stall CPU

SRAM, no Wait-State

- 64K or 96K Byte size options , For Operands or Instructions
- Back-up retention in Deep Software Standby Mode

DMA

- Four fully programmable internal DMA channels
- Two EXDMA channels for external-to-external transfers
- Data Transfer Controller (DTC)

Reset and Supply Management

- Power-On Reset (POR) monitor/generator
- Low Voltage Detect (LVD) with precision setting

System Clocking with Clock Monitoring

- External crystal, 8 MHz to 14 MHz to Internal PLL
- PLL source to system, USB, and Ethernet
- Internal 125 kHz LOCO for IWDT
- External crystal, 32 kHz for RTC

Real Time Clock

- Full calendar function, BCD format

Two Independent Watchdog Timers

- 125-kHz LOCO operation

Up to 14 Communication Interfaces

- (2) USB 2.0 Full-Speed interfaces with PHY
- Supports Host/Function/OTG
- 10 endpoints for types: Control, Interrupt, Bulk, Isochronous
- (1) Ethernet MAC 10/100 Mbps, Half or Full Duplex Supported.
- Dedicated DMA with 2-Kbyte transmit and receive FIFOs.
- RMII or MII interface to external PHY
- (1) CAN ISO11898-1, supports 32 mailboxes
- (6) SCI channels: Asynchronous, clock sync, smartcard, and 9-bit modes
- (2) I2C interfaces up to 1M bps, SMBus support
- (2) RSPI

External Address Space

- Eight CS areas (8 × 16 Mbytes), 8-/16-/32-bit bus space selectable for each area
- 128-Mbyte SDRAM area

TFT-LCD up to WQVGA resolution

Up to 20 Extended Function Timers

- (12) 16-bit MTU2 --Input capture, Output Compare, PWM output, phase count mode
- (4) 8-bit TMR and (4) 16-bit CMT

1-MHz ADC units with two combination choices

- 12-bit × 8 ch. unit with single sample/hold circuit
- or (2) 10-bit × 4 ch units each with a sample/hold circuit
- AD-converted value addition mode (12-bit A/D converter)

10-bit DAC, 2 channels

Up to 128 GPIO

- 5V tolerant, Open-Drain, Internal Pull-up

Operation Temp

- –40°C to +85°C

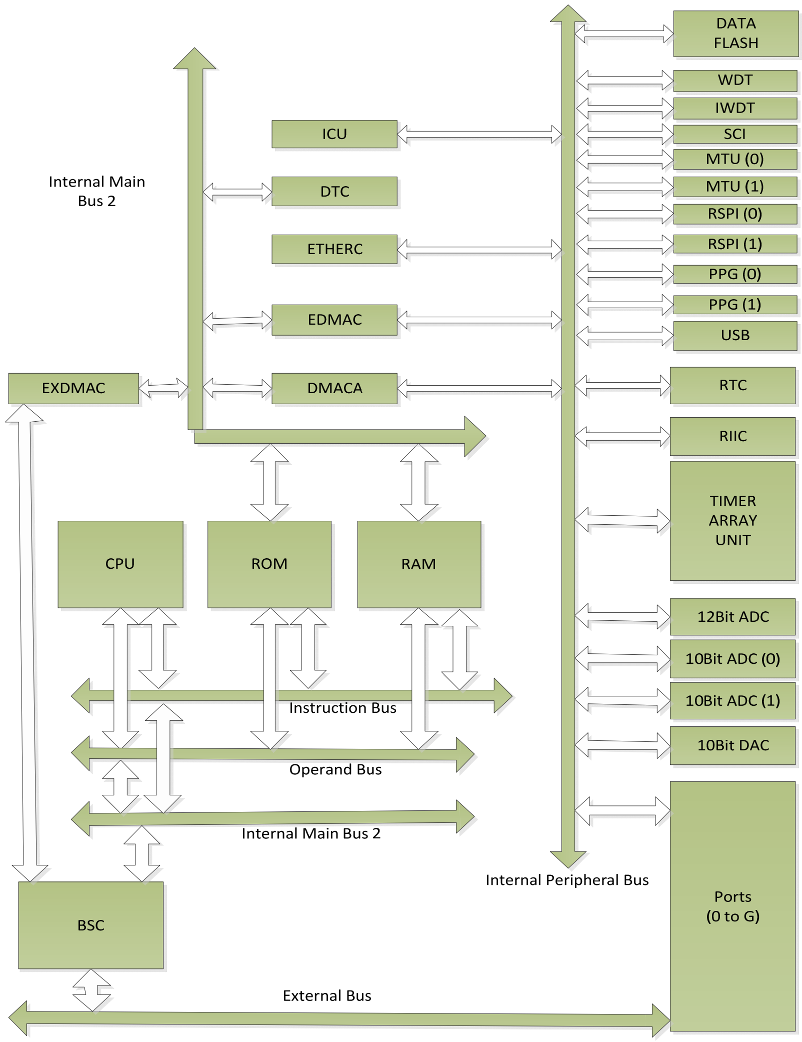

Figure 9 RX62N/RX621 Device Architecture Diagram

5. Reference Design Architecture

Table 1 Requirements Table

Digital Stethoscope Requirements	Relevance	Renesas Device RL78/G13	Required External Hardware	Renesas Device RX62N/RX621	Required External Hardware
Amplifier	Medium	None	External	None	External
Analog Filter	Low	None	External	None	External
Audio ADC	High	Internal 10 bit ADC		Internal 12 bit ADC	
Digital signal Processing	High	Hardware MAC		Hardware MAC and Floating point support	
Audio DAC	High	None	External	Internal 10 bit DAC	
Audio Amplifier	Low	None	External	None	External
USB	Low	None (Future Planned)	External	Internal USB Function	
Wireless Connectivity	High	None	External	None	External
LCD Controller	High	None	External	TFT-LCD with WQVGA	
Data Flash	High	Available		Available	
Low power Operation	High	Yes		Yes	

5.1 Hardware Architecture

A proposed implementation of Digital stethoscope using RL78/G13 device is shown in Figure 10. It consists of an amplifier and filter circuit to process the signals generated by the chest piece before being digitized by the RL78/G13 device for further processing by the software. An audio play back circuit which can reproduce the processed audio signals for the physician is on-board. The digital stethoscope also has connectivity solution (either USB or Wireless). A large custom LCD display is used to display user interface data.

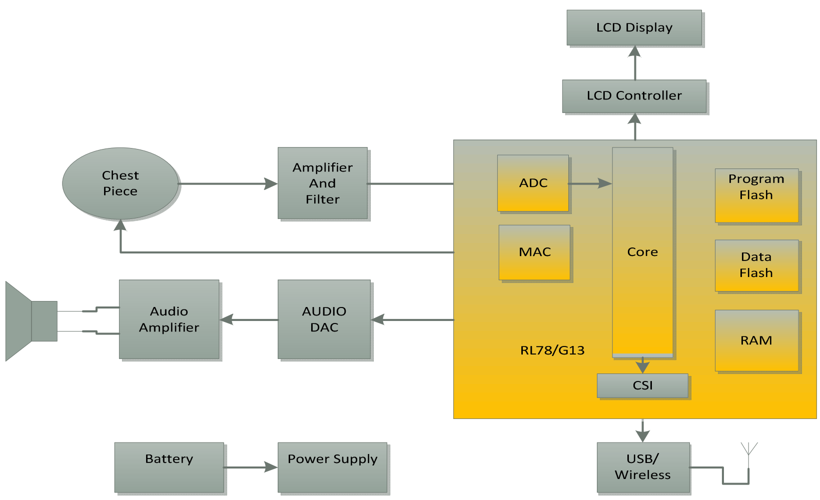

Figure 10 Hardware Implementation Diagram for simple digital stethoscope

An implementation of High end Digital Stethoscope using RX62N/RX621 device is shown in Figure 11. This supports enhanced analog interface with a 12 bit ADC along with standard amplifier and filter circuits. The microcontroller with built in floating point unit can process the signals. With the graphics controller hardware, it can display both pre and post processed signals. In addition the graphical display can have a touch screen which greatly enhances user interface.

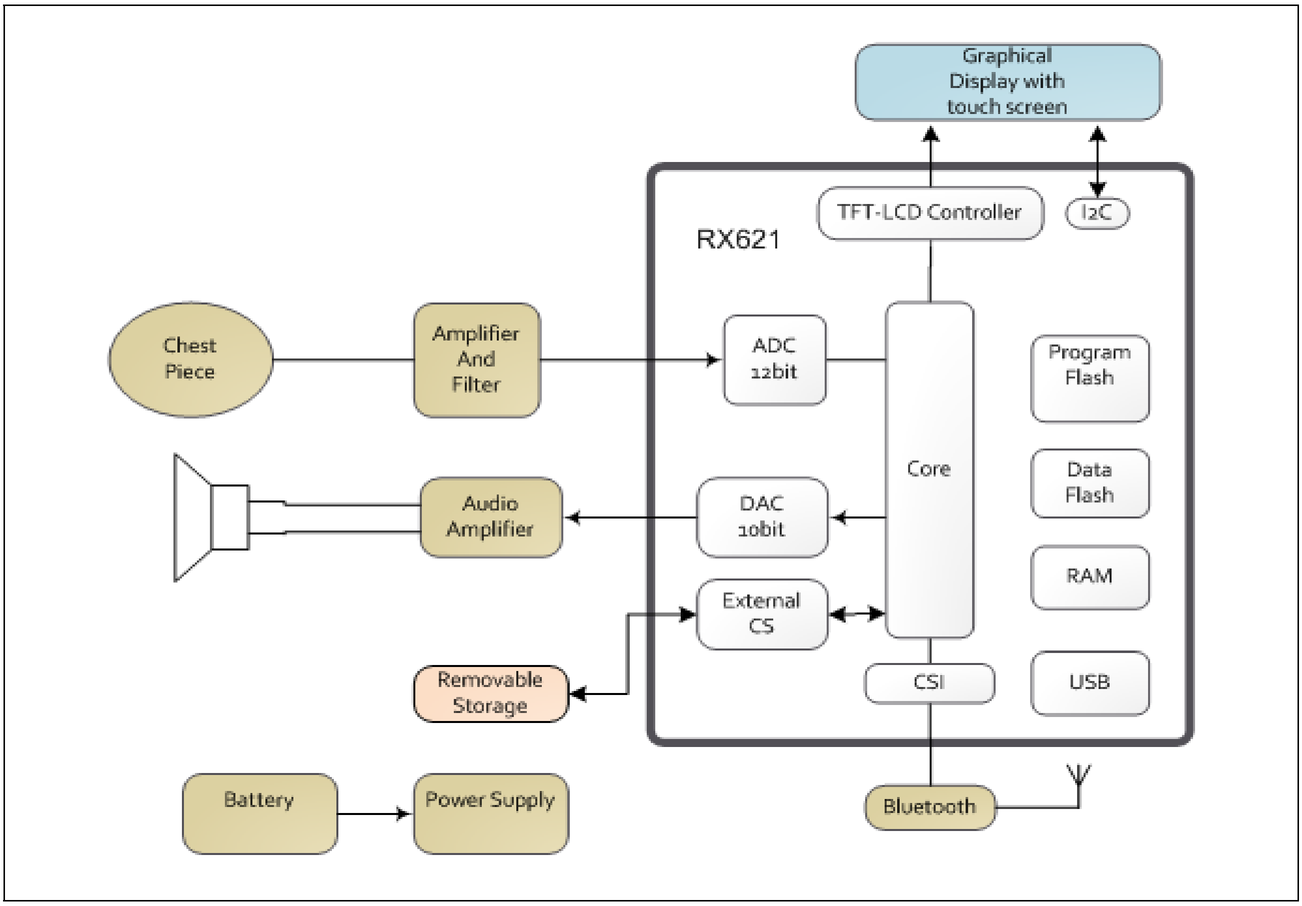

Figure 11 Hardware Implementation Diagram with Graphical Display

5.2 Software Architecture

Digital stethoscope firmware architecture is shown in Figure 12. It comprises of various device drivers to communicate with hardware to control them, signal processing and data archiving firmware and user interface firmware for display and taking the user inputs. In addition, communication software will take care of device connectivity and data transfer functionality. The firmware can be implemented without the need of an embedded operating system by using interrupt driven mechanism. Since RL78/G13 supports hardware MAC functionality, fast signal processing software can be implemented. For advanced models using RX62N/RX621 devices, drivers for Graphical display and touch screen are required. In addition all the signal processing should be accomplished locally and display the waveforms and data on the graphical display. Touch screen enables an enhanced User interface implementation. As the device has integrated USB function, it will be used to enable Continua™ support.

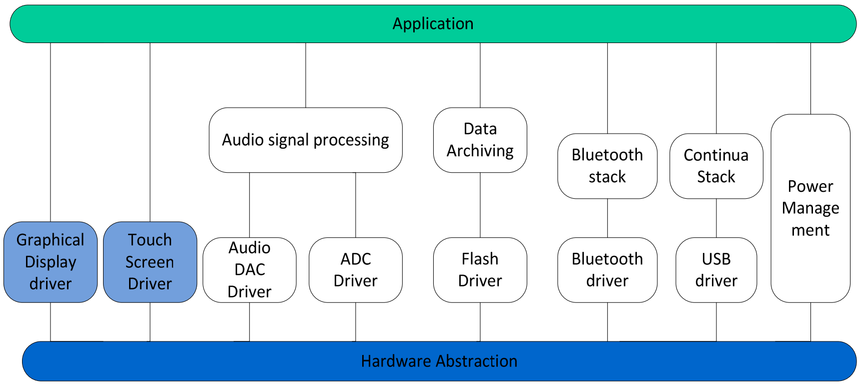

Figure 12 Software Architecture

6. High Level Software Flow Charts

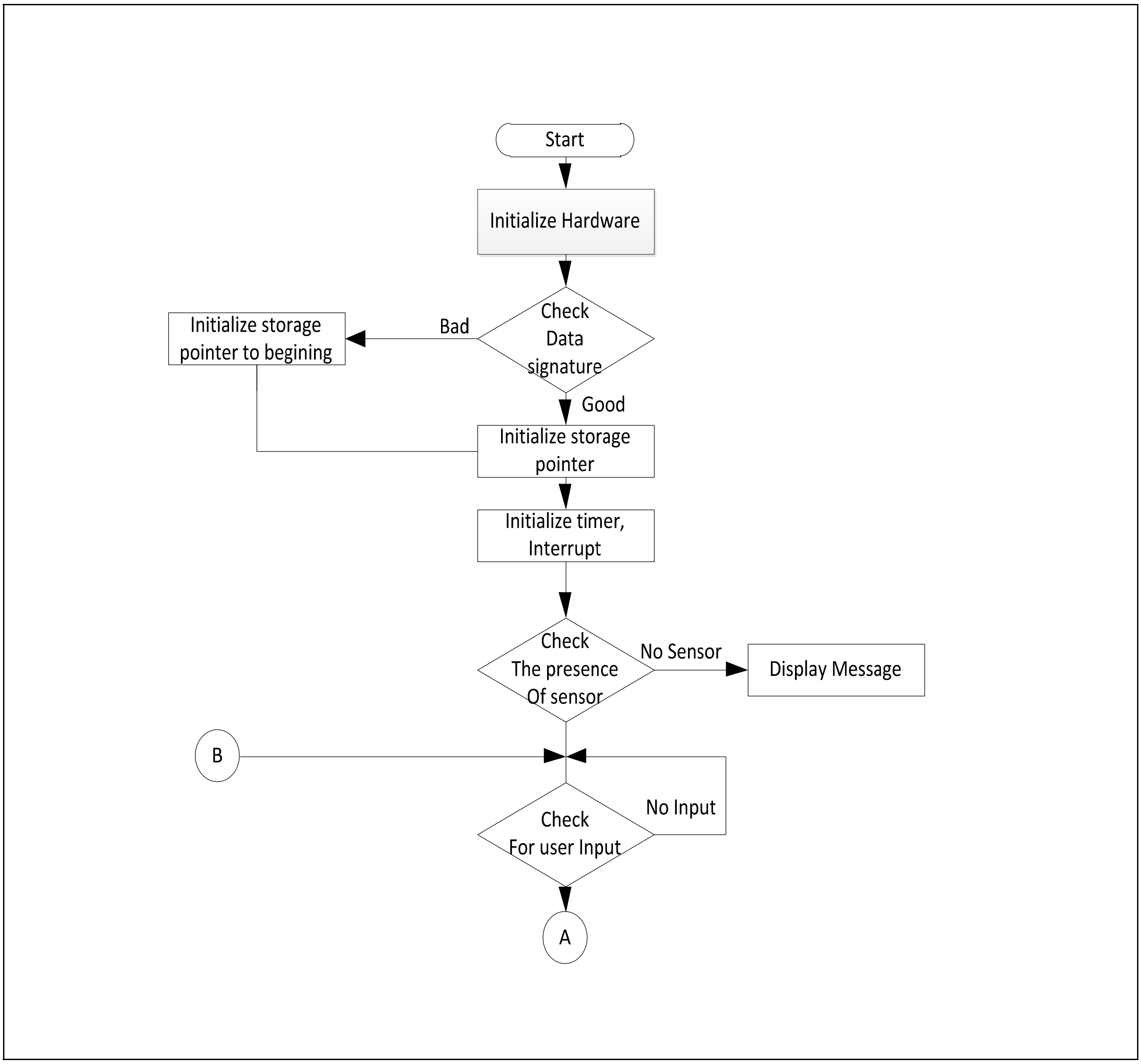

Figure 13 Main program Flowchart for Digital Stethoscope (1)

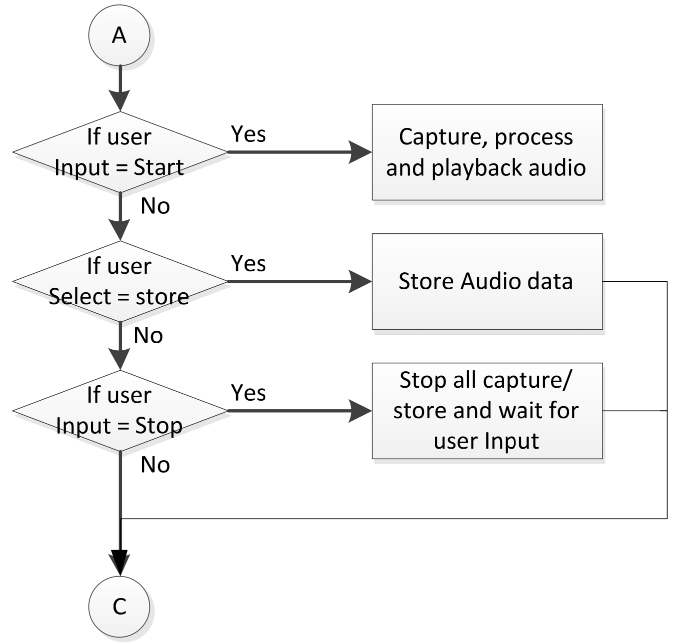

Figure 14 Main program Flowchart for Digital Stethoscope (2)

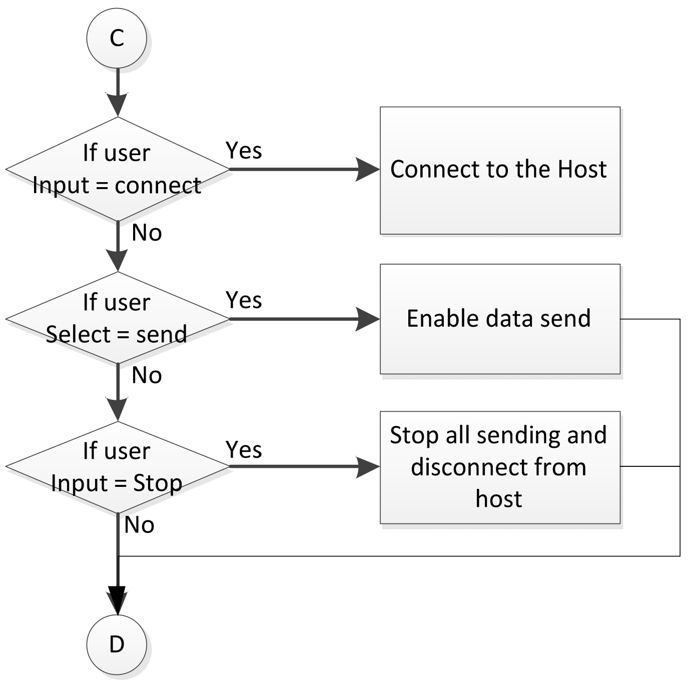

Figure 15 Main program Flowchart for Digital Stethoscope (3)

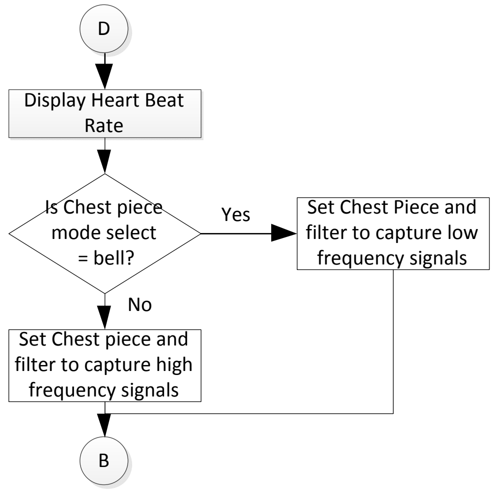

Figure 16 Main program Flowchart for Digital Stethoscope (4)

Appendix A - References

[1] Yuan-ting Zhang, Gregory Chan, Xin-Yu Zhang, Lung Yip, " Heart sounds and stethoscopes", in *Encyclopedia of Biomedical Engineering*, Vol. 3, Wiley- Interscience, 2006, pp. 1826-1834.

[2] Herman Vermarien,"Phono cardiography", in Encyclopedia of Medical Devices and Instrumentation, Second edition, Vol 5, Wiley-Interscience, 2006, pp. 288-289.

[3] N.Jatupaiboon, S. Pan-ngum and P. Israsena, Electronic Stethoscope Prototype with Adaptive Noise Cancellation, Eighth International Conference on ICT and Knowledge Engineering, 2010,Bangkok, Thailand, November 24-25, 2010

[4] Ginés *Doménech-Asensi, Juan Martínez-Alajarín, Ramón Ruiz-Merino, José A. López-AlcantudW.*, Synthesis on FPAA of a Smart Stethoscope Analog subsystem, International conference on Field Programmable Logic and Applications (FPL), 2007 Amesterdam, Netherlands, 27-29 August, 2007

[5] Julie Johnson, David Hermann, Melody Witter, Etienne Cornu, Robert Brennan and Alain Dufaux, An ultra-low power subband-based Electronic Stethoscope, ICASSP 2006 Proceedings, IEEE International conference on Acoustics, Speech and Signal Processing, 2006, Toulouse, France, Date:14-19 May, 2006

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision Record

Rev.	Date	Description: Page	Description: Summary
1.00	November 15, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.1