

# RL78/G13, 78K0/Kx2

## Migration Guide from 78K0 to RL78: Option byte

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### Introduction

This application note describes how to migrate the option byte functions from the 78K0/Kx2 to the RL78/G13.

### Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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## 1. Differences in Function Overview

Table 1.1 summarizes the differences between the option byte functions of the 78K0/Kx2 and the RL78/G13.

Table 1.1 Differences

Item	78K0/Kx2	RL78/G13
Function	<ul style="list-style-type: none"> <li>• Watchdog timer setting (Including Internal low-speed oscillator setting)</li> <li>• power-on-clear circuit (POC) setting</li> <li>• On-chip debug operation setting</li> </ul>	<ul style="list-style-type: none"> <li>• Setting of watchdog timer operation</li> <li>• Setting of LVD operation mode</li> <li>• On-chip debug operation setting</li> <li>• Setting of the frequency of the high-speed on-chip oscillator</li> <li>• Setting of flash operation mode</li> </ul>
Address	0080H - 0084H, 1080H - 1084H (Note1)	000C0H - 000C3H, 010C0H - 010C3H (Note1)
Reserved area	0082H - 0083H, 1082H - 1083H (Note1)	None
Setting method	Self-programming, Dedicated flash memory programmer	Self-programming, Dedicated flash memory programmer, Serial programming using external device (UART communication)
Internal low-speed oscillator	Internal low-speed oscillator operation can be stopped by software. ( $f_{RL} = 240$ kHz typ.)	Low-speed on-chip oscillator operation ( $f_{IL} = 15$ kHz typ.) cannot be stopped. Watchdog timer counter operation can be stopped in HALT/STOP mode.
POC (Note2)	The voltage for release from the reset state after power on can be selected from 2.7 V typ. and 1.59 V typ.	The voltage ( $V_{LVD}$ ) for release from the reset state after power on can be selected from 14 levels. Rising edge : 1.70~4.14V (Max.) Falling edge : 1.60~3.90V (Min.)
Interval interrupt of watchdog timer	None	Interval interrupt is generated when 75% + $1/2f_{IL}$ of the overflow time is reached.
Select internal high-speed oscillation clock frequency	8.0MHz (TYP.) only	FRQSEL3 = 1 32MHz, 16MHz, 8MHz, 4MHz, 2MHz, 1MHz (TYP.) FRQSEL3 = 0 24MHz, 12MHz, 6MHz, 3MHz (TYP.)
Setting of flash operation mode	No	Yes
Setting of on-chip debug operation	Yes (uPD78F05xxD, 78F05xxDA only)	Yes

Note1. When the boot swap operation is used.

Note2. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming.

## 2. Option byte Compatibilities

Table 2.1 shows the compatibilities of the option byte between the 78K0/Kx2 and the RL78/G13.

Table 2.1 Option byte Compatibilities

Item	78K0/Kx2	RL78/G13
Watchdog timer window open period setting	Address:0080H / 1080H <sup>(Note1)</sup> WINDOW1 bit, WINDOW0 bit	Address:000C0H / 010C0H <sup>(Note1)</sup> WINDOW1 bit, WINDOW0 bit
Operation control of watchdog timer counter	Address:0080H / 1080H <sup>(Note1)</sup> WDTON bit	Address:000C0H / 010C0H <sup>(Note1)</sup> WDTON bit
Watchdog timer overflow time	Address:0080H / 1080H <sup>(Note1)</sup> WDCS2 to WDCS0 bit	Address:000C0H / 010C0H <sup>(Note1)</sup> WDCS2 to WDCS0 bit
Internal low-speed oscillator operation	Address:0080H / 1080H <sup>(Note1)</sup> LSROSC bit	No
Operation control of watchdog timer counter (HALT/STOP mode)	No	Address:000C0H / 010C0H <sup>(Note1)</sup> WDSTBYON bit
Use of interval interrupt of watchdog timer	No	Address:000C0H / 010C0H <sup>(Note1)</sup> WDTINT bit
POC mode selection	Address:0081H / 1081H <sup>(Note1)</sup> POCMODE bit <sup>(Note2)</sup>	No
LVD setting	No	Address:000C1H / 010C1H <sup>(Note1)</sup> VPOC2 to VPOC0 bit, LVIS1 bit, LVIS0 bit, LVIMDS1 bit, LVIMDS0 bit
Setting of the frequency of the high-speed on-chip oscillator	No	Address:000C2H / 010C2H <sup>(Note1)</sup> FRQSEL3 to FRQSEL0 bit
Setting of flash operation mode	No	Address:000C2H / 010C2H <sup>(Note1)</sup> CMODE1 bit, CMODE0 bit
Control of on-chip debug operation	Address:0084H / 1084H <sup>(Note1)</sup> OCDEN1 bit, OCDEN0 bit	Address:000C3H / 010C3H <sup>(Note1)</sup> OCDENSET bit, OCDERSD bit

Note1. When the boot swap operation is used.

Note2. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming.

### 3. Reference Documents

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

### Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 29, 2019.	-	First edition issued

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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