RL78/G10

Timer Array Unit (Interval Timer) CC-RL

Introduction

This application note describes the interval timer function of the timer array unit (TAU). This unit inverts the LED indication each time a timer interrupt occurs. Also, it changes the timer interrupt cycle time based on the number of times the switch is pressed.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

RENESAS

1. Specifications

This application note shows example settings for using timer interrupts (INTTM00) from the interval timer and interrupts (INTP0) generated on pin input edge detection. The TAU inverts the LED indication each time a timer interrupt (INTTM00) occurs 250 times. Also, this unit changes the timer interrupt (INTTM00) cycle time based on the number of times the switch (SW) is pressed.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 shows the outline of timer operation and its interrupts.

Table 1.1   Peripheral Functions to be Used and their Uses

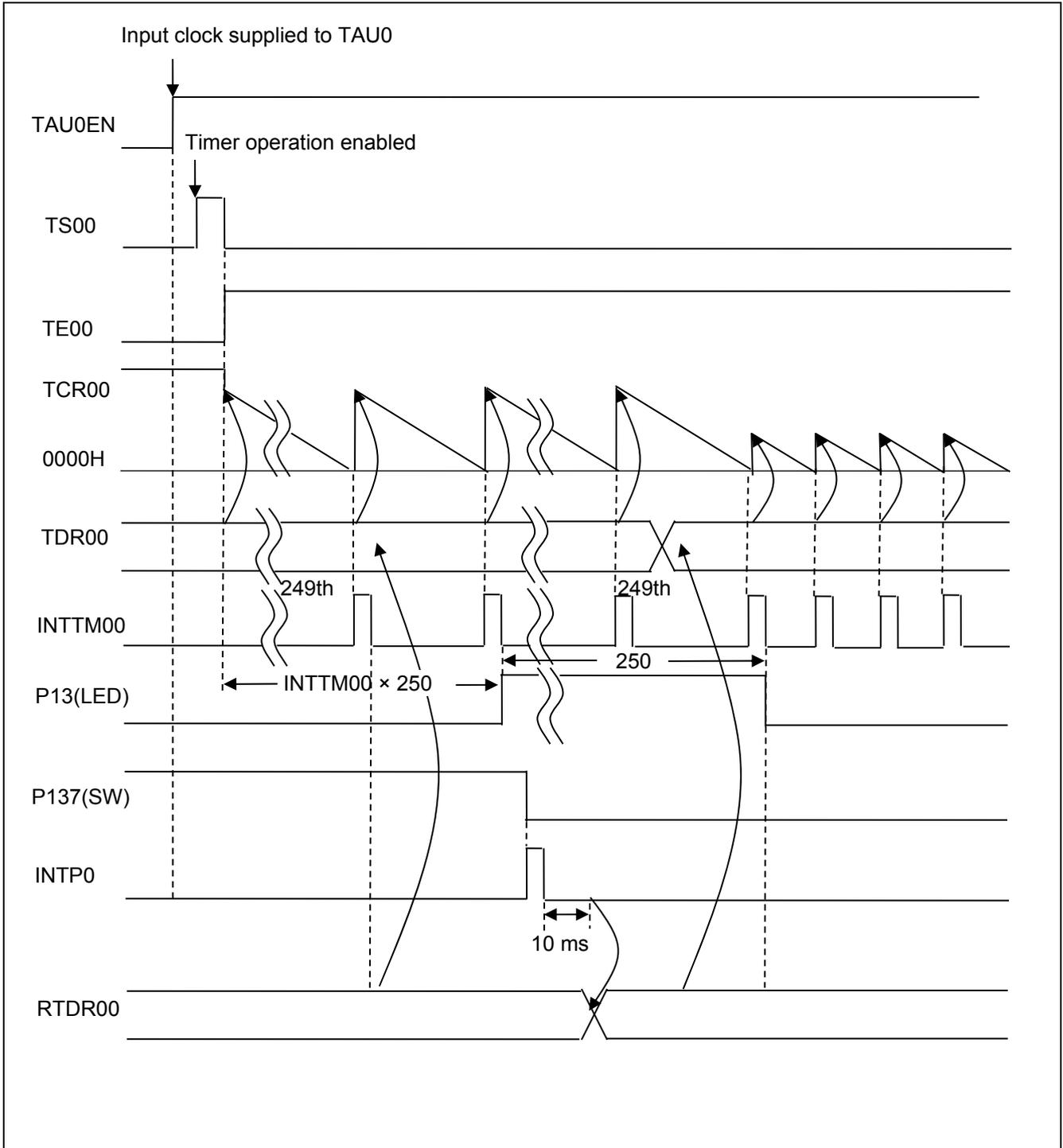| Peripheral Function	Use
Timer array unit 0 (channel 0)	Time interval control for inversion of the P13 pin output (LED indication)
P00	Output port for LED indications
P137/INTP0	Switch input for changing the timer interrupt (INTTM00) cycle time

Figure 1.1   Outline of Timer Operation and Interrupts

2.   Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1   Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10YASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 20 MHz • CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 to 5.5 V.) SPOR detection voltage: Falling edge: VDD < 2.84V Rising edge: VDD >= 2.90V
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e² studio)	e² studio V4.0.2.008 from Renesas Electronics Corp.
Assembler (e² studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

3.   Related Application Note

The application note that is related to this application note is listed below for reference.

RL78/G10 Initialization CC-RL (R01AN2668E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.
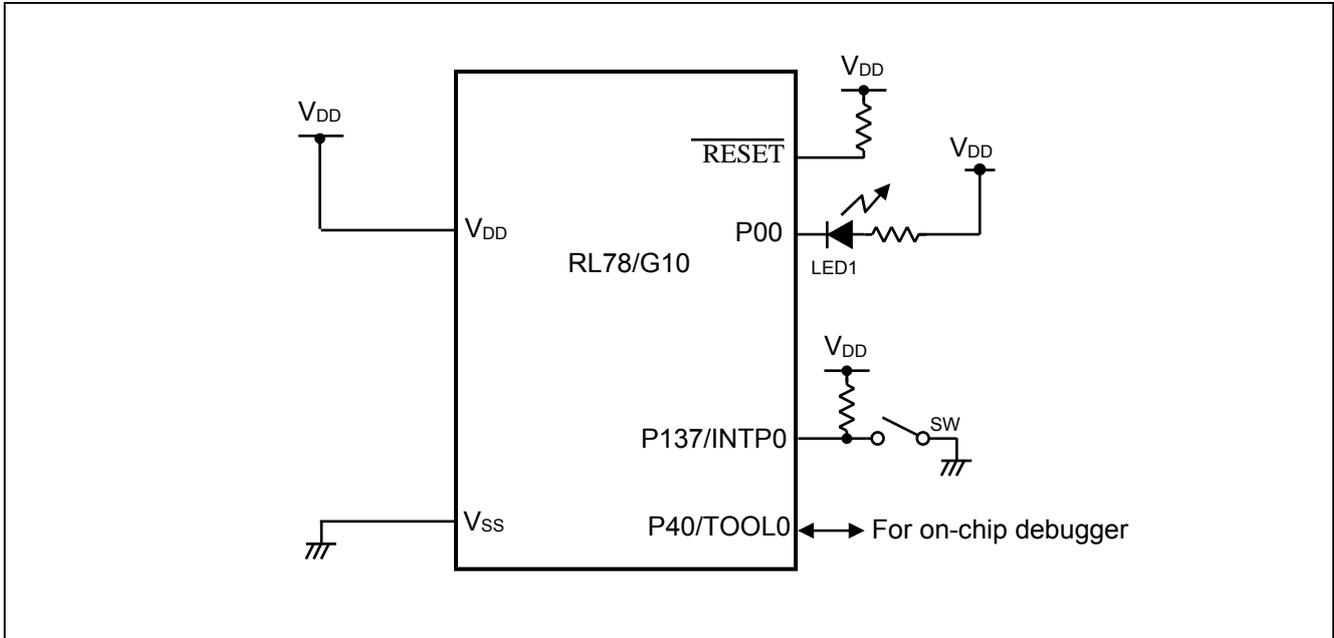

Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must supply not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P00	Output	Output port for LED indications
P137/INTP0	Input	Switch (SW) input pin (external interrupt request input pin)

5.   Description of the Software

5.1   Operation Outline

This application note describes how to set up the interval timer function of TAU0.

This setup is followed by operation for counting the number of timer interrupts (INTTM00) generated by the interval timer. When the count reaches 249, the value of the interval timer is changed. Each time the count reaches 250, the LED indication is inverted. The timer interrupt (INTTM00) cycle time is changed according to the number of times the switch is pressed. The LED on/off cycle time is changed as follows.

500 ms $\rightarrow$ 250 ms $\rightarrow$ 125 ms $\rightarrow$ 62.5 ms $\rightarrow$ 31.25 ms $\rightarrow$ 500 ms $\rightarrow$ …

  (1)   Initialize the TAU.

- Use the interval timer mode as the timer operation mode.

- Initialize timer data register 00 (TDR00) to 2 ms.

- Set the timer output enable register to disable operation.

- Use timer interrupts (INTTM00) from timer channel 0.

  (2)   Initialize the external edge detection interrupt.

- Select a falling edge as the valid edge for INTP0.

- Use INTP0 interrupts.

  -
  (3)   Execute a HALT instruction

- Wait for timer interrupts (INTTM00).

(4) Timer interrupt (INTTM00)

- After the HALT mode is cancelled by a timer interrupt (INTTM00), the number of INTTM00 interrupts generated is counted.

(5) Set the timer data register (TDR00)

- When the timer interrupt (INTTM00) count reaches 249, the value (RTDR00) in RAM for the timer data register is set in the timer data register (TDR00).

(6) Invert the LED indication

- When the timer interrupt (INTTM00) count reaches 250, the LED indication is inverted.

(7) INTP0 interrupt processing

- INTP0 interrupt processing changes the switch input count (INTP0 interrupt count) and RTDR00 value.

5.2   List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1   Option Byte Settings

Address	Value	Description
000C0H	11101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	11110111B	SPOR detection voltage: Falling edge: VDD < 2.84V Rising edge: VDD >= 2.90V
000C2H	11111001B	HOCO: 20 MHz
000C3H	10000101B	Enables the on-chip debugging.

5.3   List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2   Constants for the Sample Program

Constant	Setting	Description
INTERVAL	2h	Interval timer period (in milliseconds).
CCHNGLED	0x00000001	LED blink data.
PERIOD	20000× INTERVAL	TM00 count value at 500 ms.
PERIOD2	PERIOD/2	TM00 count value at 250 ms.
PERIOD3	PERIOD/4	TM00 count value at 125 ms.
PERIOD4	PERIOD/8	TM00 count value at 62.5 ms.
PERIOD5	PERIOD/16	TM00 count value at 31.25 ms.
TINTVL	(PERIOD-1) (PERIOD2-1) (PERIOD3-1) (PERIOD4-1) (PERIOD5-1)	TDR00 settings by number of times the switch is pressed.
T10MSWAIT	(5+1) (10+1) (20+1) (40+1) (80+1)	10 ms timer count values by number of times the switch is pressed.

5.4   List of variables

Table 5.3 lists the global variables that are used by this sample program.

Table 5.3   Global Variables

Type	Variable Name	Contents	Function Used
8 bits	RSWCNT	Switch press counter.	IINTP0, main
8 bits	RTMCNT	Timer interrupt occurrence counter.	SINTTM00, main
16 bits	RTDR00	Value which is set in TDR00 each time the timer interrupt count reaches 250.	SINTTM00, IINTP0, main

5.5   List of Functions (Subroutines)

Table 5.4 lists the functions (subroutines) that are used by this sample program.

Table 5.4   List of Functions (Subroutines)

Function Name	Outline
SSTARTINTV	Starts operation of TAU0 channel 0.
IINTTM00	Processes timer interrupts on TAU0 channel 0.
SINTTM00	Counts the number of INTTM00 interrupts generated. Inverts the LED indication each time the interrupt count reaches 250.
IINTP0	Processes INTP0 interrupts.

5.6   Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] SSTARTINTV

Synopsis	TAU0 channel 0 operation start
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Argument	None
Return value	None
Remarks	None

[Function Name] IINTTM00

Synopsis	TAU0 channel 0 timer interrupt processing
Explanation	This function calls the function which will invert the LED indication.
Argument	None
Return value	None
Remarks	None

[Function Name] SINTTM00

Synopsis	LED turning on/off
Explanation	This function counts 250 timer interrupts (INTTM00) and then inverts the LED indication (for port latch inversion). Also, when the count reaches 249, this function changes the setting of TDR00 to the value specified in RTDR00.
Argument	None
Return value	None
Remarks	None

[Function Name] IINTP0

Synopsis	INTP0 interrupt enable
Explanation	This function processes INTP0 interrupts as they occur.
	It waits 10 ms and then scans P137 (SW input pin). When the switch is pressed, this function changes the RTD00 value.
Argument	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flowchart of the sample program described in this application note.
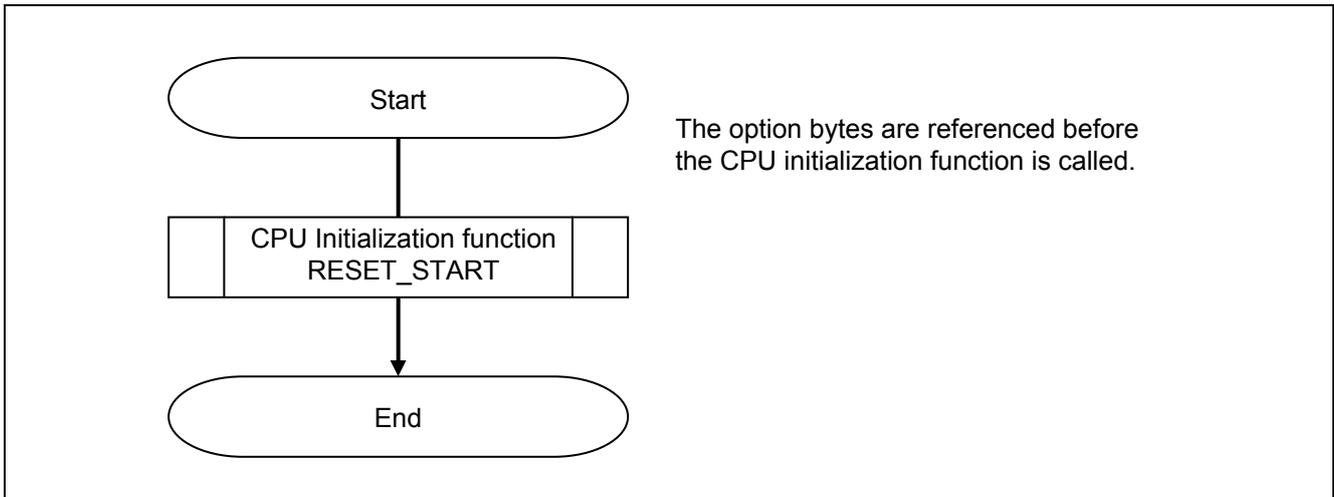
Figure 5.1   Overall Flowchart

5.7.1   CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.
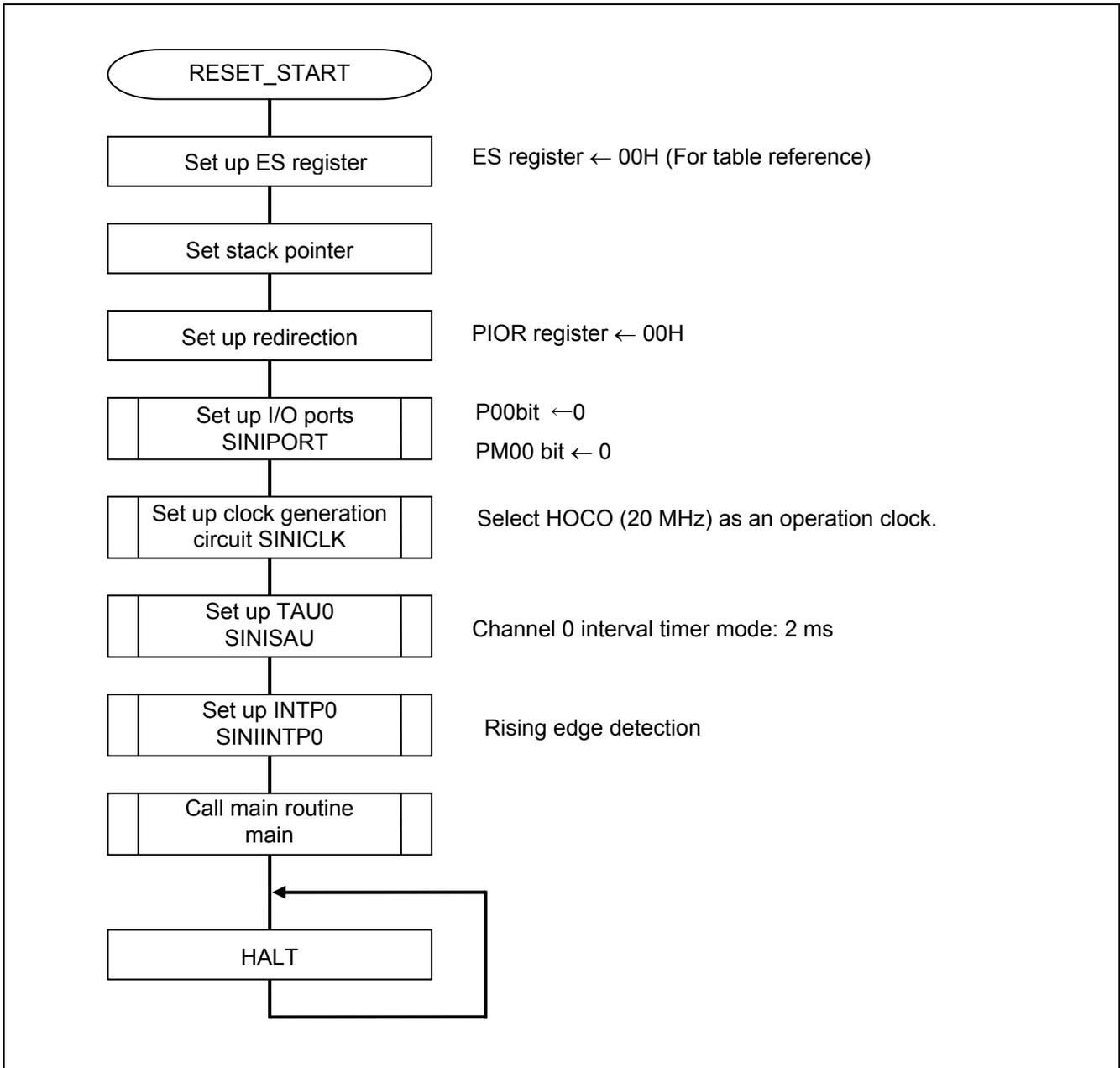
Figure 5.2   CPU Initialization Function

5.7.2   I/O Port Setup

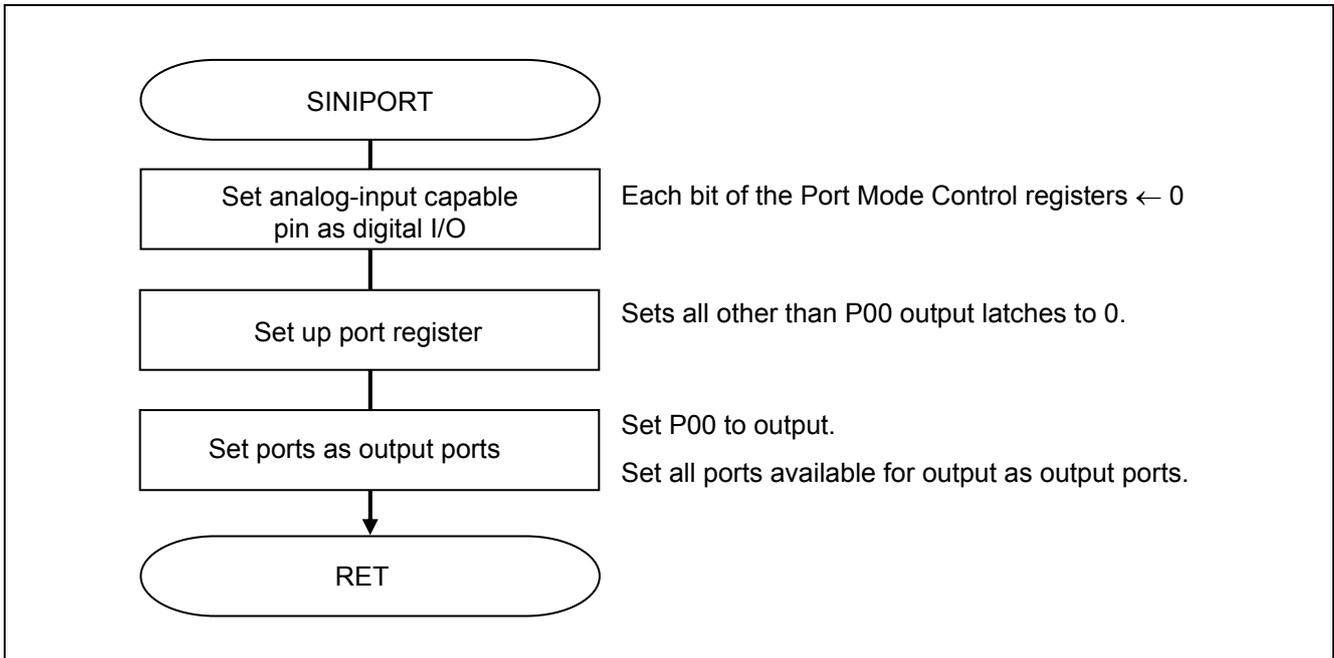Figure 5.3 shows the flowchart for I/O port setup.

Figure 5.3   I/O Port Setup

Note1:   Refer to the section entitled "Flowcharts" in RL78/G10 Initialization CC-RL Application Note (R01AN2668E)
         for the configuration of the unused ports.

   2:   Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any
        unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED port

- Port mode register 0 (PM0)
  Select I/O mode for the port.

10-pin products

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
1	1	1	0	0	0	0	**0**

Bit 0

PM00	P00 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

16-pin products

Symbol: PM0

7	6	5	4	3	2	1	0
PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00
0	0	0	0	0	0	0	**0**

Bit 0

PM00	P00 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.3   Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup.
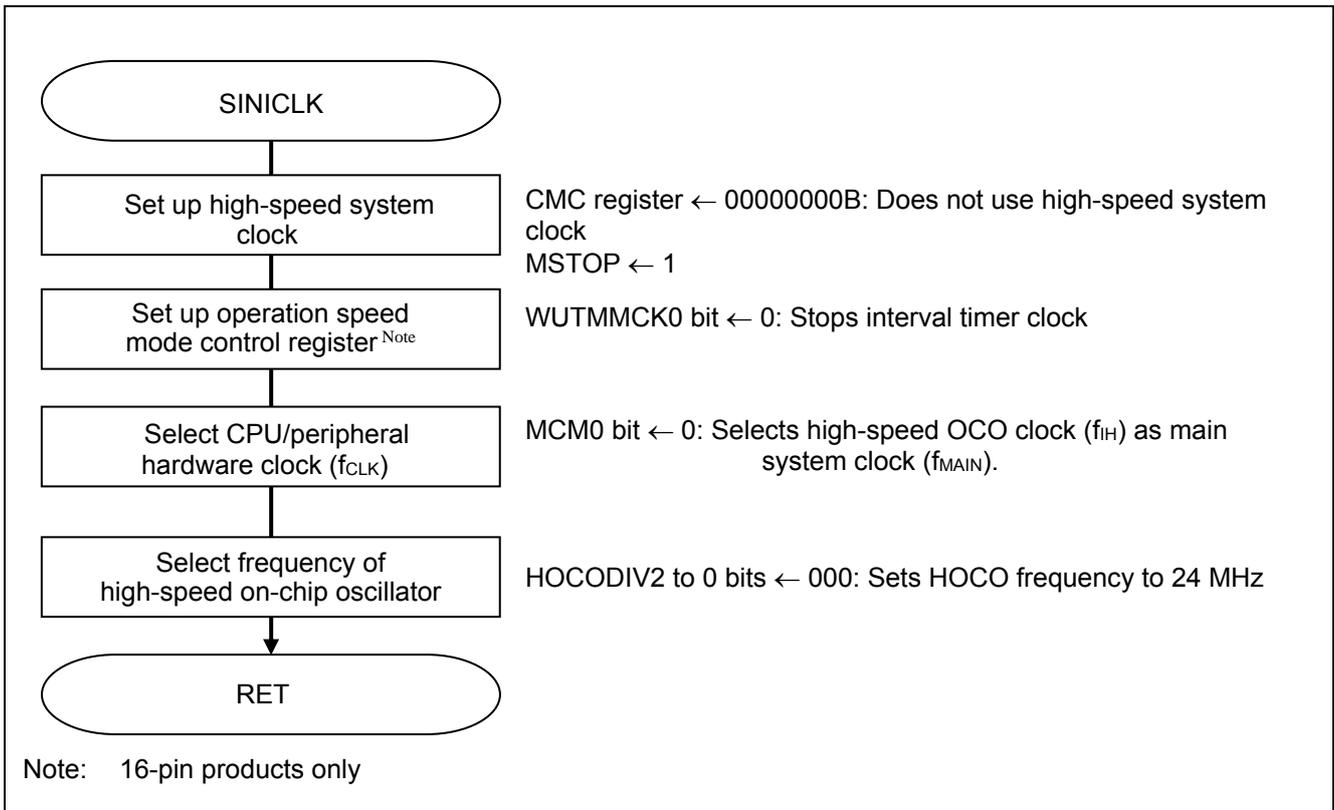
Figure 5.4   Clock Generation Circuit Setup

Caution: For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G10 Initialization CC-RL Application Note (R01AN2668E).

5.7.4   Timer Array Unit Setup

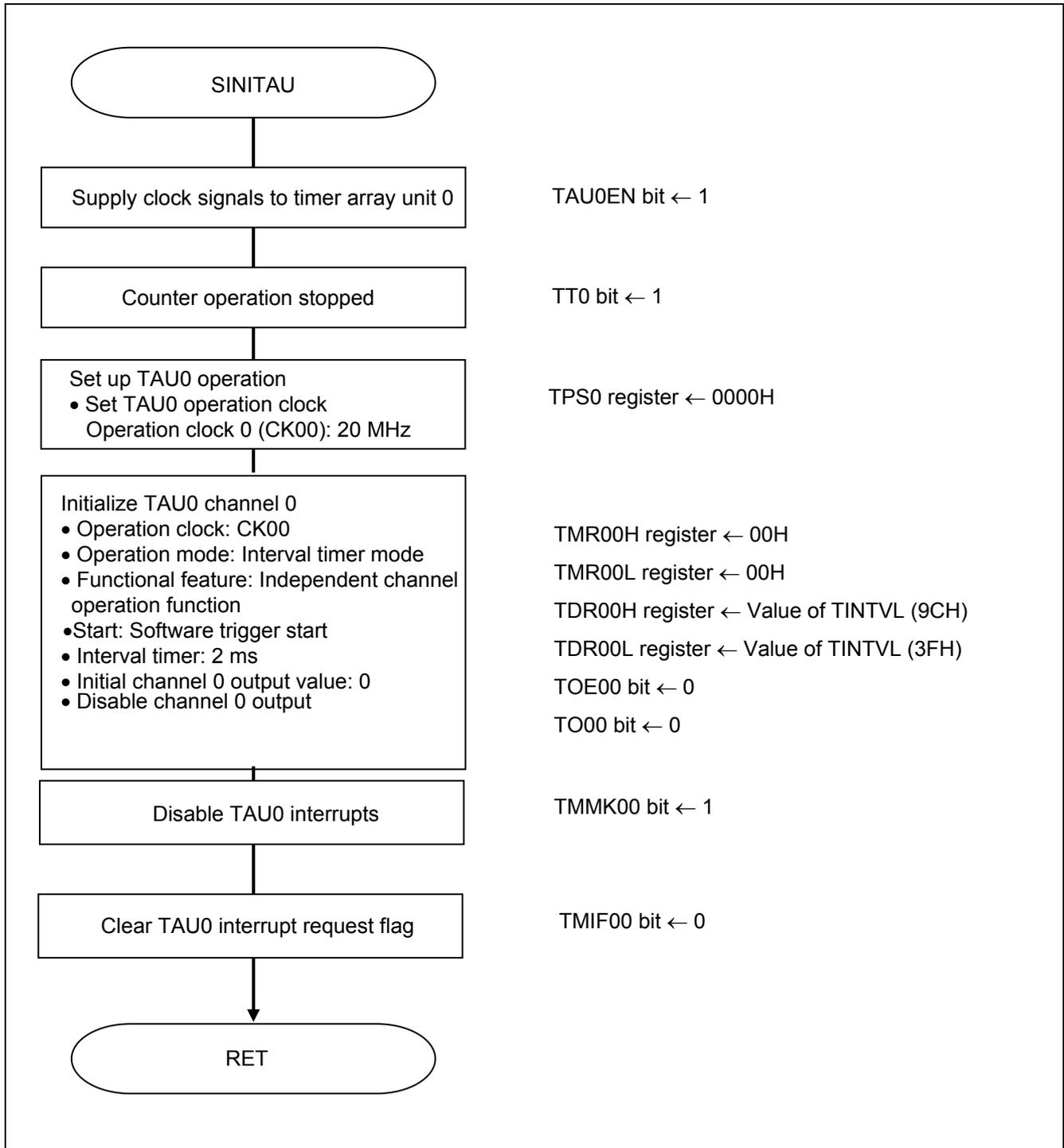Figure 5.5 shows the flowchart for setting up the timer array unit.

Figure 5.5   Timer Array Unit Setup

(1) Starting clock supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
  Start supplying clock to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN[Note]	CMPEN[Note]	ADCEN	IICA0EN[Note]	0	SAU0EN	0	TAU0EN
0	0	x	0	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops supply of input clock.
1	**Supplies input clock.**

Note: 16-pin products only.
Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(2) Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)
  Select an operation clock for timer array unit 0.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK}= 1.25MHz	f_{CLK}= 2.5MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz
0	**0**	**0**	**0**	f_{CLK}	1.25 MHz	2.5 MHz	5 MHz	10 MHz	**20 MHz**
0	0	0	1	$f_{CLK}/2$	625 kHz	1.25 MHz	2.5 MHz	5 MHz	10 MHz
0	0	1	0	$f_{CLK}/2^2$	313 kHz	625 kHz	1.25 MHz	2.5 MHz	5 MHz
0	0	1	1	$f_{CLK}/2^3$	156 kHz	313 kHz	625 kHz	1.25 MHz	2.5 MHz
0	1	0	0	$f_{CLK}/2^4$	78 kHz	156 kHz	313 kHz	625 kHz	1.25 MHz
0	1	0	1	$f_{CLK}/2^5$	39 kHz	78 kHz	156 kHz	313 kHz	625 kHz
0	1	1	0	$f_{CLK}/2^6$	19.5 kHz	39 kHz	78 kHz	156 kHz	313 kHz
0	1	1	1	$f_{CLK}/2^7$	9.8 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
1	0	0	0	$f_{CLK}/2^8$	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz	78 kHz
1	0	0	1	$f_{CLK}/2^9$	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz	39 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz	19.5 kHz
1	0	1	1	$f_{CLK}/2^{11}$	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz	9.8 kHz
1	1	0	0	$f_{CLK}/2^{12}$	313 Hz	625 Hz	1.22 kHz	2.5 kHz	4.9 kHz
1	1	0	1	$f_{CLK}/2^{13}$	152 Hz	313 Hz	625 Hz	1.22 kHz	2.5 kHz
1	1	1	0	$f_{CLK}/2^{14}$	78 Hz	152 Hz	313 Hz	625 Hz	1.22 kHz
1	1	1	1	$f_{CLK}/2^{15}$	39 Hz	78 Hz	152 Hz	313 Hz	625 Hz

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(3) Setting up channel 0 operation mode

- Timer mode register 00 (TMR00H, TMR00L)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select the software trigger start.
  Set up the operation mode.

Symbol: TMR00H

7	6	5	4	3	2	1	0
CKS001	0	0	CCS00	0	STS002	STS001	STS000
0	0	0	**0**	0	**0**	**0**	**0**

Bit 7

CKS001	Selection of operation clock (f_{MCK}) of channel n selection
0	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS00	Selection of count clock (f_{TCLK}) of channel n
0	**Operation clock (f_{MCK}) specified by the CKS001 bit**
1	Valid edge of input signal input from the TI00 pin

Bit 2-0

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	When the channel is used as a slave channel with the one-shot pulse output, PWM output function, or multiple PWM output function: The interrupt request signal of the master channel (INTTM0n) is used as the start trigger.
1	1	0	When the channel is used as a slave channel in two-channel input with one-shot pulse output function: The interrupt request signal of the master channel (INTTM0n) is used as the start trigger. A valid edge of the TI03 pin input of the slave channel is used as the end trigger
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

Symbol: TMR00L

7	6	5	4	3	2	1	0
CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	0	**0**	**0**	**0**	**0**

Bits 7 and 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Bits 3-0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Counting operation of TCR
0	**0**	**0**	**1/0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of the MD000 bit operation varies depending on each operation mode (see the table below).

Operation mode (Value set by the MD003 to MD001 bits) (See the above table)	MD000	Setting of starting counting and interrupt
● Interval timer mode (0, 0, 0) **● Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
● Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
● One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
● Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

(4) Setting the interval timer cycle time

- Timer data register 00 (TDR00)
  Configure the interval timer compare value.

Symbol: TDR00H, TDR00L

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
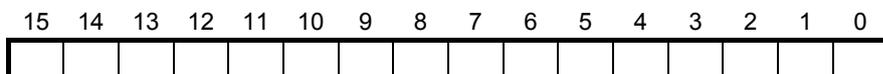
Timer interrupt (INTTM00) occurrence = (TDR00 setting + 1) × Count clock cycle time

(5) Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	TOE03[Note]	TOE02[Note]	TOE01	TOE00
0	0	0	0	0	0	0	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Disables the timer output.** **Timer operation is not reflected in the TO00 bit, and the output is fixed.** **Writing to the TO00 bit is allowed.**
1	Enables the timer output. Timer operation is reflected in the TO00 bit, and output waveform is generated. Writing to the TO00 bit is ignored.

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.5   INTP0 Initialization

Figure 5.6 shows the flowchart for INTP0 initialization.
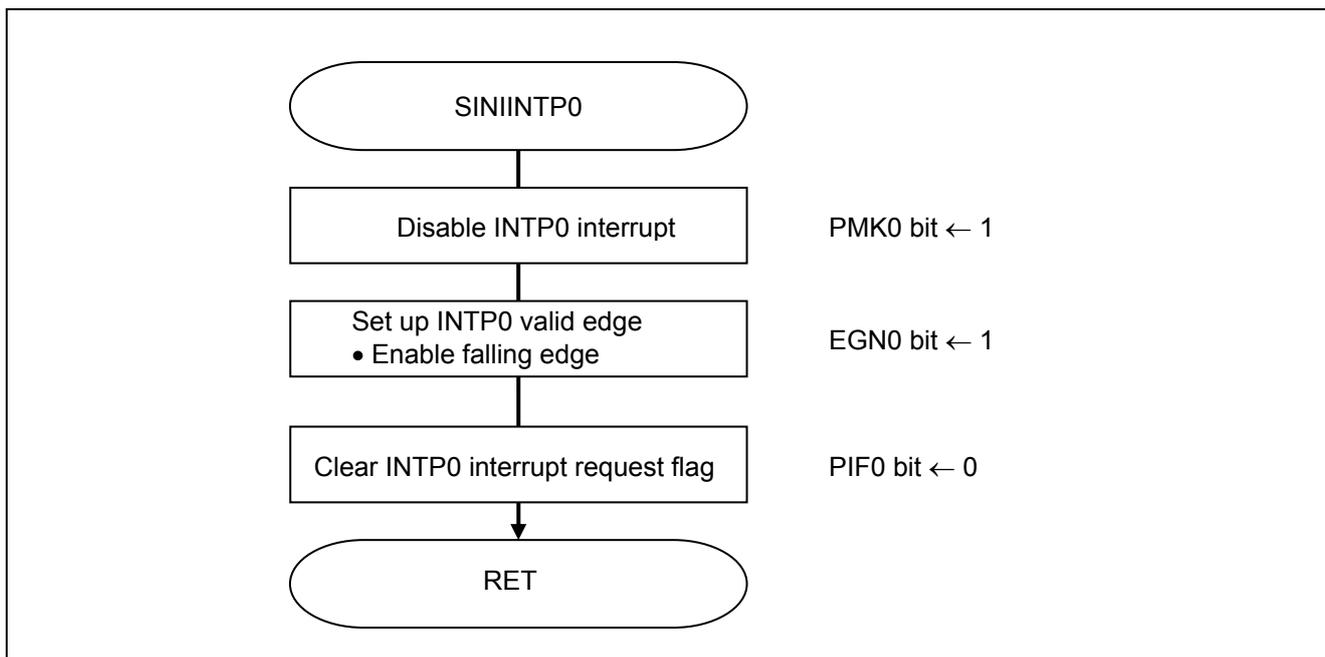
Figure 5.6   INTC Module Setup

(1) Setup for INTP0 pin edge detection

- External interrupt rising edge enable register (EGP0)
  External interrupt falling edge enable register (EGN0)
  Select a valid edge for INTP0

Symbol: EGP0

7	6	5	4	3	2	1	0
0	0	0	0	EGP3 Note	EGP2 Note	EGP1	EGP0
0	0	0	0	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
0	0	0	0	EGN3 Note	EGN2 Note	EGN1	EGN0
0	0	0	0	x	x	x	**1**

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled.
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Note: 16-pin products only

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.6   Main Processing

Figure 5.7 shows the flowchart for main processing.
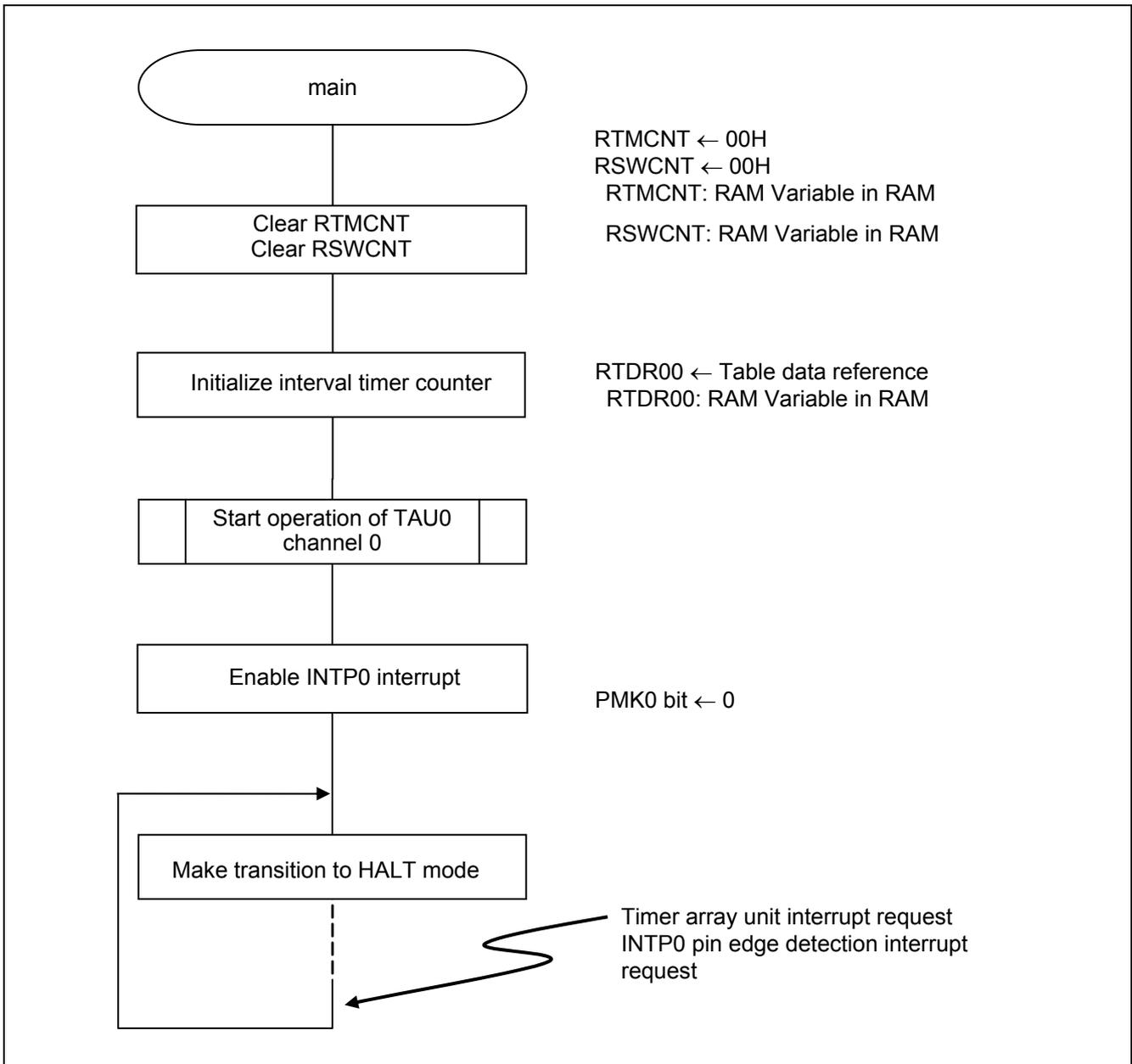
Figure 5.7   Main Processing

5.7.7   TAU0 Channel 0 Startup

Figure 5.8 shows the flowchart for starting the operation of TAU0 channel 0.
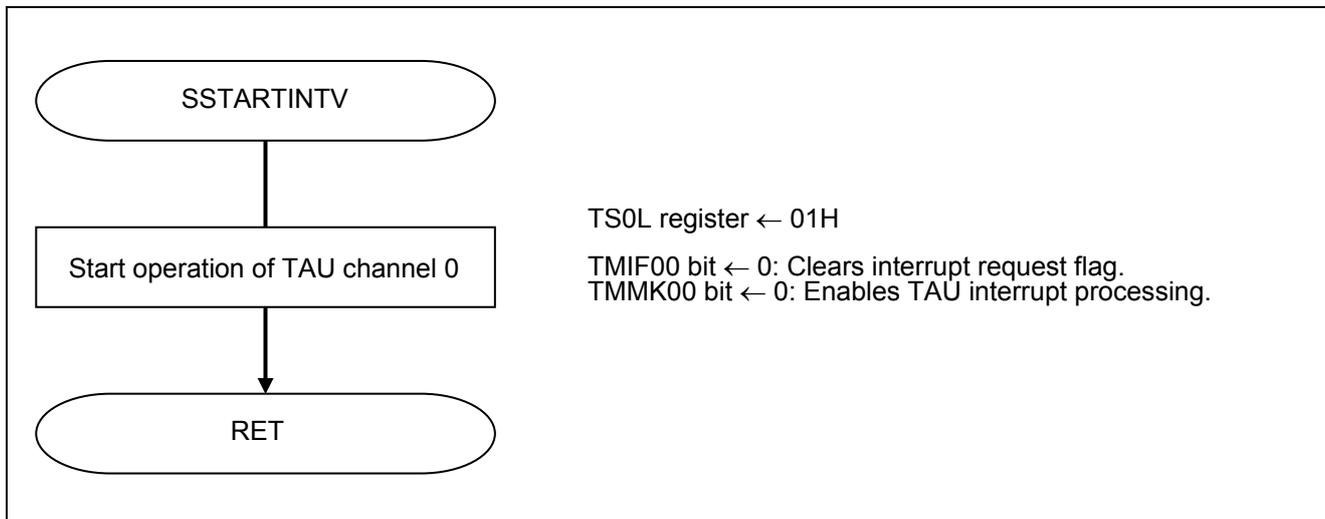
Figure 5.8   TAU0 Channel 0 Startup

(1) Setup for timer channel start

● Timer channel start register 0 (TS0)
Start count operation

Symbol: TS0

7	6	5	4	3	2	1	0
0	0	0	0	TS03[Note]	TS02[Note]	TS01	TS00
0	0	0	0	0	0	0	**1**

Bit 0

TS00	Operation start trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled.

(2) Timer count completion interrupt setup

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 7

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
0	x	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt processing control
0	**Interrupt processing enabled**
1	Interrupt processing disabled

Caution: For details on the register setup procedures, refer to RL78/G10 User's Manual: Hardware.

5.7.8 INTTM00 Interrupt Processing

Figure 5.9 shows the flowchart for INTTM00 interrupt processing.
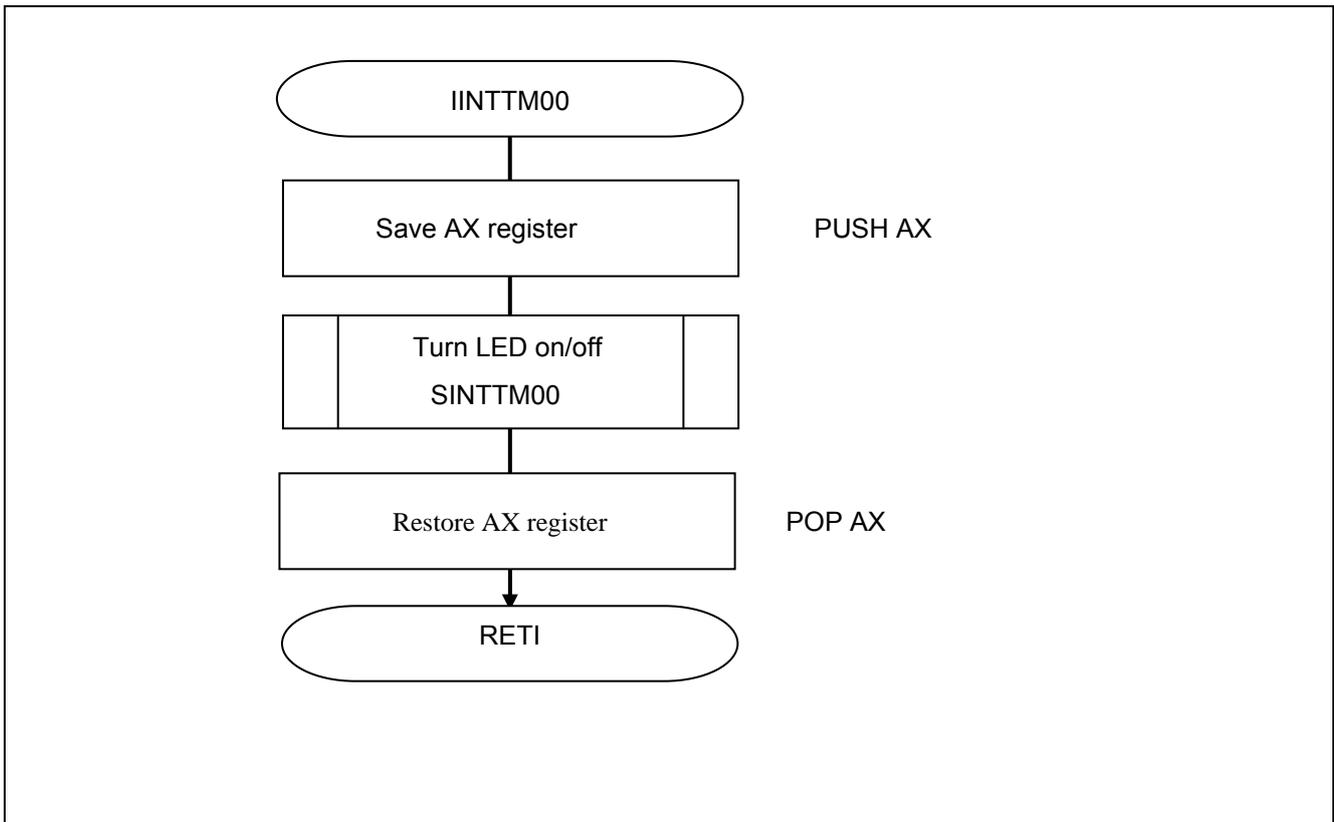
Figure 5.9   INTTM00 Interrupt Processing

5.7.9   LED Turn-On/Off Processing

Figure 5.10 shows the flowchart for LED turn-on/off processing.
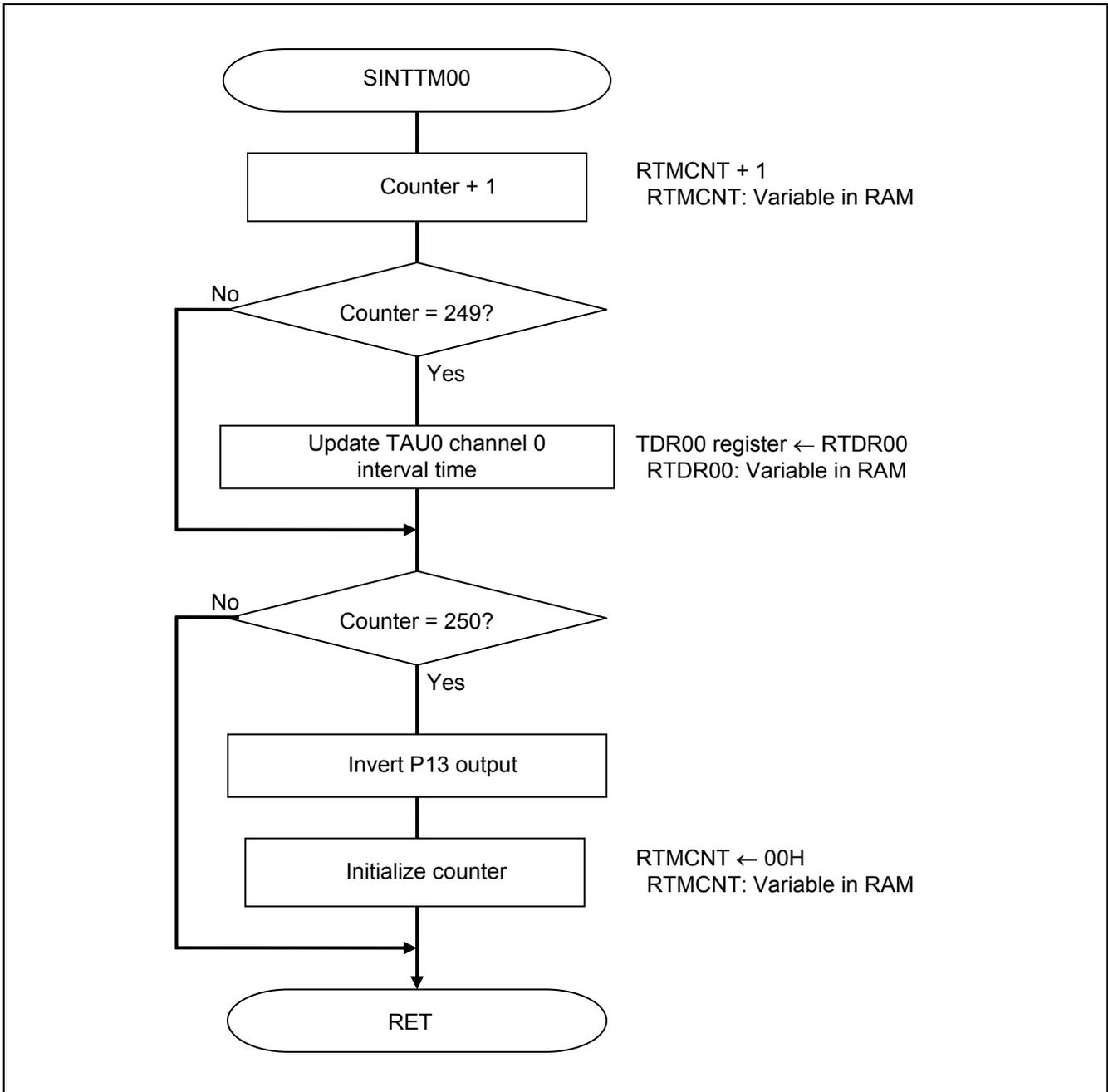
Figure 5.10   Flowchart for LED Turn-on/off Processing

5.7.10 INTP0 Interrupt Processing

Figures 5.11 and 5.12 show the flowchart for INTP0 interrupt processing.
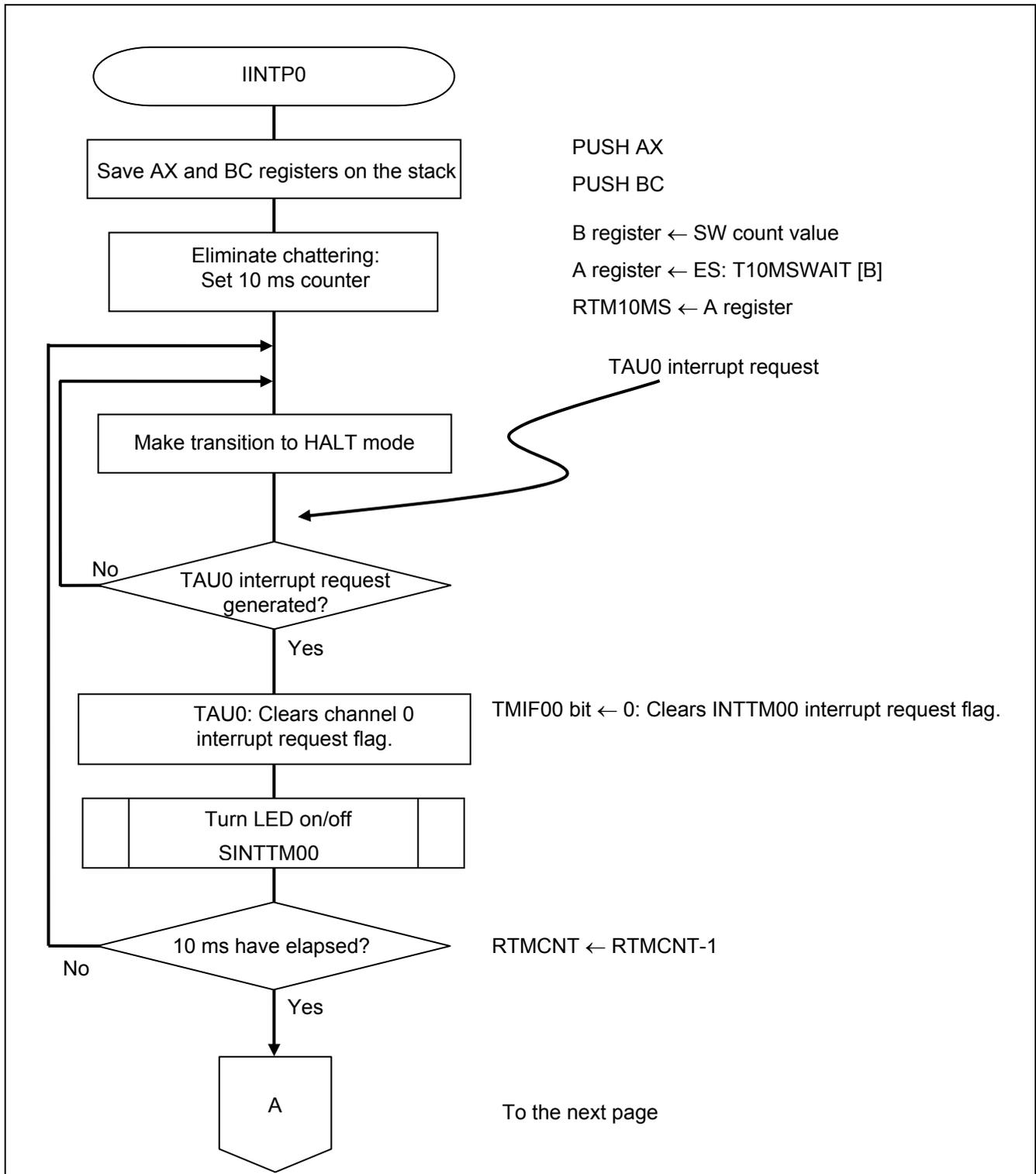
Figure 5.2   INTP0 Interrupt Processing (1/2)

A

P137 is "0"? — No → | If no, it is determined that chatter has occurred.

Yes

Update SW1 input count
RSWCNT = 0 → 1 → 2 → 3 → 4 → 0

RSWCNT ← RSWCNT + 1

RSWCNT ← Loop between 0 and 4

RSWCNT

B register ← RSWCNT

Shift B register left by one bit.

| 0 | 1 | 2 | 3 | 4 |

Obtain TDR00 setting
(LED inversion cycle: 500 ms)

Obtain TDR00 setting
(LED inversion cycle: 125 ms)

Obtain TDR00 setting
(LED inversion cycle: 31.25 ms)

Obtain TDR00 setting
(LED inversion cycle: 250 ms)

Obtain TDR00 setting
(LED inversion cycle: 62.5 ms)

AX register ← ES: TINTVL [B]

Update interval setting

Update the setting of TDR00 each time the number of timer interrupts reaches 250.

RTDR00 ← AX

Initialize INTP0 interrupt request flag

PIF0 bit ← 0: Clear INTP0 interrupt request flag.

Restore AX and BC registers from the stack

POP AX

POP BC

RETI

Figure 5.3   INTP0 Interrupt Processing (2/2)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Website and Support

Renesas Electronics Website
- http://www.renesas.com/index.jsp

Inquiries
- http://www.renesas.com/contact/

Revision Record	RL78/G10 Timer Array Unit (Interval Timer) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Jan. 12, 2016	—	First edition issued

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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