RL78/G10

A/D Conversion CC-RL

Introduction

This application note describes the procedures for performing A/D conversion on analog voltages using the RL78/G10's A/D converter.

The sample program discussed in this application note performs data conversion on the A/D conversion results (shifting the data right by six bits) and places the converted values in the internal RAM of the RL78/G10.

Target Device

RL78/G10

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specification 3

2. Operation Check Conditions 4

3. Related Application Notes 4

4. Description of the Hardware 5
4.1 Hardware Configuration Example 5
4.2 List of Pins to be Used 5

5. Description of the Software 6
5.1 Operation Outline 6
5.2 List of Option Byte Settings 7
5.3 List of Variables 7
5.4 List of Functions (Subroutines) 8
5.5 Function Specifications 8
5.6 Flowcharts 9
5.6.1 CPU Initialization Function 10
5.6.2 I/O Port Setup Function 11
5.6.3 Clock Generation Circuit Setup 12
5.6.4 A/D Converter Setup 13
5.6.5 Main Processing 19
5.6.6 A/D Conversion Start Processing 20

6. Sample Code 22

7. Documents for Reference 22

Revision Record 23

General Precautions in the Handling of MPU/MCU Products 24

1. Specification

This application note provides examples of using the software trigger and sequential conversion modes of the A/D converter. The analog signal input from the P01/ANI0 pin is converted to digital values. Subsequently, the conversion result is subjected to data conversion (shifting the data right by six bits) and the result is stored in the RL78/G10's internal RAM.

Table 1.1 lists the peripheral function to be used and its uses. Figure 1.1 shows the outline of the conversion operation of the A/D converter.

Table 1.1 Peripheral Function to be Used and its Use

Peripheral Function	Use
A/D converter	Converts the level of the analog signal input from the P01/ANI0 pin.

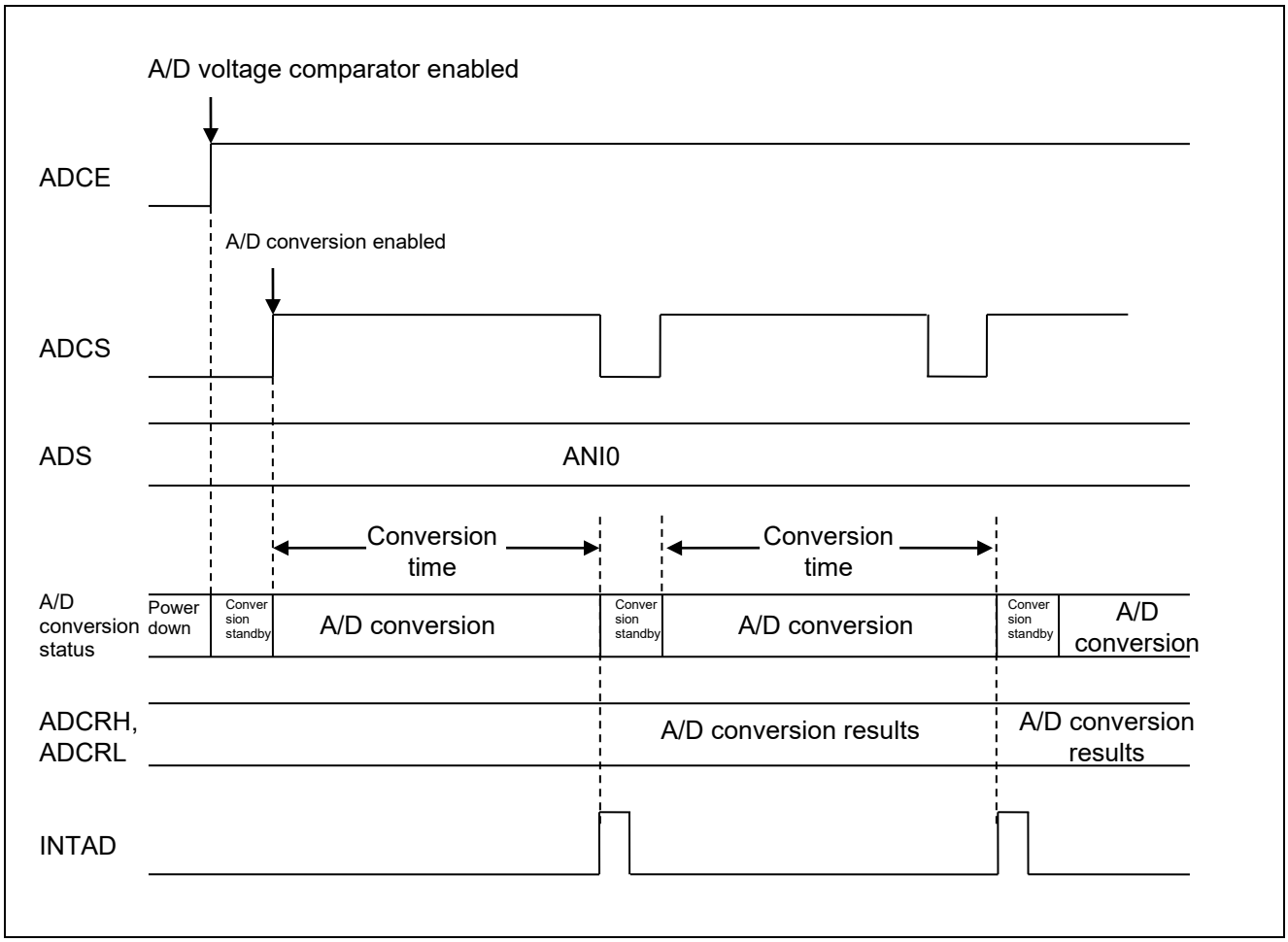

Figure 1.1 Outline of the A/D Converter Conversion Processing

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G10 (R5F10Y16ASP)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 20 MHz • CPU/peripheral hardware clock: 20 MHz
Operating voltage	5.0 V (can run at a voltage range of 2.9 V to 5.5 V.) SPOR detection voltage When reset occurs: V_{DD} < 2.84 V When reset is released: $V_{DD} \geq$ 2.90 V
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e2 studio V4.0.0.26 from Renesas Electronics Corp.
Assembler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems
Assembler (IAR)	IAR Assembler for Renesas RL78 V4.21.2.2420 from IAR Systems
Board to be used	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G10 Initialization (R01AN2668E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

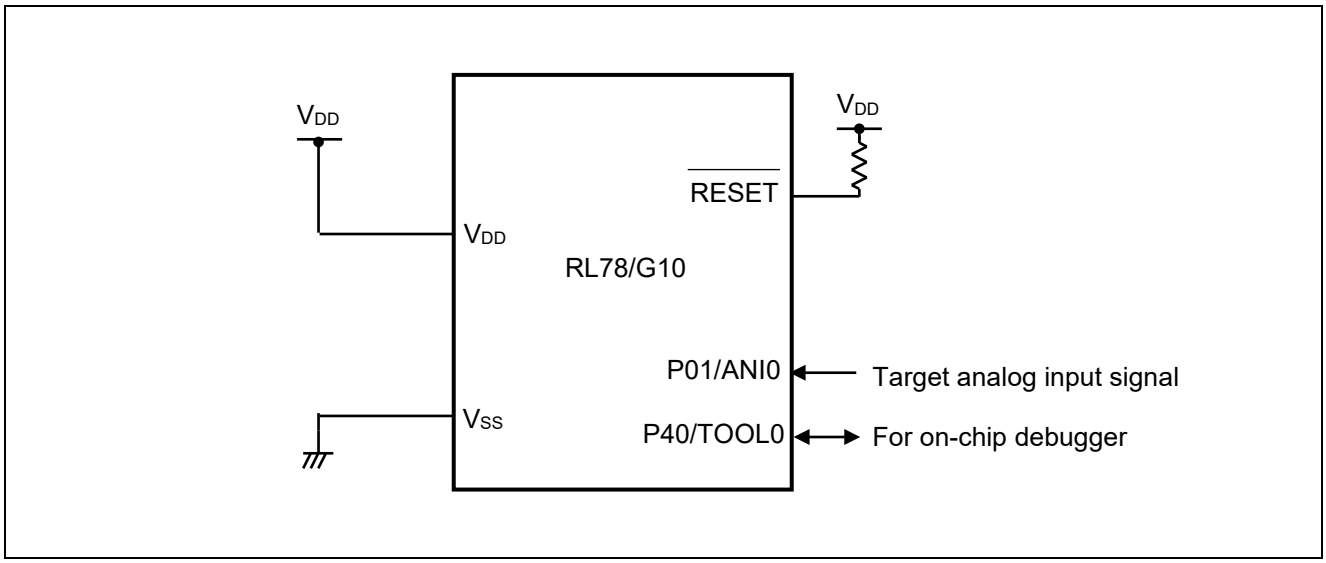

Figure 4.1 Hardware Configuration

Cautions 1 The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical characteristics conditions are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

2 V_{DD} must be held at not lower than the reset release voltage (V_{SPOR}) that is specified as SPOR.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their function.

Table 4.1 Pins to be Used and their Function

Pin Name	I/O	Description
P01/ANI0	Input	A/D converter analog input port

5. Description of the Software

5.1 Operation Outline

This sample code performs A/D conversion on the analog voltage that is input to pin ANI0 using the A/D converter. It awaits the end of A/D conversion in HALT mode. After A/D conversion is completed, the sample code shifts the result of A/D conversion right by six bits and places the result in the internal RAM of the RL78/G10.

(1) Initialize the A/D converter.
<Setup conditions>

- Pin P01/ANI0 is used for the analog input.
- Ten-bit resolution is used for the A/D conversion resolution.

(2) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion, executes the HALT instruction, places the chip in the HALT mode, and waits for an A/D conversion end interrupt.

(3) After completing the A/D conversion of the voltage input from pin ANI0, the A/D converter transfers the result of A/D conversion to the ADCRH and ADCRL registers and generates an A/D conversion end interrupt.

(4) On release from the HALT mode in response to the A/D conversion end interrupt, the sample program reads the result of A/D conversion from the ADCRH and ADCRL registers, shifts the result right by six bits, and stores the shifted data in the internal RAM of the RL78/G10.

(5) The sample program sets the ADCS bit of the ADM0 register to 1 (A/D conversion start) to start A/D conversion, places the chip in the HALT mode again, and waits for an A/D conversion end interrupt.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	11101110B	Stops the watchdog timer operation. (Stops counting after the release of the reset state.)
000C1H	11110111B	SPOR detection voltage When reset occurs: V_{DD} < 2.84 V When reset is released: $V_{DD} \geq$ 2.90 V
000C2H	11111001B	HOCO: 20 MHz
000C3H	10000101B	Enables the on-chip debugging function.

5.3 List of Variables

Table 5.2 lists the variable that is used by this sample program.

Table 5.2 Global Variable

Type	Variable Name	Contents	Function Used
16-bit variable	RADCBUF	Area for storing the A/D conversion results	main

5.4 List of Functions (Subroutines)

Table 5.3 lists the functions (subroutines) that are used by this sample program.

Table 5.3 List of Functions (Subroutines)

Function Name	Outline
SINIADC	Initializes A/D converter
SSTARTAD	Starts A/D conversion

5.5 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START

Synopsis	Initializes the CPU at reset start.
Explanation	Calls the main function after setting the stack pointer and initializing the hardware.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIADC

Synopsis	Initializes the A/D converter.
Explanation	Sets the conversion time, resolution (10-bit conversion), and analog input channels of the A/D converter.
Arguments	None
Return value	None
Remarks	None

[Function Name] SSTARTAD

Synopsis	Starts A/D conversion.
Explanation	Enables A/D conversion end interrupts and starts A/D conversion processing.
Arguments	None
Return value	None
Remarks	None

5.6 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

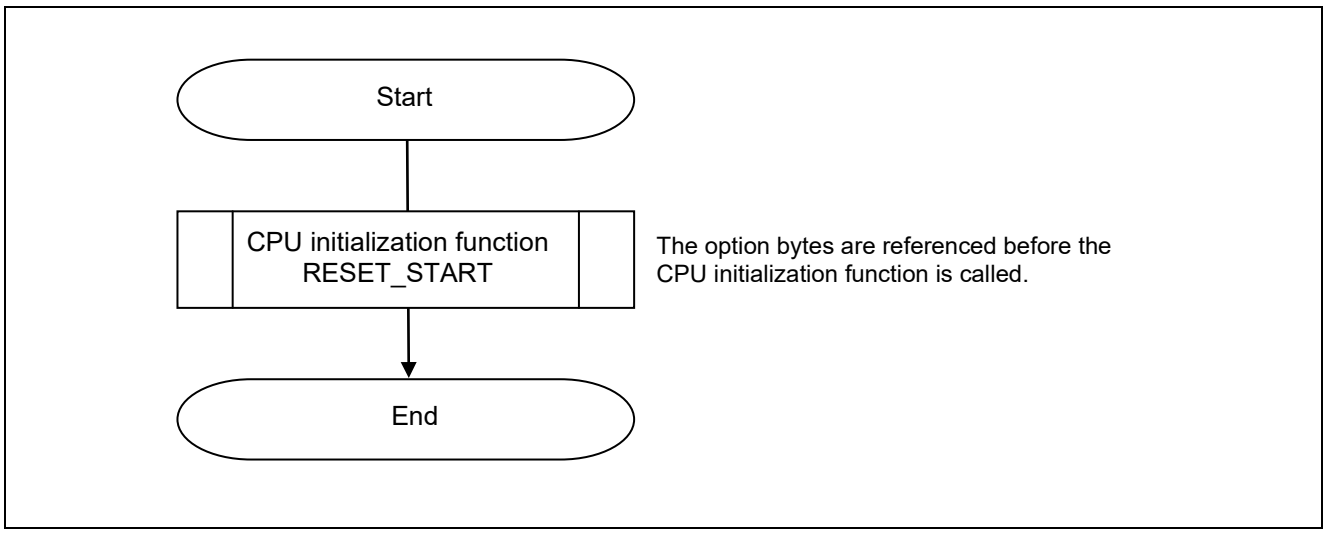

Figure 5.1 Overall Flow

5.6.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

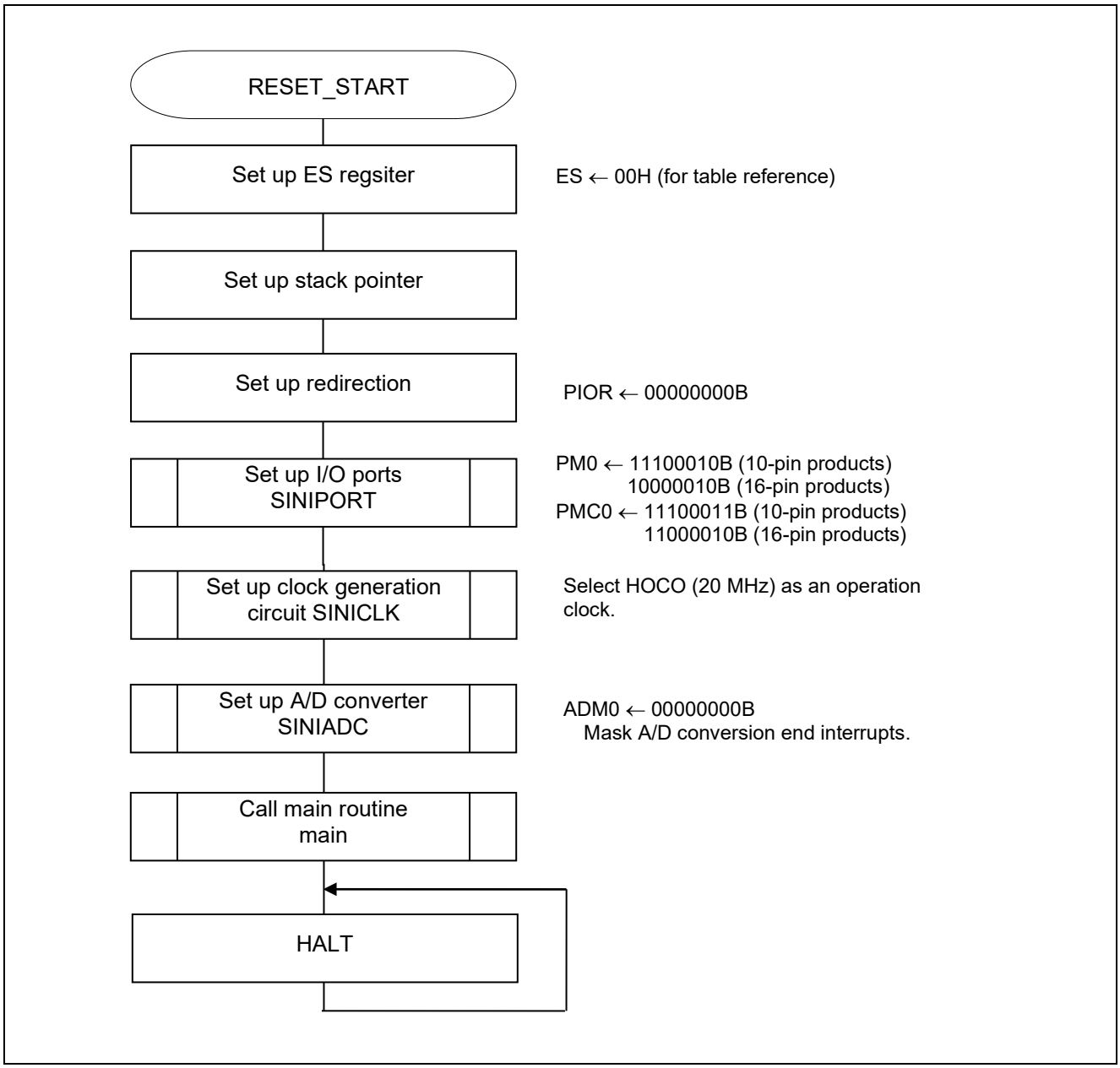

Figure 5.2 CPU Initialization Function

5.6.2 I/O Port Setup Function

Figure 5.3 shows the flowchart for the I/O port setup function.

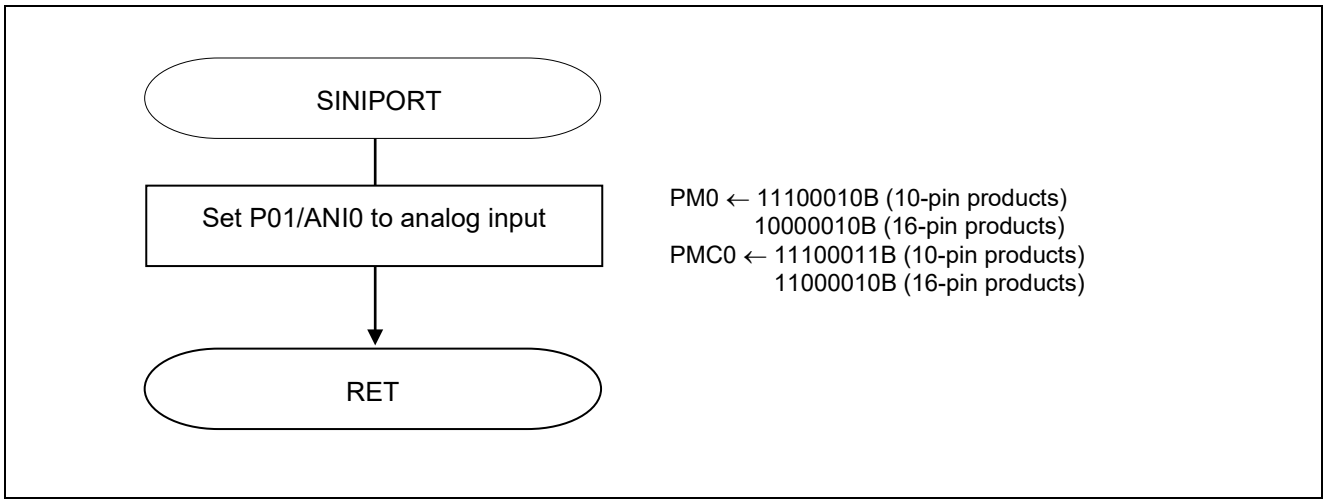

Figure 5.3 I/O Port Setup Function

Note Refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN2668E) for the configuration of the unused ports.

Caution Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via separate resistors.

5.6.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for clock generation circuit setup. Because 10-pin products do not have the resonator connection pins for the main system clock (X1 and X2) and the external clock input pin (EXCLK), only the high-speed on-chip oscillator frequency should be set in 10-pin products.

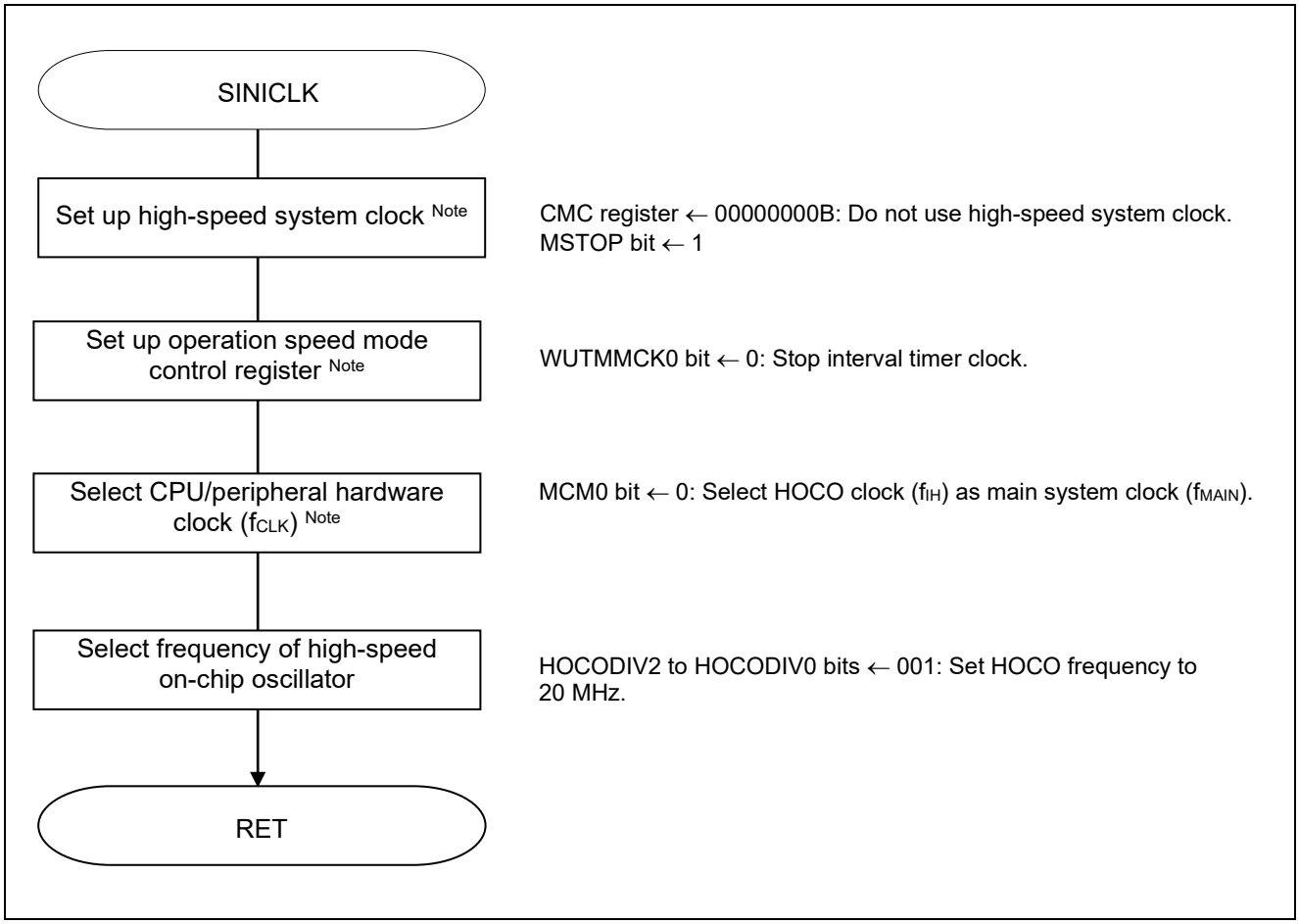

Figure 5.4 Clock Generation Circuit Setup

Note 16-pin products only.

Caution For details on the procedure for setting up the clock generation circuit (SINICLK), refer to the section entitled "Flowcharts" in RL78/G10 Initialization Application Note (R01AN2668E).

5.6.4 A/D Converter Setup

Figure 5.5 shows the flowchart for setting up the A/D converter.

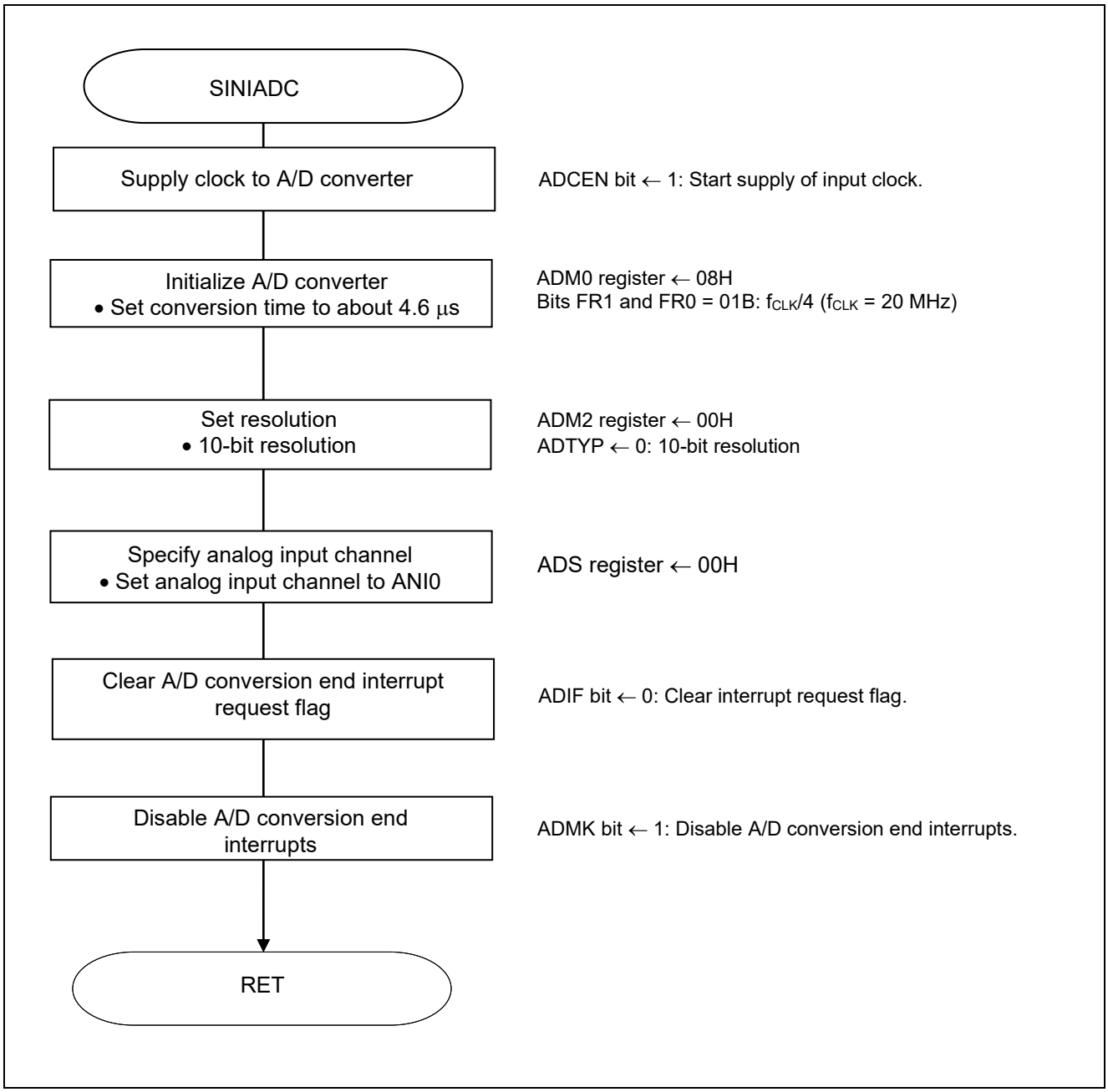

Figure 5.5 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN Note	0	ADCEN	IICA0EN Note	0	SAU0EN	0	TAU0EN
x	0	**1**	x	x	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note 16-pin products only.

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
x	0	0	**0**	**1**	0	**0**	x

Bits 4, 3, and 1

(1) 10-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [μs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	**f_{CLK} = 20 MHz**
0	0	**0**	$f_{CLK}/8$	23 f_{AD} (Number of sampling clock: 9 f_{AD})	$184/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	9.2
0	**1**		**$f_{CLK}/4$**		**$92/f_{CLK}$**			18.4	9.2	**4.6**
1	0		$f_{CLK}/2$		$46/f_{CLK}$		18.4	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$23/f_{CLK}$	18.4	9.2	4.6	Setting prohibited	
0	0	1	$f_{CLK}/8$	17 f_{AD} (Number of sampling clock: 5 f_{AD})	$136/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	18.4	6.8
0	1		$f_{CLK}/4$		$68/f_{CLK}$			18.4	9.2	3.4
1	0		$f_{CLK}/2$		$34/f_{CLK}$		13.6	9.2	4.6	Setting prohibited
1	1		f_{CLK}		$17/f_{CLK}$	13.6	6.8	4.6	Setting prohibited	

(2) 8-Bit Resolution A/D Conversion Time Selection

ADM0			Conversion Clock	Number of Conversion Clock	Conversion Time	Conversion Time Selection [μs]				
FR1	FR0	LV0				f_{CLK} = 1.25 MHz	f_{CLK} = 5 MHz	f_{CLK} = 5 MHz	f_{CLK} = 10 MHz	f_{CLK} = 20 MHz
0	0	0	$f_{CLK}/8$	21 f_{AD} (Number of sampling clock: 9 f_{AD})	$168/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	16.8	8.4
0	1		$f_{CLK}/4$		$84/f_{CLK}$			16.8	8.4	4.2
1	0		$f_{CLK}/2$		$43/f_{CLK}$		16.8	8.4	4.2	Setting prohibited
1	1		f_{CLK}		$21/f_{CLK}$	16.8	8.4	4.2	Setting prohibited	
0	0	1	$f_{CLK}/8$	15 f_{AD} (Number of sampling clock: 3 f_{AD})	$120/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	12.0	6.0
0	1		$f_{CLK}/4$		$60/f_{CLK}$			12.0	6.0	3.0
1	0		$f_{CLK}/2$		$30/f_{CLK}$		12.0	6.0	3.0	Setting prohibited
1	1		f_{CLK}		$15/f_{CLK}$	12.0	6.0	3.0	Setting prohibited	

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up the resolution

- A/D converter mode register 2 (ADM2)
  Sets the resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ADTYP
0	0	0	0	0	0	0	**0**

Bit 0

ADTYP	Resolution of A/D conversion
0	**10-bit resolution**
1	8-bit resolution

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Specifying the input channel

- Analog input channel specification register (ADS)
  Specifies the input channel for the analog voltage to be subjected to A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
0	0	0	0	0	ADS2 Note1	ADS1	ADS0
0	0	0	0	0	**0**	**0**	**0**

10-pin products

ADS1	ADS0	Analog input channel	Input source
0	**0**	**ANI0**	**P01/ANI0 pin**
0	1	ANI1	P02/ANI1 pin
1	0	ANI2	P03/ANI2 pin
1	1	ANI3	P04/ANI3 pin

16-pin products

ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**ANI0**	**P01/ANI0 pin**
0	0	1	ANI1	P02/ANI1 pin
0	1	0	ANI2	P03/ANI2 pin
0	1	1	ANI3	P04/ANI3 pin
1	0	0	ANI4	P05/ANI4 pin
1	0	1	ANI5	P10/ANI5 pin
1	1	0	ANI6	P11/ANI6 pin
1	1	1	Internal reference voltage (0.815 V (typ.)) Note2	—

Note1 16-pin products only.
Note2 When the internal reference voltage is selected as the target for conversion by the A/D converter, be sure to clear the LV0 bit in the A/D converter mode register 0 (ADM0) to 0.
Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

Setting up A/D conversion end interrupts

- Interrupt request flag register (IF0H)
  Clears the interrupt request flag.
- Interrupt mask flag register (MK0H)
  Disables interrupts.

Symbol: IF0H

7	6	5	4	3	2	1	0
0	0	0	0	0	KRIF	ADIF	TMIF01
0	0	0	0	0	x	**0**	x

Bit 1

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
x	x	x	x	x	x	**1**	x

Bit 1

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

5.6.5 Main Processing

Figure 5.6 shows the flowchart for the main processing.

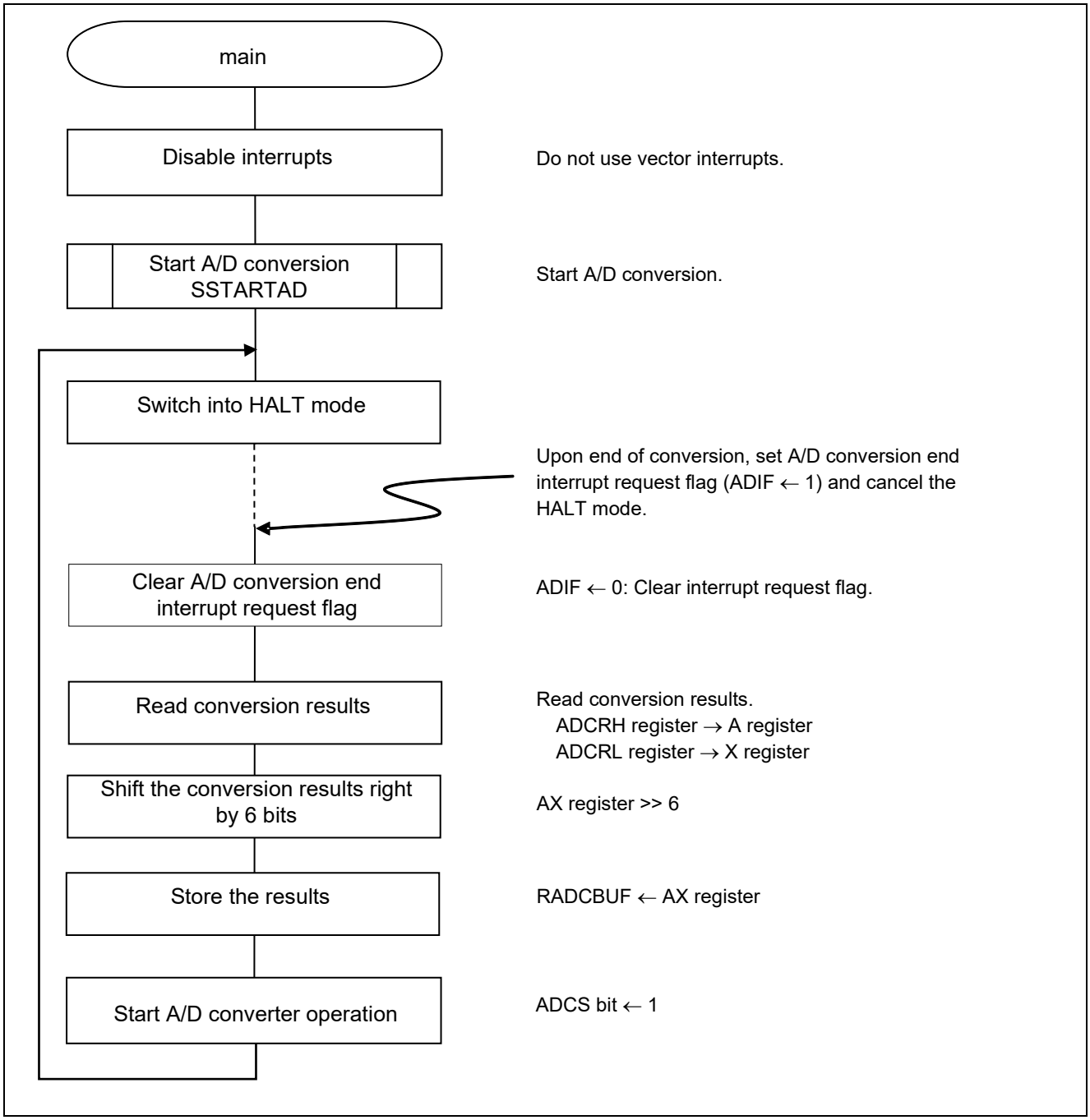

Figure 5.6 Main Processing

5.6.6 A/D Conversion Start Processing

Figure 5.7 shows the flowchart for the A/D conversion start processing.

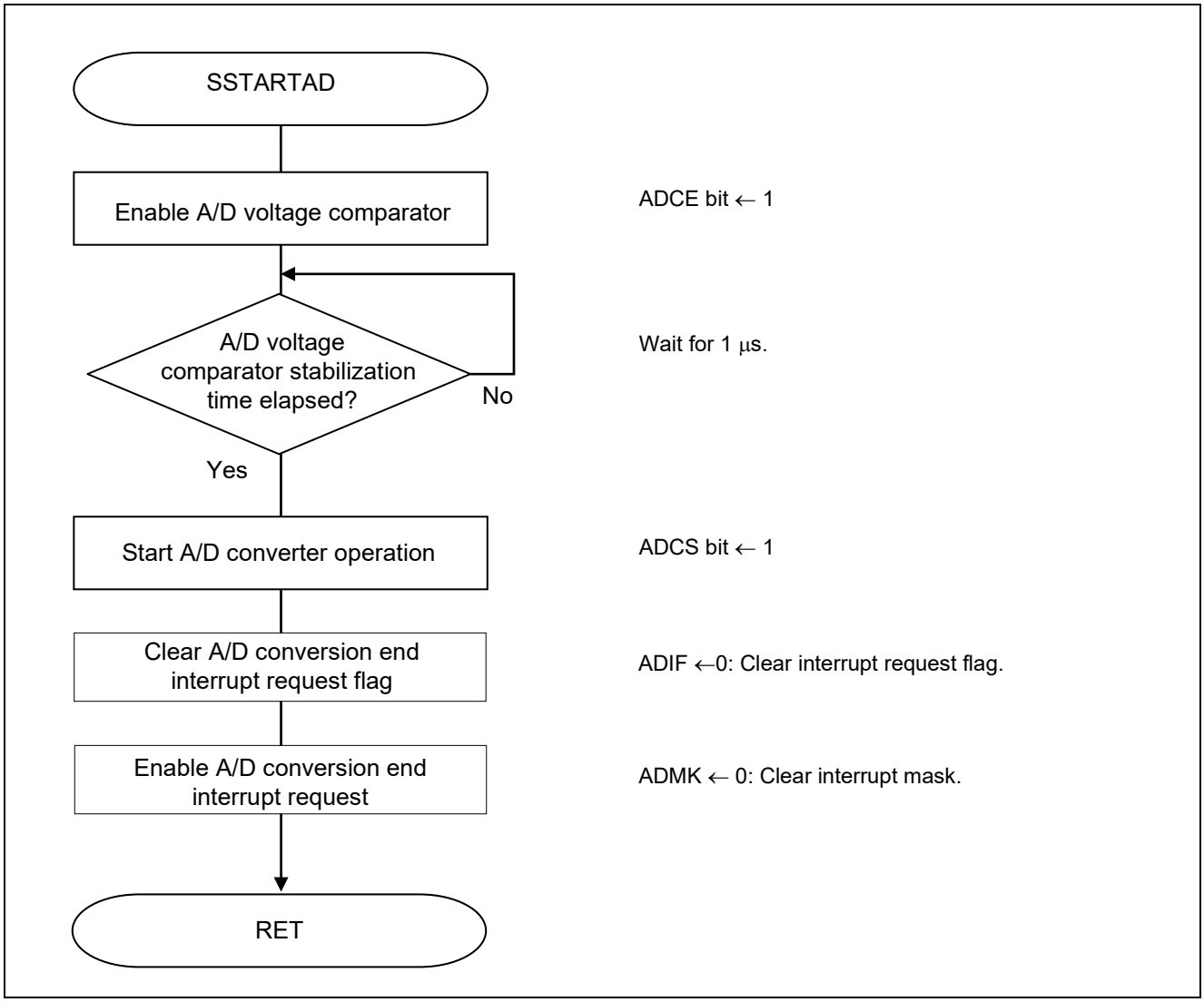

Figure 5.7 A/D Conversion Start Processing

Starting conversion operation

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	0	0	FR1	FR0	0	LV0	ADCE
1	0	0	0	1	x	x	**1**

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation
1	**Enables conversion operation**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	**Enables A/D voltage comparator operation**

Caution For details on the procedure for setting up the registers, refer to RL78/G10 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware (R01UH0384E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision Record	RL78/G10 A/D Conversion CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 01, 2015	—	First edition issued
1.01	Oct.05,2016	—	Error correction
1.10	June.24,2022	**4**	Operation check condition is updated.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

- A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

- The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

- Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

- Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

- After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

- Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

- Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

- Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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