R8C/M12A Group

Setting Example of System Base Clock

R01AN0092EJ0100
Rev. 1.00
July 19, 2011

Abstract

This document describes a method of setting the system base clock switching operation in the R8C/M12A Group.

Product

R8C/M12A Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The system base clock is switched as follows:

- Low-speed on-chip oscillator (no division) → High-speed on-chip oscillator (no division)
- Low-speed on-chip oscillator (no division) → Low-speed on-chip oscillator (divided-by-8)
- Low-speed on-chip oscillator (no division) → XIN clock (no division)
- Low-speed on-chip oscillator (no division) → XIN clock (no division) → High-speed on-chip oscillator (no division)

In this document, no division of system clock (f) is used for the CPU clock (fs).

Table 1.1 lists the Peripheral Function and Its Application. Figures 1.1 to 1.4 show the Transition Diagram of the System Base Clock (Sample Programs 1 to 4).

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Clock generation circuit	System base clock switching

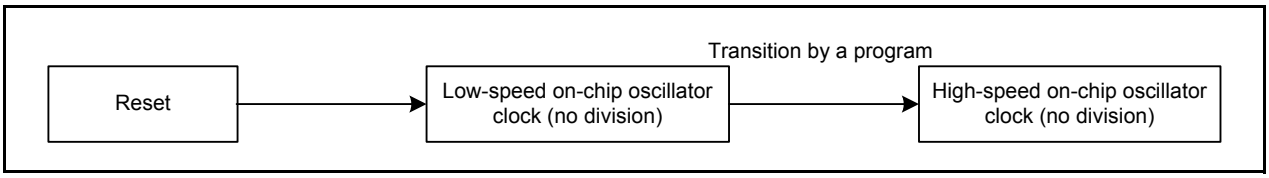

Figure 1.1 Transition Diagram of the System Base Clock (Sample Program 1)

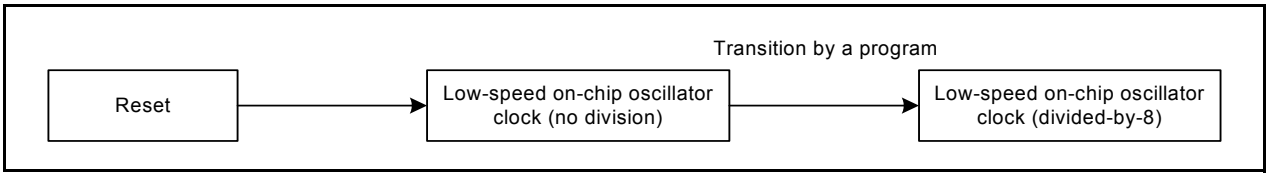

Figure 1.2 Transition Diagram of the System Base Clock (Sample Program 2)

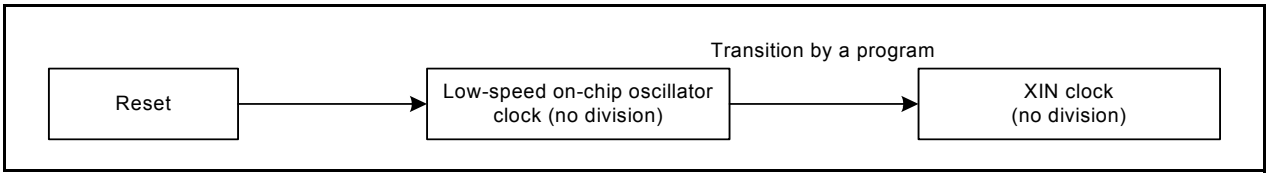

Figure 1.3 Transition Diagram of the System Base Clock (Sample Program 3)

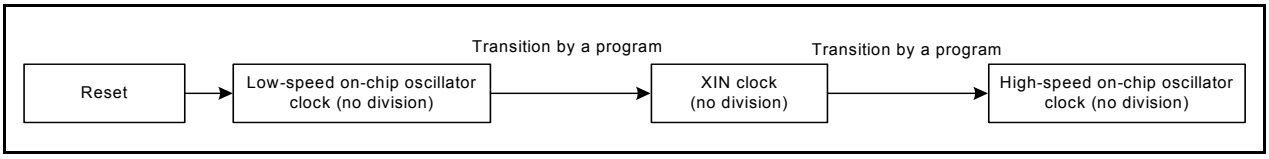

Figure 1.4 Transition Diagram of the System Base Clock (Sample Program 4)

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R8C/M12A Group
Operating frequencies	Sample program 1 • High-speed on-chip oscillator clock: 20 MHz (typical) • System clock (f): 20 MHz • CPU clock (fs): 20 MHz Sample program 2 • Low-speed on-chip oscillator clock: 125 kHz (typical) • System clock (f): 15.625 kHz • CPU clock (fs): 15.625 kHz Sample program 3 • XIN clock: 20 MHz • System clock (f): 20 MHz • CPU clock (fs): 20 MHz Sample program 4 • XIN clock: 20 MHz • High-speed on-chip oscillator clock: 20 MHz (typical) • System clock (f): 20 MHz • CPU clock (fs): 20 MHz
Operating voltage	5.0 V (2.7 to 5.5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation M16C Series, R8C Family C Compiler V.5.45 Release 01
	Compile options -D__UART0__ -c -finfo -dir "$(CONFIGDIR)" -R8C (Default setting is used in the integrated development environment.)

3. Software: Sample Program 1

3.1 Operation Overview

(1) No division of fLOCO (low-speed on-chip oscillator) is automatically selected for fBASE (system base clock) after reset.
(2) Set the HOCOE bit in the OCOCR register to 1, oscillate fHOCO (high-speed on-chip oscillator), and wait until oscillation stabilizes by a program.
(3) Set the HSCKSEL bit in the SCKCR register to 1 and select fHOCO for fHSCK (high-speed clock).
(4) Set 00h to the PHISEL register and select no division of fBASE for f (system clock).
(5) Set the SCKSEL bit in the CKSTPR register to 1 and switch fBASE from fLOCO to fHSCK.
(6) Set bits PHISSEL2 to PHISSEL0 in the SCKCR register to 000b and select no division of f for fs (CPU clock).

Refer to r01an0092_src_sample1.c for a sample program.

Figure 3.1 shows the Timing Diagram of the Sample Program 1 Setting.

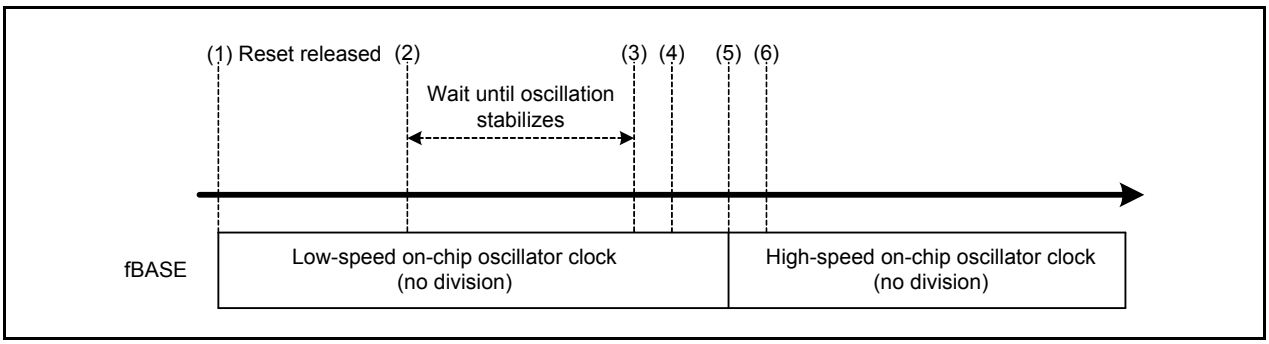

Figure 3.1 Timing Diagram of the Sample Program 1 Setting

3.2 Required Memory Size

Table 3.1 lists the Required Memory Size.

Table 3.1 Required Memory Size

Memory Used	Size	Remarks
ROM	70 bytes	In the r01an0092_src_sample1.c module
RAM	0 bytes	In the r01an0092_src_sample1.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

3.3 Flowcharts

3.3.1 Main Processing

Figure 3.2 shows the Main Processing.

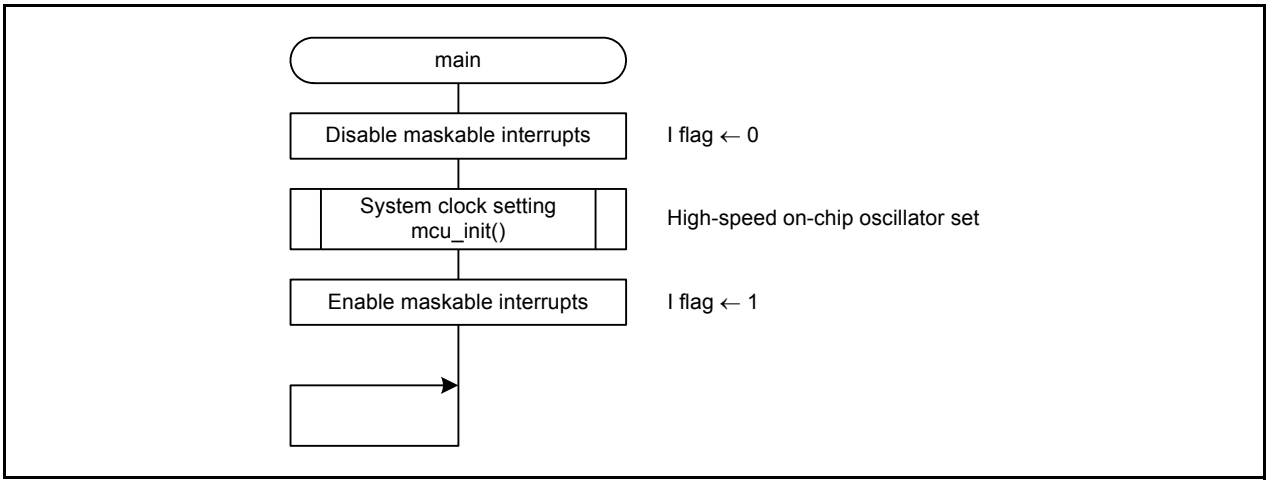

Figure 3.2 Main Processing

3.3.2 System Clock Setting

Figure 3.3 shows the System Clock Setting.

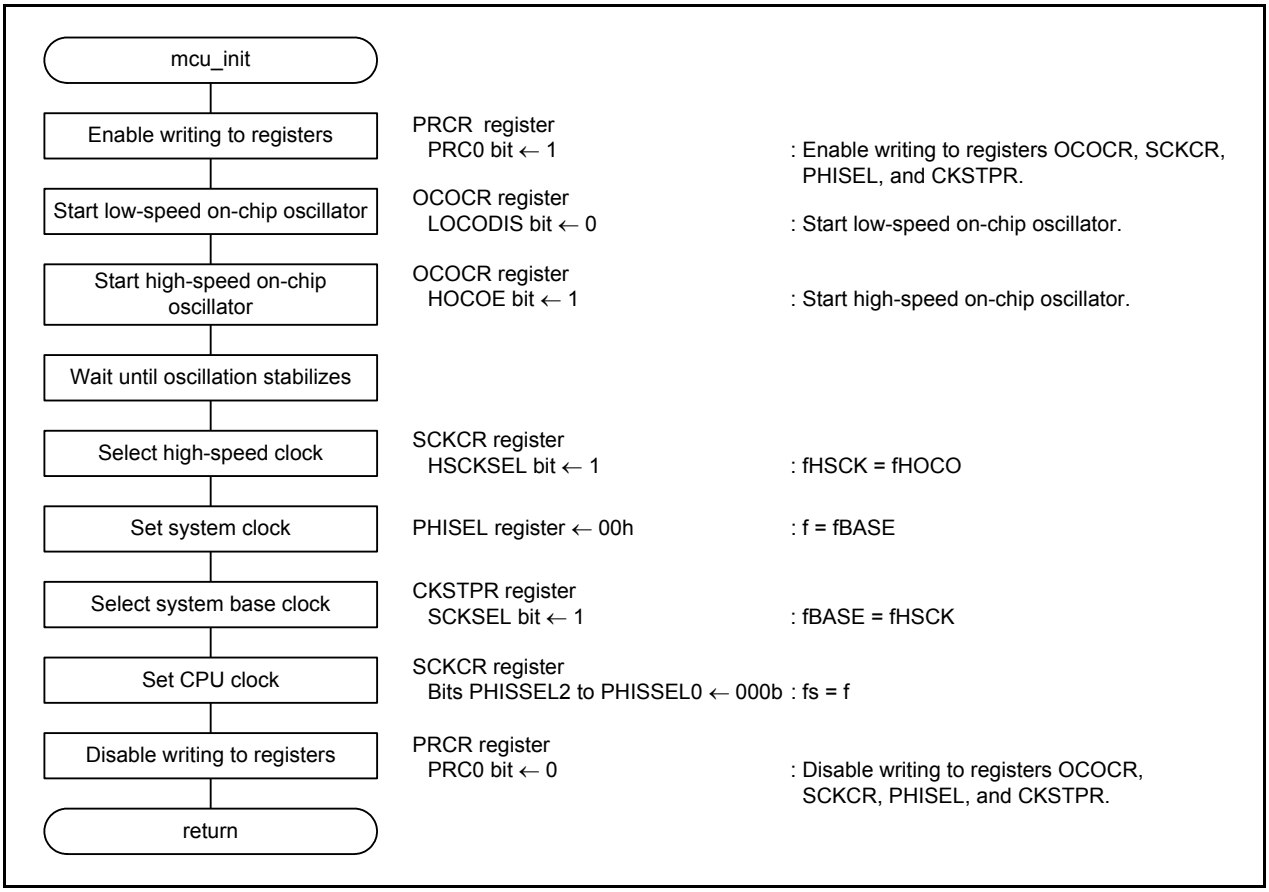

Figure 3.3 System Clock Setting

4. Software: Sample Program 2

4.1 Operation Overview

(1) No division of fLOCO (low-speed on-chip oscillator) is automatically selected for fBASE (system base clock) after reset.
(2) Set 08h to the PHISEL register and select fBASE divided-by-8 of for f (system clock).
(3) Set the SCKSEL bit in the CKSTPR register to 0 and select fLOCO for fBASE.
(4) Set bits PHISSEL2 to PHISSEL0 in the SCKCR register to 000b and select no division of f for fs (CPU clock).

Refer to r01an0092_src_sample2.c for a sample program.

Figure 4.1 shows the Timing Diagram of the Sample Program 2 Setting.

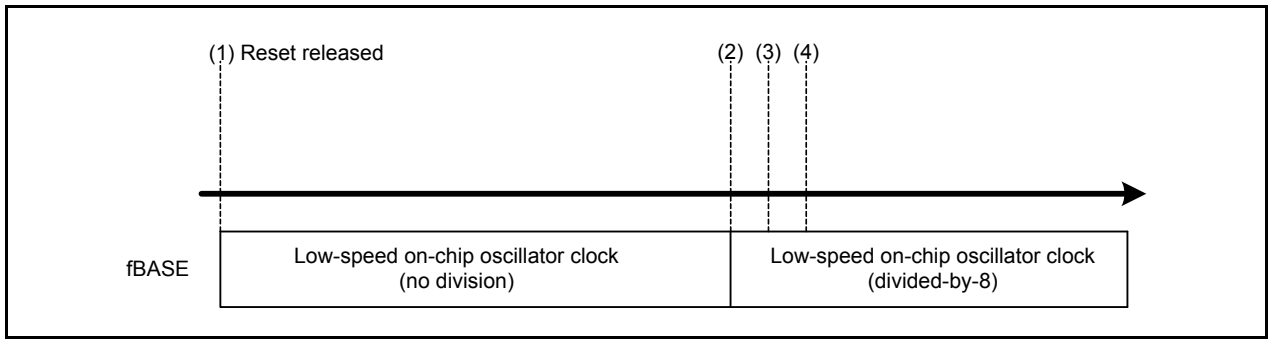

Figure 4.1 Timing Diagram of the Sample Program 2 Setting

4.2 Required Memory Size

Table 4.1 lists the Required Memory Size.

Table 4.1 Required Memory Size

Memory Used	Size	Remarks
ROM	44 bytes	In the r01an0092_src_sample2.c module
RAM	0 bytes	In the r01an0092_src_sample2.c module
Maximum user stack usage	6 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

4.3 Flowcharts

4.3.1 Main Processing

Figure 4.2 shows the Main Processing.

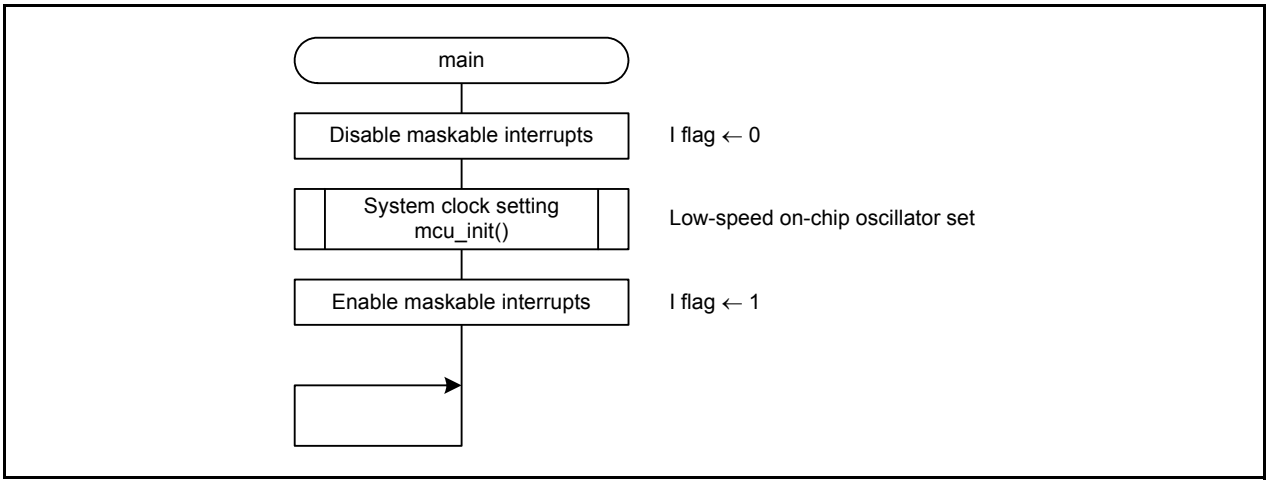

Figure 4.2 Main Processing

4.3.2 System Clock Setting

Figure 4.3 shows the System Clock Setting.

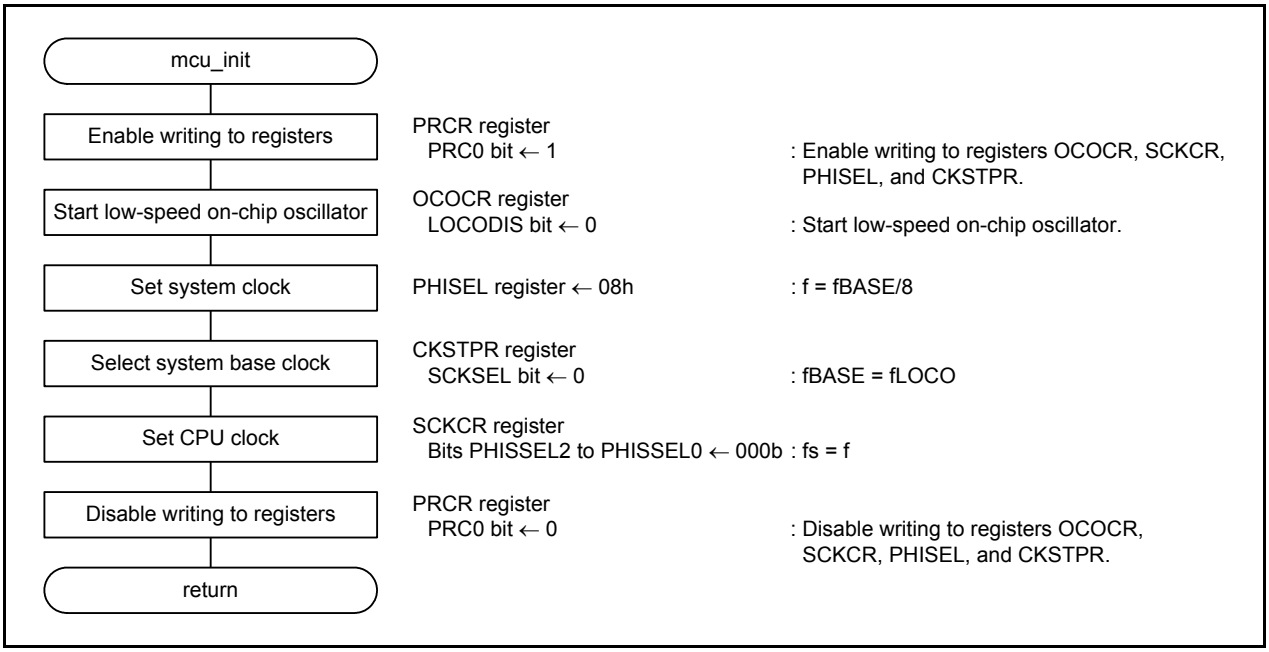

Figure 4.3 System Clock Setting

5. Software: Sample Program 3

5.1 Operation Overview

(1) No division of fLOCO (low-speed on-chip oscillator) is automatically selected for fBASE (system base clock) after reset.
(2) Set bits CKPT1 and CKPT0 in the EXCKCR register to 11b (P4_6: XIN, P4_7: XOUT), start fXIN (XIN clock), and wait until oscillation stabilizes by a program.
(3) Set the HSCKSEL bit in the SCKCR register to 0 and select fXIN for fHSCK (high-speed clock).
(4) Set 00h to the PHISEL register and select no division of fBASE for f (system clock).
(5) Set the SCKSEL bit in the CKSTPR register to 1 and switch fBASE from fLOCO to fHSCK.
(6) Set bits PHISSEL2 to PHISSEL0 in the SCKCR register to 000b and select no division of f for fs (CPU clock).

Refer to r01an0092_src_sample3.c for a sample program.

Figure 5.1 shows the Timing Diagram of the Sample Program 3 Setting.

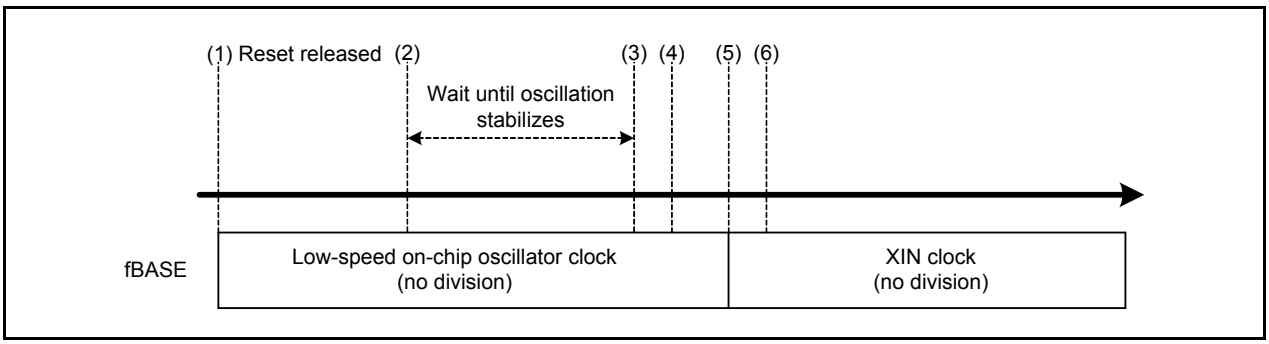

Figure 5.1 Timing Diagram of the Sample Program 3 Setting

5.2 Required Memory Size

Table 5.1 lists the Required Memory Size.

Table 5.1 Required Memory Size

Memory Used	Size	Remarks
ROM	70 bytes	In the r01an0092_src_sample3.c module
RAM	0 bytes	In the r01an0092_src_sample3.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

5.3 Flowcharts

5.3.1 Main Processing

Figure 5.2 shows the Main Processing.

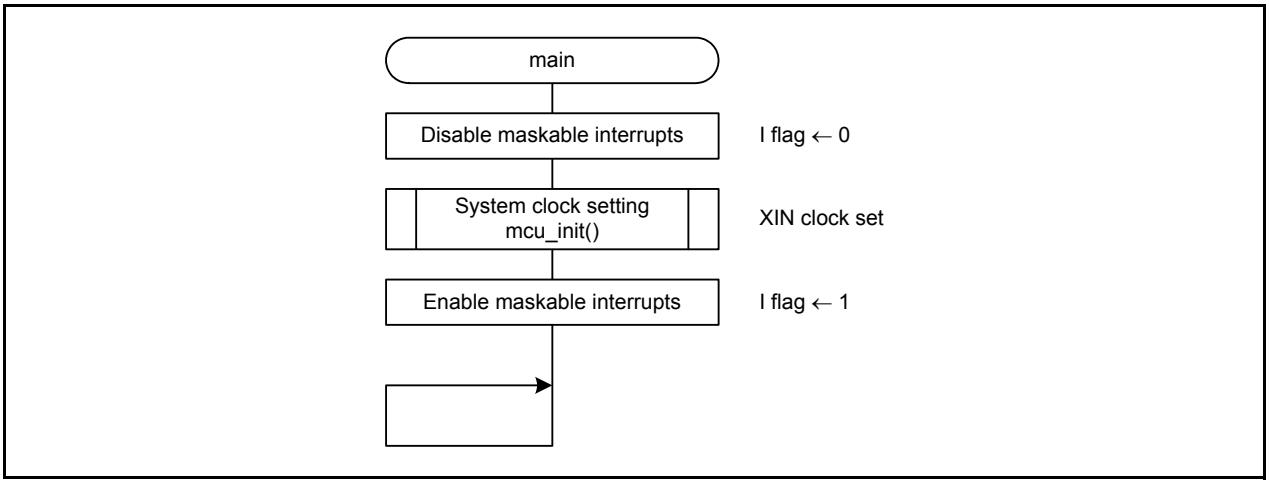

Figure 5.2 Main Processing

5.3.2 System Clock Setting

Figure 5.3 shows the System Clock Setting.

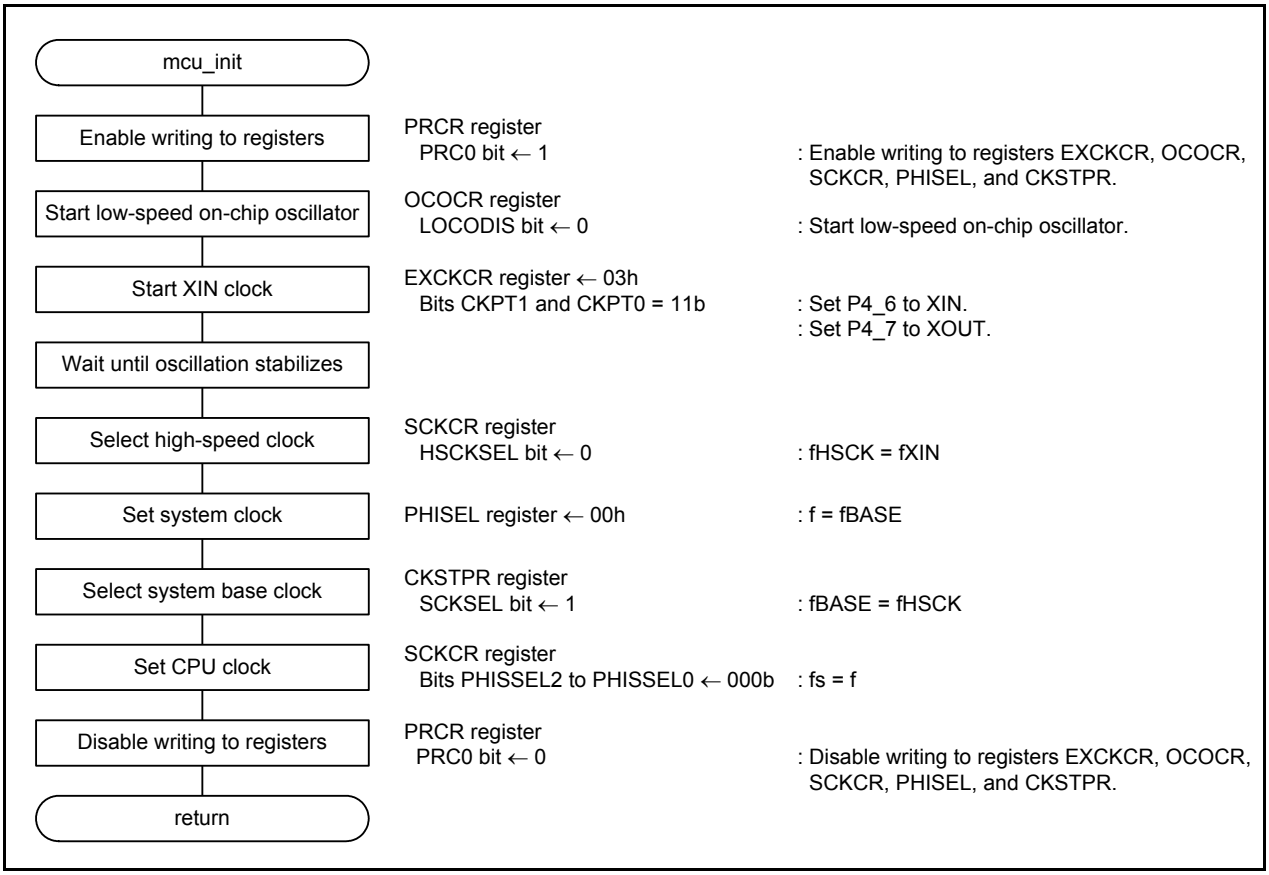

Figure 5.3 System Clock Setting

6. Software: Sample Program 4

6.1 Operation Overview

(1) No division of fLOCO (low-speed on-chip oscillator) is automatically selected for fBASE (system base clock) after reset.

mcu_init(): System clock setting

(2) Set bits CKPT1 and CKPT0 in the EXCKCR register to11b (P4_6: XIN, P4_7: XOUT), start fXIN (XIN clock), and wait until oscillation stabilizes by a program.
(3) Set the HSCKSEL bit in the SCKCR register to 0 and select fXIN for fHSCK (high-speed clock).
(4) Set 00h to the PHISEL register and select no division of fBASE for f (system clock).
(5) Set the SCKSEL bit in the CKSTPR register to 1 and switch fBASE from fLOCO to fHSCK.
(6) Set bits PHISSEL2 to PHISSEL0 in the SCKCR register to 000b and select no division of f for fs (CPU clock).

clock_change(): System base clock switching

(7) Set the HOCOE bit in the OCOCR register to 1, start fHOCO (high-speed on-chip oscillator), and wait until oscillation stabilizes by a program.
(8) Set the HSCKSEL bit in the SCKCR register to 1 and switch fHSCK from fXIN to fHOCO.
(9) Set 00h to the PHISEL register and select no division of fBASE for f.
(10) Set the SCKSEL bit in the CKSTPR register to 1 and select fHSCK for fBASE.
(11) Set bits PHISSEL2 to PHISSEL0 in the SCKCR register to 000b and select no division of f for fs.

Refer to r01an0092_src_sample4.c for a sample program.

Figure 6.1 shows the Timing Diagram of the Sample Program 4 Setting.

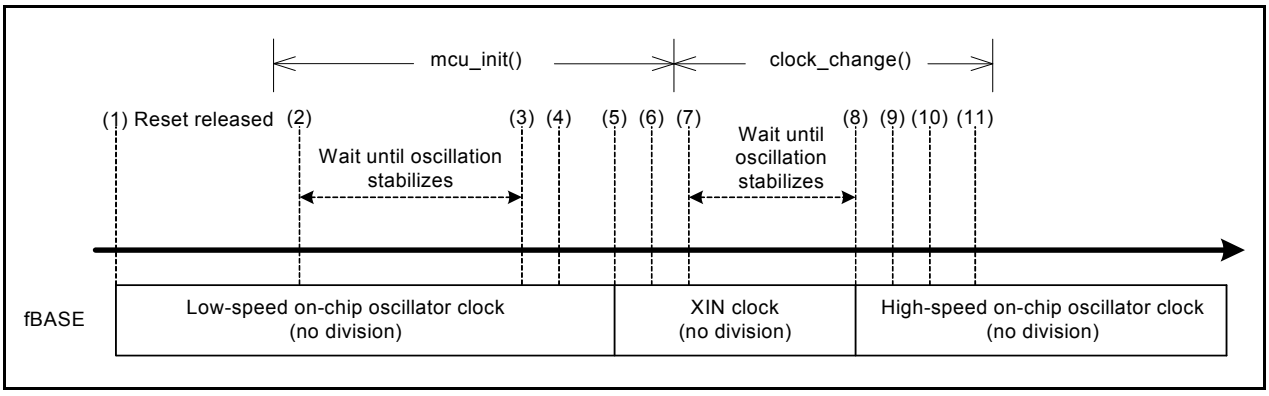

Figure 6.1 Timing Diagram of the Sample Program 4 Setting

6.2 Required Memory Size

Table 6.1 lists the Required Memory Size.

Table 6.1 Required Memory Size

Memory Used	Size	Remarks
ROM	128 bytes	In the r01an0092_src_sample4.c module
RAM	0 bytes	In the r01an0092_src_sample4.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	0 bytes	

The required memory size varies depending on the C compiler version and compile options.

6.3 Functions

Table 6.2 lists the Functions.

Table 6.2 Functions

Function Name	Outline
mcu_init	System clock setting
clock_change	System base clock switching

6.4 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	System clock setting
Header	None
Declaration	void mcu_init(void)
Description	Set the system clock.
Argument	None
Returned value	None
Remark	—

clock_change	
Outline	System base clock switching
Header	None
Declaration	void clock_change(void)
Description	Set the high-speed on-chip oscillator (no division) for the system base clock.
Argument	None
Returned value	None
Remark	—

6.5 Flowcharts

6.5.1 Main Processing

Figure 6.2 shows the Main Processing.

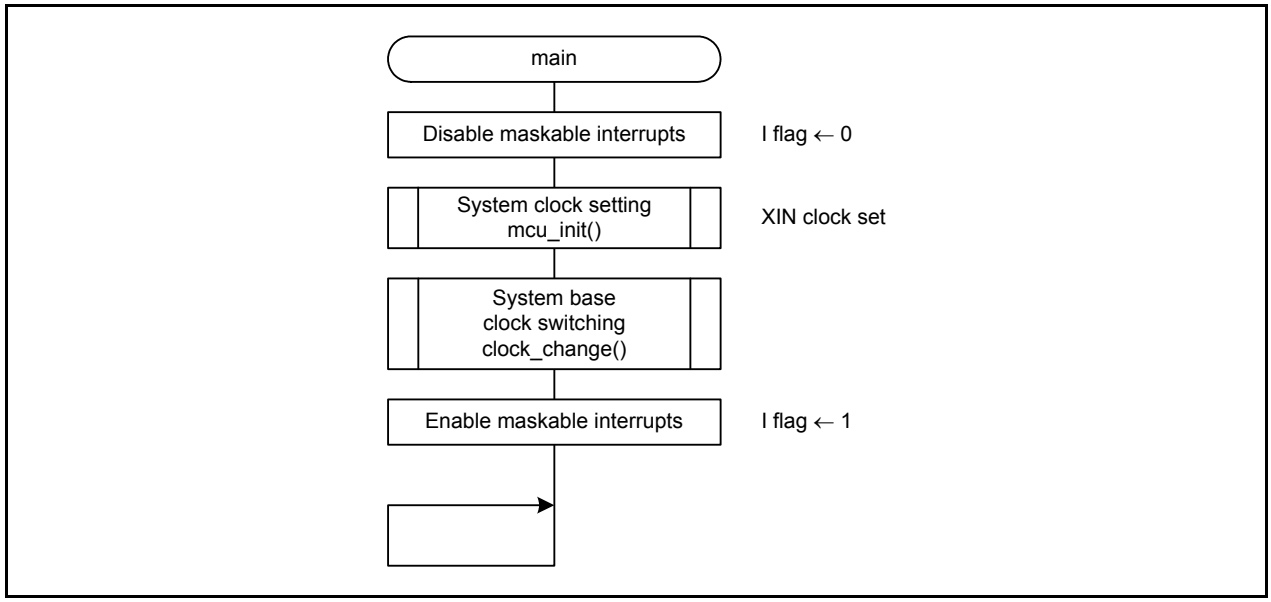

Figure 6.2 Main Processing

6.5.2 System Clock Setting

Figure 6.3 shows the System Clock Setting.

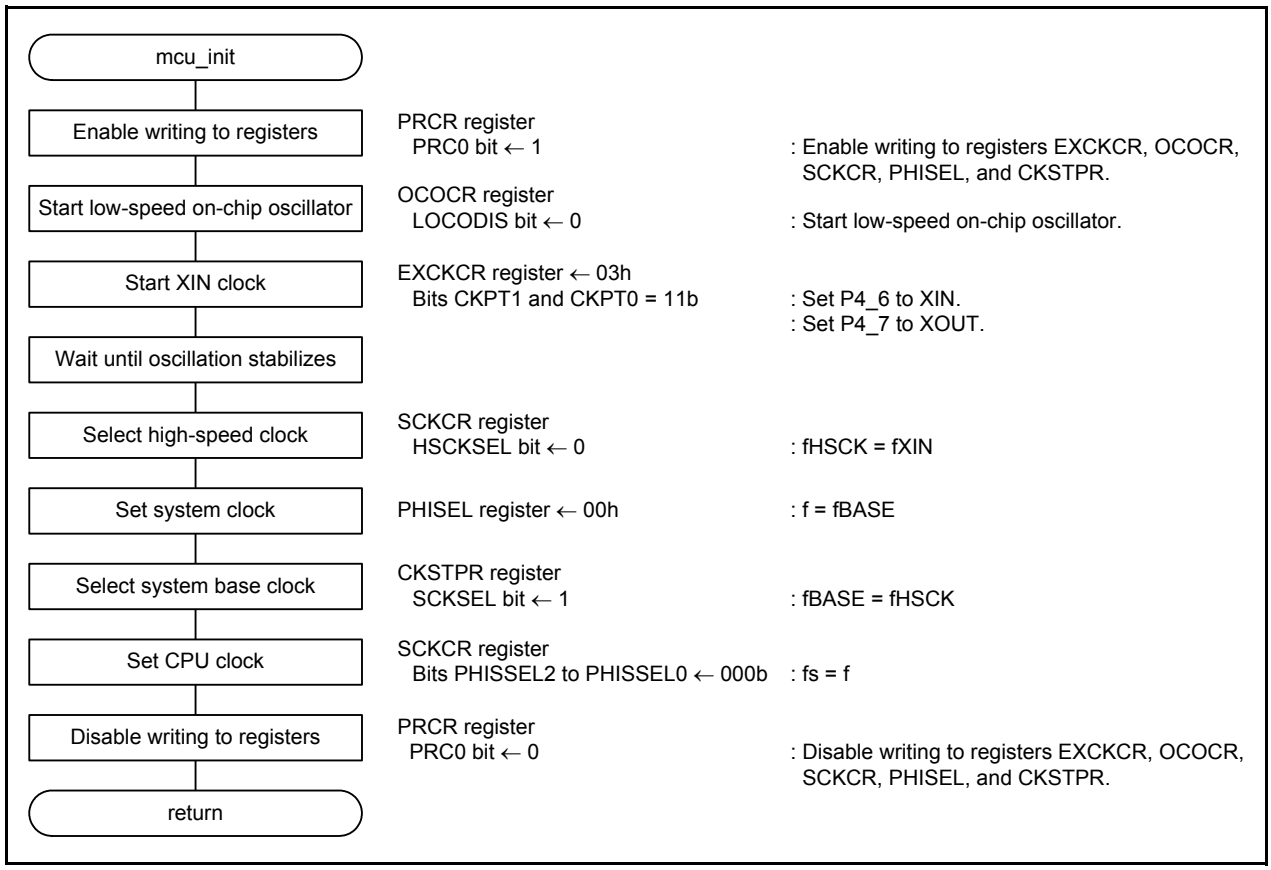

Figure 6.3 System Clock Setting

6.5.3 System Base Clock Switching

Figure 6.4 shows the System Base Clock Switching.

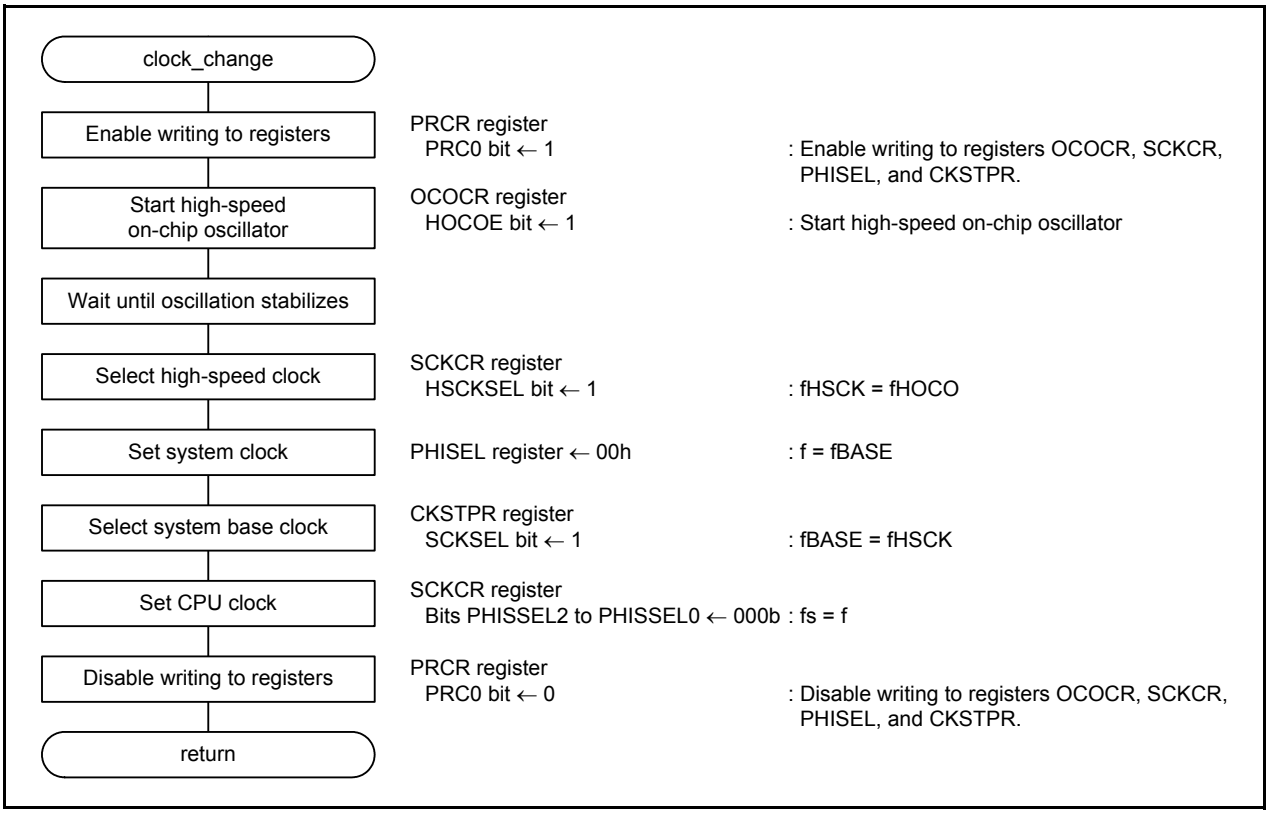

Figure 6.4 System Base Clock Switching

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

R8C/M12A Group User's Manual: Hardware Rev.1.02
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
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Revision History	R8C/M12A Group Setting Example of System Base Clock

Rev.	Date	Description	
		Page	Summary
1.00	July 19, 2011	—	First edition issued

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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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