R8C/L38M Group, R8C/LA8A Group, RL78/L13

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Peripheral Function Comparison between R8C/L38M Group, R8C/LA8A Group, and RL78/L13

Abstract

This document describes the peripheral function comparison between R8C/L38M Group, R8C/LA8A Group, and RL78/L13.

Products

R8C Family: R8C/L38M Group, R8C/LA8A Group

RL78 Family: RL78/L13 (80-pin package)

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Peripheral Function Comparison

Table 1.1 to Table 1.4 list the peripheral function comparison between the R8C/L38M Group, R8C/LA8A Group, and RL78/L13 MCUs.

In this application note, peripheral functions of the RL78/L13 are compared to the peripheral functions of the R8C/L38M Group and R8C/LA8A Group in order to show a guideline when replacing the R8C Family with the RL78 Family. Tables comparing the peripheral functions show which peripheral functions of the R8C/L38M Group and R8C/LA8A Group apply to the peripheral functions of the RL78/L13. A comparison of CPU cores is not included in the tables.

For more details on RL78/L13 peripheral functions, refer to the documents listed in 2 Reference Documents.

Table 1.1 Peripheral Function Comparison (1/4)

Item		R8C/L38M Group (80-pin)	R8C/LA8A Group (80-pin)	RL78/L13 (80-pin)
Resets		Hardware reset		External reset input by the RESET pin
		Power-on reset		Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
		Voltage monitor 0 reset		Internal reset by comparison of supply voltage and detection voltage of the voltage detector (LVD)
		Watchdog timer reset		Internal reset by watchdog timer program loop detection
		Software reset		N/A
		N/A		Internal reset by execution of illegal instruction
		N/A		Internal reset by RAM parity error
		N/A		Internal reset by illegal-memory access
Voltage Detection Circuit	Voltage monitor 0	Voltage monitor 0 reset		Voltage detector, LVD (reset mode) Voltage detector, LVD (interrupt & reset mode)
	Voltage monitor 1	Voltage monitor 1 interrupt		Voltage detector, LVD (interrupt mode)
	Voltage monitor 2	Voltage monitor 2 interrupt		Voltage detector, LVD (interrupt mode)
Ports	I/O control	Port Pi direction register (i = 0 to 7, 10 to 13)	Port Pi direction register (i = 0 to 9)	Port mode register (i = 0 to 7, 12, 13)
		N/A		Digital I/O, analog input
	Input port	Pull-up control		Pull-up resistor option
		Input threshold control		TTL input buffer is selectable
	Output port	Drive capacity control		N/A
		N/A		N-ch open drain output is selectable
Clocks	External oscillator	XIN clock generation circuit (0 to 20 MHz)		X1 oscillator (1 to 20 MHz)
	External sub-oscillator	XCIN clock generation circuit (32.768 kHz)		XT1 oscillator (32.768 kHz)
	On-chip oscillation circuit (high-speed)	High-speed on-chip oscillator (40 MHz, divide-by-2 to 9 can be selected)	High-speed on-chip oscillator (20 MHz, divide-by-1 to 8 can be selected)	High-speed on-chip oscillator (Its frequency can be selected from 48, 24, 16, 12, 8, 4, and 1 MHz)
	On-chip oscillator circuit	Low-speed on-chip oscillator (125 kHz)		Low-speed on-chip oscillator (15 kHz)
	Enable/disable peripheral clock provision	• Timer RA • Timer RB • Timer RC • Timer RD • Timer RG • A/D converter	• Timer RB0 • Timer RB1 • Timer RC • Timer RH • Timer RJ0 • Timer RJ1 • Timer RJ2 • Serial interface (UART0) • Serial interface (UART2) • Clock synchronous serial interface • A/D converter • LCD drive control circuit	• High accuracy real-time clock • A/D converter • Serial interface IICA0 • Serial array unit 1 (SAU1) • Serial array unit 0 (SAU0) • Timer array unit (TAU) • 12-bit interval timer • Comparators 0 and 1 • 16-bit timer KB20
Power Control/ Standby Function	Operating current reduce function	Wait mode		HALT mode
		Stop mode		STOP mode
		Power-off mode	Power-off 0 mode	N/A
		N/A	Power-off 2 mode	N/A
		N/A		SNOOZE mode
Protect/ Safety Functions	Register protect function	Protection by the protect register (Registers related to clock, reset, A/D converter, voltage detection are protected)		SFR guard function (Registers related to ports, interrupts, clock control, voltage detector, RAM parity error detection are protected)
	RAM guard function	N/A		RAM guard function
	Data error detection	N/A		Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
	Parity error detection	N/A		RAM parity error detection function
	Illegal access detection	N/A		Invalid memory access detection function
	Frequency detection	N/A		Frequency detection function
	A/D test function	N/A		A/D test function
	I/O function check	N/A		Digital output signal level detection function for I/O ports
Interrupts	Non-maskable interrupts	Undefined instruction interrupt		N/A
		Overflow interrupt		N/A
		BRK instruction interrupt		BRK instruction execute interrupt
		INT instruction interrupt		N/A
		Watchdog timer interrupt		Watchdog timer interval interrupt
		Oscillation stop detection interrupt		N/A
		Voltage monitor 1 interrupt/comparator A1 interrupt	Voltage monitor 1 interrupt	N/A
		Voltage monitor 2 interrupt/comparator A2 interrupt	Voltage monitor 2 interrupt	N/A
		Address match interrupt		N/A
	Maskable interrupts	Voltage monitor 1 interrupt		Voltage detector, LVD (interrupt & reset mode) Voltage detector, LVD (interrupt mode)
		Voltage monitor 2 interrupt		Voltage detector, LVD (interrupt & reset mode) Voltage detector, LVD (interrupt mode)
		Peripheral function interrupt		Peripheral function interrupt
	INT interrupt	INT interrupt input (INT0 to INT7) (INT input filter is available. Both edges, rising and falling edges are selectable)		Pin input edge detection (INTP0 to INTP7) (input filter is not available. Both edges, rising and falling edges are selectable.)
	Key input interrupt	Key input interrupt (KI0 to KI7) (Specify the falling edge or rising edge)		Key interrupt input (KR0 to KR7) (Specify the falling edge or rising edge)

Table 1.2 Peripheral Function Comparison (2/4)

Item		R8C/L38M Group (80-pin)	R8C/LA8A Group (80-pin)	RL78/L13 (80-pin)
Option Function Select Area/Option Byte	Watchdog timer	• Start or stop the watchdog timer (after reset) • Set the watchdog timer underflow period • Set the watchdog timer refresh acknowledgement period • Enable or disable count source protection mode after reset		• Disable or enable the watchdog timer count operation after a reset is released • Disable or enable the watchdog timer count operation in HALT or STOP mode • Set the watchdog timer overflow time • Set the watchdog timer window open period • Use or not use the watchdog timer interval interrupt
	Parallel I/O mode access control	Enable or disable the ROM code protect		N/A
	Voltage detection	• Select voltage detection 0 level • Enable or disable voltage detection 0 circuit		• Set the LVD operating mode (interrupt & reset mode, reset mode, or interrupt mode) • Set the LVD detection level (VLVDH, VLVDL, or VLVD)
	Flash memory	N/A		• Set the flash memory operating mode (LV mode, LS mode, or HS mode) • Handle the data in flash memory when the security ID authentication failed
	High-speed on-chip oscillator	N/A		Set the high-speed on-chip oscillator frequency (1 MHz, 4 MHz, 8 MHz, 12 MHz, 16 MHz or 24 MHz)
	On-chip debug	N/A		Disable or enable the on-chip debug operation
Watchdog Timer	Count source	Count source protection mode can be enabled or disabled • When count protection mode is disabled: CPU clock is specified as the count source • When count protection mode is enabled: Low-speed on-chip oscillator clock for watchdog timer is specified as the count source		Low-speed on-chip oscillator is specified as the count source
	Interrupt source	• At underflow • Writing in other than the refresh acknowledgement period		Interval interrupt is generated when the watchdog timer reaches 75% of the overflow time
	Reset source	• At underflow • Writing in other than the refresh acknowledgement period		Internal reset when a program loop is detected • At overflow • 1-bit manipulation instruction to the WDTE register is executed • When the data other than "ACH" is written to the WDTE register • When data is written to the WDTE register during a window close period
	Count stop condition	• When count protection mode is disabled: stop mode, wait mode • When count protection mode is enabled: none		When the WDSTBYON bit is 0: HALT mode, STOP mode or SNOOZE mode
	Count start condition	• After a reset, count starts automatically • Count starts by writing to the WDTS register		Count starts after a reset is released
Data Transfer Function	Function	DTC (Data transfer controller)	N/A	DMA (Direct Memory Access)
	Unit of transfers	Byte	N/A	8-bit or 16-bit
	Transfer mode	• Normal mode • Repeat mode	N/A	Single transfer mode
	Maximum number of transfer times	• Normal mode: 256 • Repeat mode: 255	N/A	1024
	Address space where can be transferred	64-KB space (00000h to 0FFFFh)	N/A	Data can be transferred between SFR and internal RAM
	Activation sources	38	N/A	12
	Operation at standby	DTC cannot be used in wait mode or stop mode	N/A	• HALT mode: normal operation • STOP mode: operation stopped
Timers	Timer RA (8-bit timer with an 8-bit prescaler)	Timer RA (timer mode)	Timer RJ (timer mode)	• TAU interval timer (channels 0 to 7) • 12-bit interval timer
		Timer RA (pulse output mode)	Timer RJ (pulse output mode)	• TAU, square wave output (channels 0 to 7)
		Timer RA (event counter mode)	Timer RJ (evemt counter mode)	• TAU, external event counter (channels 0 to 7)
		Timer RA (pulse width measurement mode)	Timer RJ (pulse width measurement mode)	• TAU, measurement of high-/low-level width of input signal (channels 0 to 7)
		Timer RA (pulse period measurement mode)	Timer RJ (pulse period measurement mode)	• TAU, input pulse interval measurement (channels 0 to 7)
	Timer RB (8-bit timer with an 8-bit prescaler)	Timer RB (timer mode)		• TAU, interval timer (channels 0 to 7) • 12-bit interval timer
		Timer RB (programmable waveform generation mode)		• TAU, square wave output (channels 0 to 7) • TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
		Timer RB (programmable one-shot generation mode)		• TAU, one-shot pulse output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7)
		Timer RB (programmable wait one-shot generation mode)		• TAU, one-shot pulse output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7)
	Timer RC (16-bit timer)	Timer RC (timer mode, input capture function)		• TAU, input pulse interval measurement (channels 0 to 7) • TAU, measurement of high-/low-level width of input signal (channels 0 to 7)
		Timer RC (timer mode, output compare function)		• TAU, square wave output (channels 0 to 7) • TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
		Timer RC (PWM mode)		• TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
		Timer RC (PWM2 mode)		• TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • TAU, one-shot pulse output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output

Table 1.3 Peripheral Function Comparison (3/4)

Item			R8C/L38M Group (80-pin)	R8C/LA8A Group (80-pin)	RL78/L13 (80-pin)
Timers	Timer RD (16-bit timers: 2)		Timer RD (timer mode, input capture function)	N/A	• TAU, input pulse interval measurement (channels 0 to 7) • TAU, measurement of high-/low-level width of input signal (channels 0 to 7)
			Timer RD (timer mode, output compare function)	N/A	• TAU, square wave output (channels 0 to 7) • TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
			Timer RD (PWM mode)	N/A	• TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
			Timer RD (reset synchronous PWM mode)	N/A	• TAU, multiple PWM output (channels 0, 1, and 2; channels 0, 2, and 3; channels 0, 3, and 4; channels 0, 4, and 5; channels 0, 5, and 6; channels 0, 6, and 7; channels 2, 3, and 4; channels 2, 4, and 5; channels 2, 5, and 6; channels 2, 6, and 7; channels 4, 5, and 6; channels 4, 6, and 7)
			Timer RD (complementary PWM mode)	N/A	N/A
			Timer RD (PWM3 mode)	N/A	N/A
	Timer RE (4-bit counter, 8-bit counter)		Timer RE (real-time clock mode)	Timer RH (real-time clock mode)	High accuracy real-time clock
			Timer RE (output compare mode)	Timer RH (output compare mode)	• TAU, square wave output (channels 0 to 7) • TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7)
	Timer RG (16-bit timer)		Timer RG (timer mode, input capture function)	N/A	• TAU, input pulse interval measurement (channels 0 to 7) • TAU, measurement of high-/low-level width of input signal (channels 0 to 7) • 16-bit timer KB20, PWM output
			Timer RG (timer mode, output compare function)	N/A	• TAU, square wave output (channels 0 to 7) • TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7)
			Timer RG (PWM mode)	N/A	• TAU, PWM output (channel 0: 1 to 7, channel 2: 3 to 7, channel 4: 5 to 7, channel 6: 7) • 16-bit timer KB20, PWM output
			Timer RG (phase counting mode)	N/A	TAU, external event counter (channels 0 to 7)
	Delay counter		N/A		TAU, delay counter (channels 0 to 7)
	Clock output/buzzer output		N/A		Clock output/buzzer output controller (pins PCLBUZ0 and 1)
	Remote control output		N/A		TAU, remote control output function (channel 2: 3, channel 4: 5)
	16-bit timer KB20		• Timer RC (PWM mode) • Timer RC (PWM2 mode) • Timer RD (PWM mode) • Timer RD (PWM3 mode) • Timer RG (PWM mode)	• Timer RC (PWM mode) • Timer RC (PWM2 mode)	PWM output
			N/A		Timer restart function
			N/A		Forced output stop function 1 and 2
			N/A		Dithering function
			N/A		Smooth start function
			N/A		Maximum frequency setting function
			N/A		Interleave function
Communication	Serial interface UART0		Clock synchronous serial I/O mode		Serial array unit (SAU), 3-wire serial I/O CSI00 (channel 0 in unit 0) CSI10 (channel 2 in unit 0)
			Clock asynchronous serial I/O mode (UART mode)		SAU, UART UART0 (channel 0 in unit 0 and channel 1 in unit 0) UART1 (channel 2 in unit 0 and channel 3 in unit 0) UART2 (channel 0 in unit 1 and channel 1 in unit 1) UART3 (channel 2 in unit 1 and channel 3 in unit 1)
	Serial interface UART1		Clock synchronous serial I/O mode	N/A	SAU, 3-wire serial I/O CSI00 (channel 0 in unit 0) CSI10 (channel 2 in unit 0)
			Clock asynchronous serial I/O mode (UART mode)	N/A	SAU, UART UART0 (channel 0 in unit 0 and channel 1 in unit 0) UART1 (channel 2 in unit 0 and channel 3 in unit 0) UART2 (channel 0 in unit 1 and channel 1 in unit 1) UART3 (channel 2 in unit 1 and channel 3 in unit 1)
	Serial interface UART2		Clock synchronous serial I/O mode		SAU, 3-wire serial I/O CSI00 (channel 0 in unit 0) CSI10 (channel 2 in unit 0)
			Clock asynchronous serial I/O mode (UART mode)		SAU, UART UART0 (channel 0 in unit 0 and channel 1 in unit 0) UART1 (channel 2 in unit 0 and channel 3 in unit 0) UART2 (channel 0 in unit 1 and channel 1 in unit 1) UART3 (channel 2 in unit 1 and channel 3 in unit 1)
			Special mode 1 (I^2C mode)		• SAU, simplified I^2C IIC00 (channel 0 in unit 0) IIC10 (channel 2 in unit 0) • Serial interface IICA
			Multiprocessor communication function		N/A
	Clock synchronous serial interface (SSU and I2C bus interface cannot be used concurrently in the R8C)	Synchronous serial communication unit (SSU)	Clock synchronous communication mode		SAU, 3-wire serial I/O CSI00 (channel 0 in unit 0) CSI10 (channel 2 in unit 0)
			4-wire bus communication mode (standard mode)		N/A
			4-wire bus communication mode (bidirectional mode)		N/A
		I2C bus interface	I^2C bus interface mode		• SAU, simplified I^2C IIC00 (channel 0 in unit 0) IIC10 (channel 2 in unit 0) • Serial interface IICA
			Clock synchronous serial mode		SAU, 3-wire serial I/O CSI00 (channel 0 in unit 0) CSI10 (channel 2 in unit 0)
	Hardware LIN		LIN communication in conjunction with timer RA and UART0	N/A	SAU, UART UART0 (channel 0 in unit 0 and channel 1 in unit 0)

Table 1.4 Peripheral Function Comparison (4/4)

Item		R8C/L38M Group (80-pin)	R8C/LA8A Group (80-pin)	RL78/L13 (80-pin)
Analog Conversion	A/D converter	One-shot mode		One-shot conversion mode
		Repeat mode 0		Sequential conversion mode
		Repeat mode 1		N/A
		Single sweep mode		N/A
		Repeat sweep mode		N/A
	D/A converter	D/A converter	N/A	N/A
	Comparator A	Comparison between a reference input voltage and an analog input voltage	N/A	Comparators 0 and 1 (comparison between a reference input voltage and an analog input voltage)
	Comparator B	Comparison between a reference input voltage and an analog input voltage		Comparators 0 and 1 (comparison between a reference input voltage and an analog input voltage)
LCD Drive Control Circuit	Output	Segment output: maximum of 48 pins Common output: maximum of 8 pins	Segment output: maximum of 40 pins Common output: maximum of 4 pins	Segment output: maximum of 51 pins Common output: maximum of 8 pins
	LCD drive voltage generator (internal voltage multiplier/external division resistor)	• External division resistor • Internal voltage multiplier	External division resistor	• External resistance division method • Internal voltage boosting method • Capacitor split method
Flash Memory	1-wire programming	Standard serial I/O mode 3		Flash memory programming mode (single-line UART)
	UART programming	Standard serial I/O mode 2		Flash memory programming mode (UART for external device connection)
	Parallel I/F	Parallel I/O mode		N/A
	Software programming	CPU rewrite mode		Flash memory programming by self-programming
	Security function	• ID code check function (standard serial I/O mode) • ROM code protect function (parallel I/O mode) • Data protect function (CPU rewrite mode)		• Block erase protection • Write protection • Boot cluster 0 rewrite protection • Flash shield window function • On-chip debug security ID
Multiplier and Divider/Multiply-Accumulator		N/A		Provided

2. Reference Documents

User's Manual: Hardware

R8C/L35M Group, R8C/L36M Group, R8C/L38M Group, R8C/L3AM Group User's Manual: Hardware Rev.1.00
R8C/LA8A Group, R8C/LA8A Group User's Manual: Hardware Rev.1.03
RL78/L13 User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R8C/L38M Group, R8C/LA8A Group, RL78/L13 Peripheral Function Comparison between R8C/L38M Group, R8C/LA8A Group, and RL78/L13

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		Page	Summary
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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Colophon 2.2