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R8C/38C Group

Timer RG Timer Mode (Output Compare Function)

1. Abstract

This document describes the setting method and an application example for toggle output using timer RG's timer mode (output compare function) in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/38C Group

The sample program in this application note can be used with other R8C/38C Group MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

3.1 Program Outline

The TRGIOA pin outputs the pulse which toggles in 100 µs intervals by a compare match between the timer RG counter register (TRG) and timer RG general register A (TRGGRA).

Main settings

• The high-speed on-chip oscillator (fOCO40M) is used as count source.
• The timer RG counter (TRG) is cleared by a compare match with the general register (TRGGRA).

Formula for setting time

100 µs = 1 ÷ fOCO40M × (TRGGRA register value + 1)
= 1 ÷ 40 MHz × (3999 + 1)
= 25 ns × 4000

Figure 3.1 shows the block diagram, Figure 3.2 shows the timing chart, and Table 3.1 shows the pin used and its function.

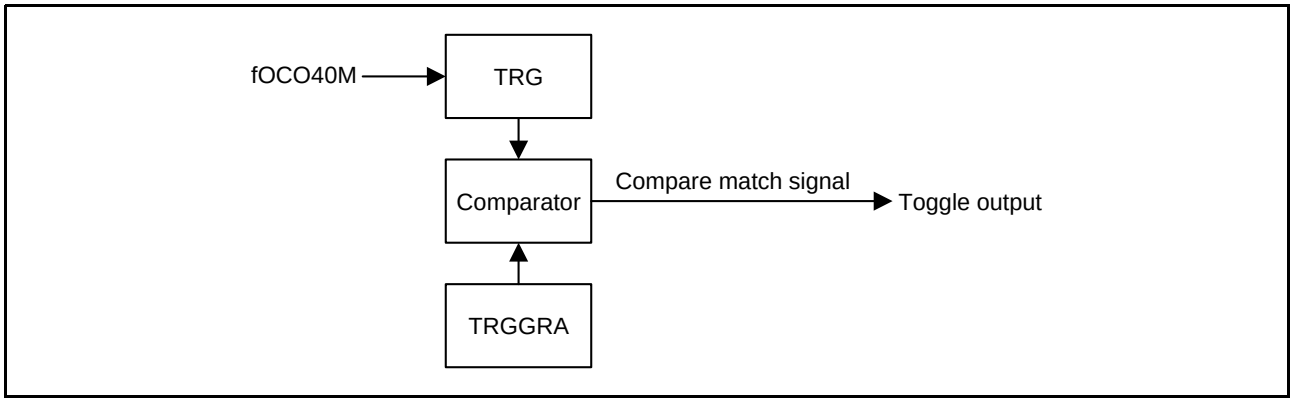


Figure 3.1 Block Diagram

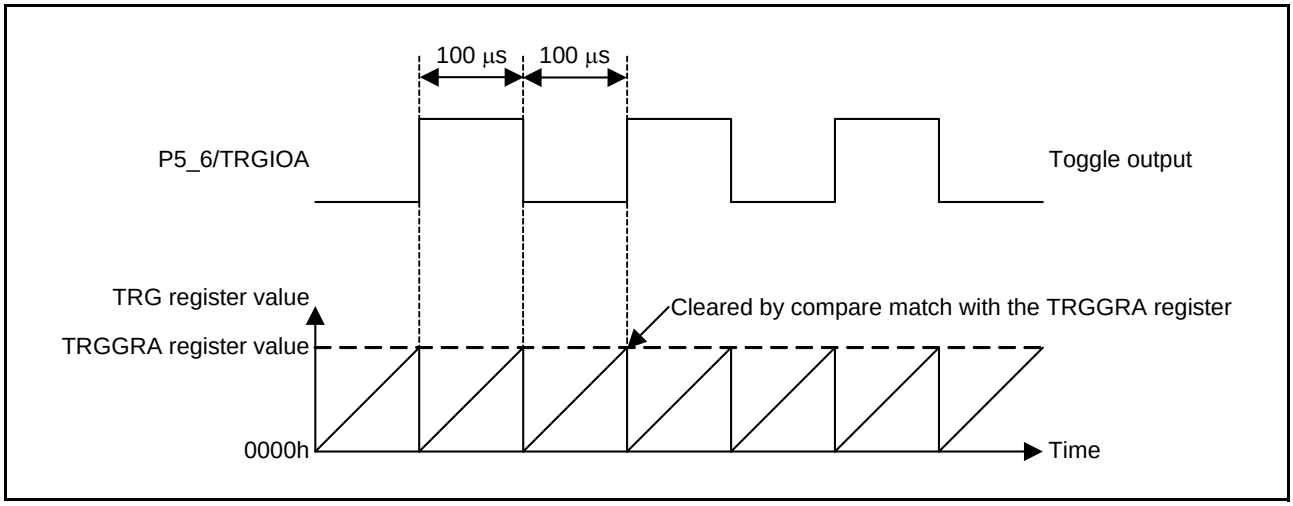


Figure 3.2 Timing Chart

Table 3.1 Pin and Function

Pin Name	I/O	Function
P5_6/TRGIOA	Output	Toggle output

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	140 bytes	In the rej05b1157_src.c module
RAM	0 bytes	In the rej05b1157_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
• C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.45 Release 00
• Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software Description

This section shows the setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

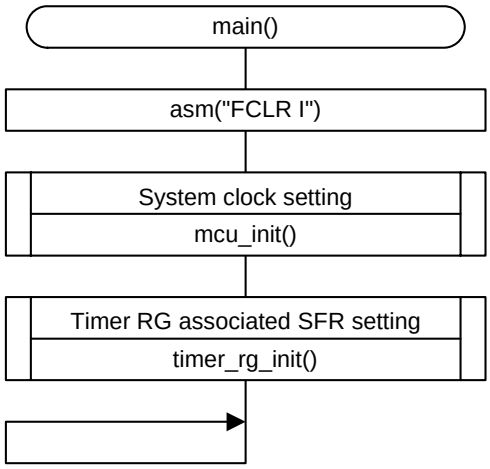
4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Content
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

Declaration	void timer_rg_init(void)		
Outline	Timer RG associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Content
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is set to use the timer RG in output compare function.		

4.2 Main Function

- Flowchart



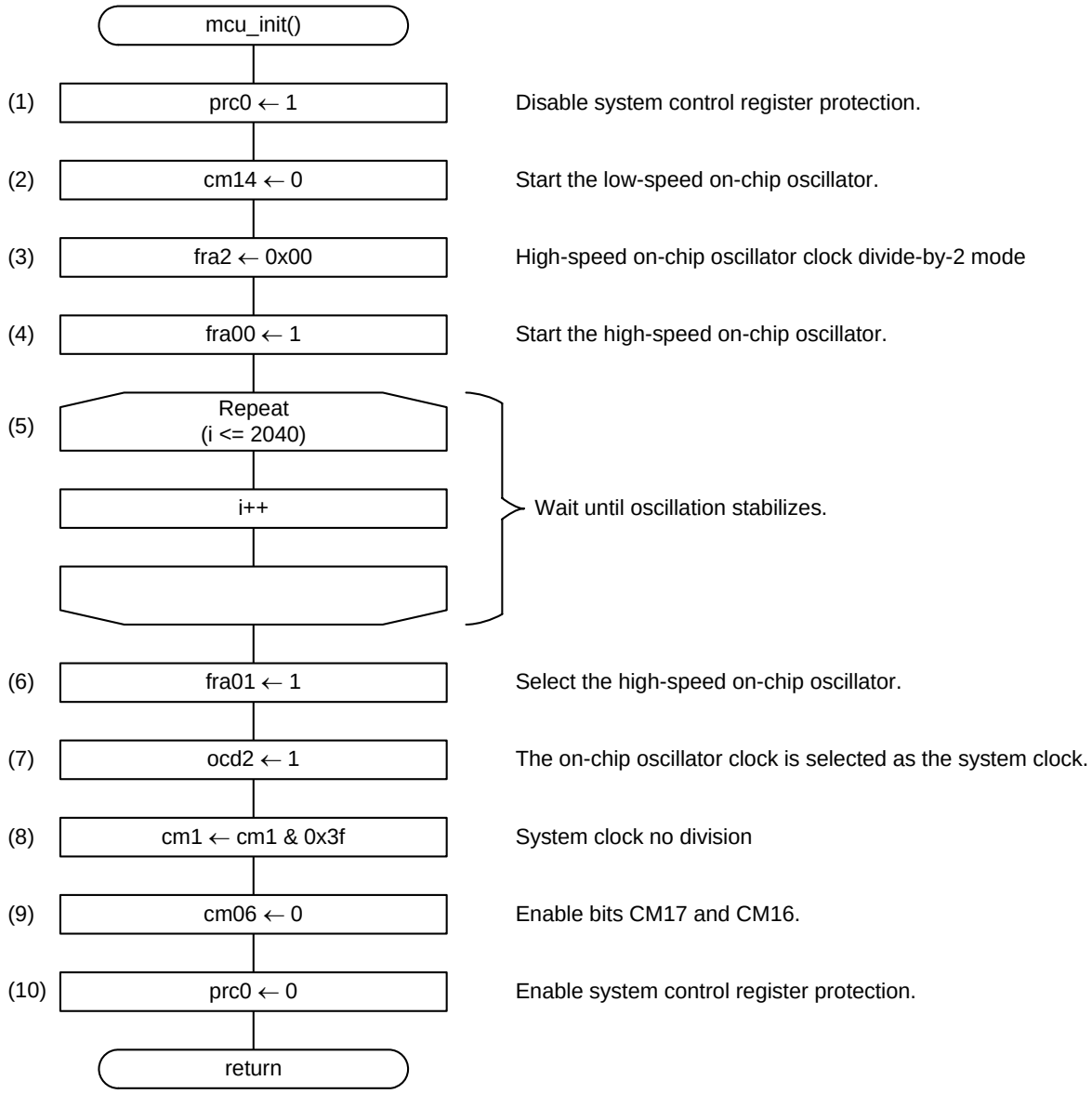
Disable the interrupt.

System clock setting (high-speed on-chip oscillator setting)

Timer RG associated SFR setting
(timer mode (output compare function) setting)

4.3 System Clock Setting

- Flowchart



• Register setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	×	×	×	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value			—	0	×	×	×	×

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	×	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	×	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	×	1	×	×

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

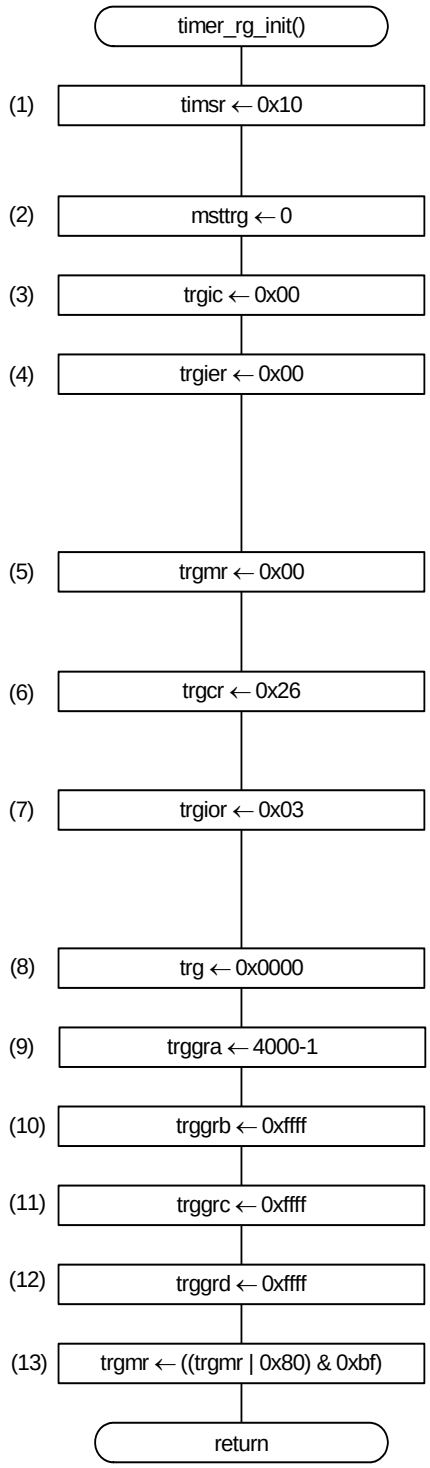
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write Disabled	R/W

4.4 Timer RG Associated SFR Setting

- Flowchart



The TRGIOA pin is assigned to P5_6.
Do not use the TRGIOB pin.

Set timer RG to active.

Disable the timer RG interrupt.

Disable the IMFA bit initiated interrupt.
Disable the IMFB bit initiated interrupt.
Disable the UDF bit initiated interrupt.
Disable the OVF bit initiated interrupt.

Select the timer mode.
Select increment.
Stop the timer RG count.

Count source: fOCO40M
TRG register clear source: TRG register cleared by compare match with TRGGRA register

TRGGRA control: Toggle output by compare match of TRGGRA register
TRGGRA mode: Output compare function
TRGGRC register function: General register

Initialize the TRG register.

Set the count period to 100 μs (25 ns x 4000 = 100 μs).

Initialize the TRGGRB register.

Initialize the TRGGRC register.

Initialize the TRGGRD register.

Start the timer RG count.

• Register Setting

(1) Set the timer pin select register.

Timer Pin Select Register (TIMSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	×	×	0	1	—	×	—	×

Bit	Symbol	Bit Name	Function	R/W
b4	TRGIOASEL	TRGIOA pin select bit	1: P5_6 assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used	R/W

(2) Set timer RG to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	MSTTRG	Timer RG standby bit	0: Active	R/W

(3) Disable the timer RG interrupt.

Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Disable all the interrupt sources for timer RG.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA flag disabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB flag disabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF flag disabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF flag disabled	R/W

(5) Set the TRGMR register.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	×	×	×	×	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	0: Timer Mode	R/W
b1	MDF	Phase counting mode select bit	0: Increment	
b7	TSTART	TRG count start bit	0: Count stops	R/W

(6) Set the count source to fOCO40M and the TRG register clear source to the compare match of the TRGGRA register.

Timer RG Control Register (TRGCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	1	×	×	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 1 1 0: fOCO40M	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 1: TRG register cleared by input capture or compare match with TRGGRA register	R/W
b6	CCLR1			R/W

(7) Set the TRGIOR register.

Timer RG I/O Control Register (TRGIOR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	×	×	×	×	0	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 1 1: Toggle output by compare match with TRGGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit	0: Output compare function	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register	R/W

(8) Initialize the TRG counter to 0000h.

Timer RG Counter (TRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count operation is increment.	0000h to FFFFh	R/W

(9) Set 4000-1 (0F9Fh) which is the compare value with the TRG counter to the TRGGRA register.

Timer RG General Register A (TRGGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	1	1	1

Bit	Function	R/W
b15 to b0	Compare value with TRG register.	R/W

(10) Initialize the TRGGRB register to FFFFh.

Timer RG General Register B (TRGGRB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in the timer RG general register A (TRGGRA).	R/W

(11) Initialize the TRGGRC register to FFFFh.

Timer RG General Register C (TRGGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in the timer RG general register A (TRGGRA).	R/W

(12) Initialize the TRGGRD register to FFFFh.

Timer RG General Register D (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	The value larger than setting value in the timer RG general register A (TRGGRA).	R/W

(13) Start the TRG counter.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	×	×	×	×	×	

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRG count start bit	1: Count starts	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Family page.

6. Reference Documents

Hardware Manual
R8C/38C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

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REVISION HISTORY	R8C/38C Group Timer RG Timer Mode (Output Compare Function)

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		Page	Summary
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