R8C/25 Group

Timer RA in Timer Mode

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1. Abstract

This document describes how to set up and use the timer RA in timer mode on the R8C/25 Group device.

2. Introduction

The application example described in this document is applied to the following:

• MCU: R8C/25 Group

This program can be used with other R8C/Tiny Series which have the same SFR (special function register) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Note on oscillation stabilization wait time
In chapter 4.2.1 , select the high-speed on-chip oscillator after starting the high-speed on-chip oscillator and waiting until oscillation stabilizes.

3. Applications

3.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA.
Figure 3.1 shows a Block Diagram of Timer RA.

Time RA has the following five modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses of which polarity inverted by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

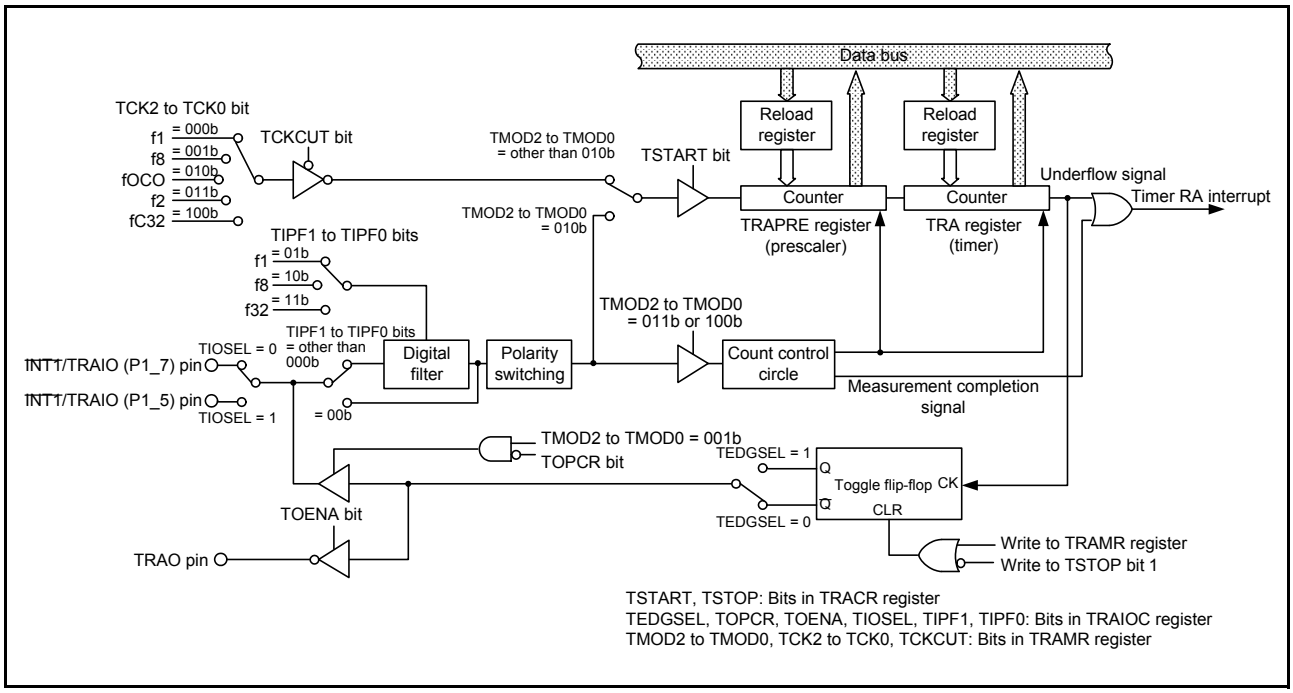


Figure 3.1 Block Diagram of Timer RA

3.2 Timer Mode

In this mode, the timer counts an internally generated count source (refer to Table 3.1).
Figure 3.2 shows Registers TRACR and TRAIOC in Timer Mode, and Figure 3.3 shows Registers TRAMR, TRAPRE, and TRA in Timer Mode.

Table 3.1 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Programmable I/O port, or $\overline{\text{INT1}}$ interrupt input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **3.3 Timer Write Control during Count Operation**).

Timer RA Control Register(4)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRACR	0100h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RA count start bit(1)	0: Count stops 1: Count starts	RW
TCSTF	Timer RA count status flag(1)	0: Count stops 1: During count	RO
TSTOP	Timer RA count forcible stop bit(2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TEDGF	Active edge judgment flag(3, 5)	0 : Active edge not received 1 : Active edge received	RW
TUNDF	Timer RA underflow flag(3, 5)	0 : No underflow 1 : Underflow	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **3.4 Notes on Timer RA**.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TPRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.
5. Set to 0 in timer mode, pulse output mode, and event counter mode.

Timer RA I/O Control Register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0

Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0 TIPF1	TRAIO input filter select bits	Set to 0 in timer mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 3.2 Registers TRACR and TRAIOC in Timer Mode

Timer RA Mode Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
				X	0	0	0

Symbol	Address	After Reset
TRAMR	0102h	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RA operating mode select bits	b2 b1 b0 0 0 0 : Timer mode	RW
TMOD1			RW
TMOD2			RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCK0	Timer RA count source select bits	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: fC32 1 0 1: 1 1 0: 1 1 1: } Do not set.	RW
TCK1			RW
TCK2			RW
TCKCUT	Timer RA count source cutoff bit	0: Provides a count source 1: Cuts off a count source	RW

NOTES:
1. When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

Timer RA Prescaler Register

b7	b0

Symbol	Address	After Reset
TRAPRE	0103h	FFh(1)

Function	Setting Range	RW
Counts an internal count source	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

Timer RA Register

b7	b0

Symbol	Address	After Reset
TRA	0104h	FFh(1)

Function	Setting Range	RW
Counts on underflow of timer RA prescaler register	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.

Figure 3.3 Registers TRAMR, TRAPRE, and TRA in Timer Mode

3.3 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 14.5 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

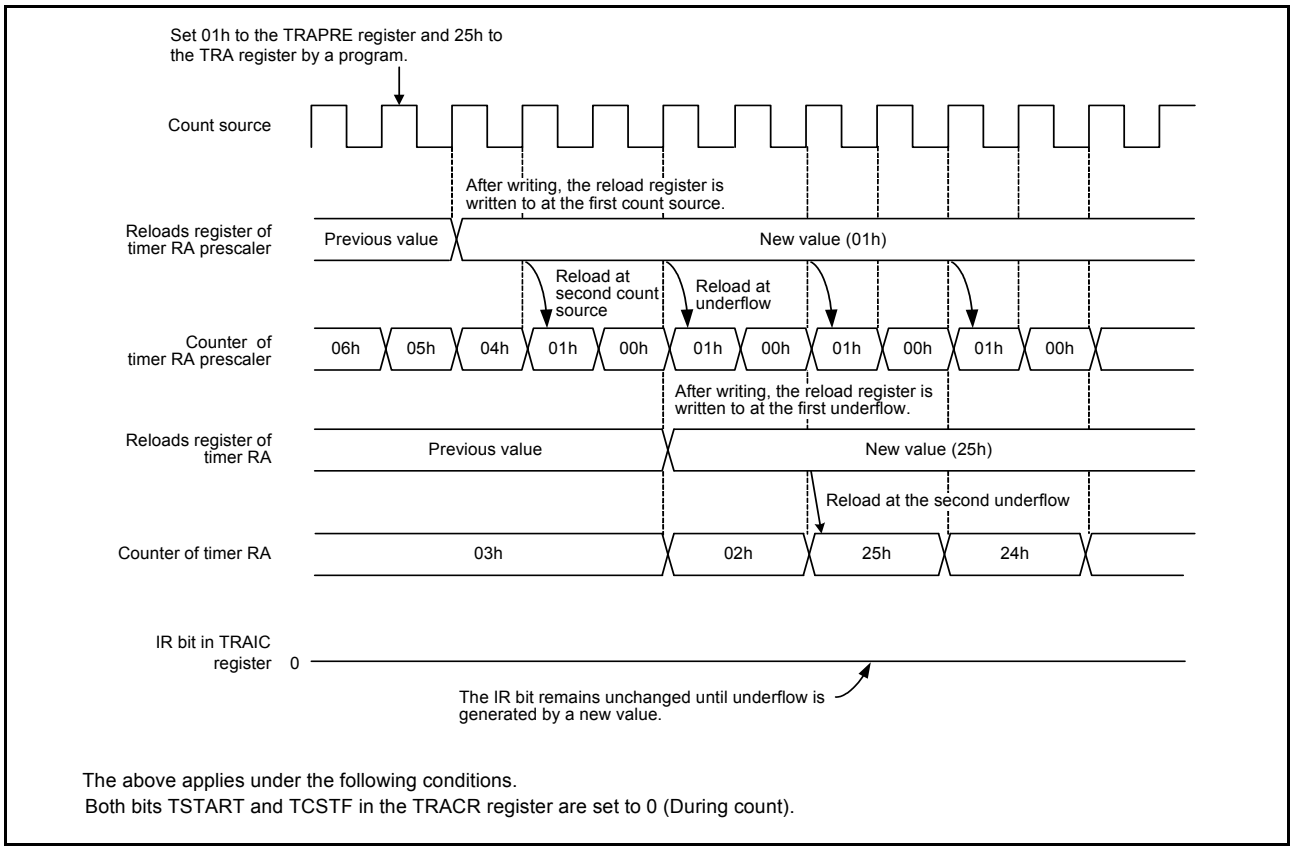


Figure 3.4 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

3.4 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
- During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
- The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress.
- During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.
- Timer RA counting is stopped when the TCSTF bit is set to 0.

NOTE:
1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

4. Program Overview

This program can be used on timer RA to underflow at 1 ms.

1 ms= fOCO(1) × (TRAPRE register setting value + 1) × (TRA register setting value + 1)
= 25 ns (40MHz) × 4 (FRA2 = 0x02: divide-by-4 mode) × (99 +1) × (99 +1)

NOTE:
1. fOCO is an operating clock generated by the high-speed on-chip oscillator. It is applied with at the divide ratio set by the high-speed on-chip oscillator control register (FRA2).

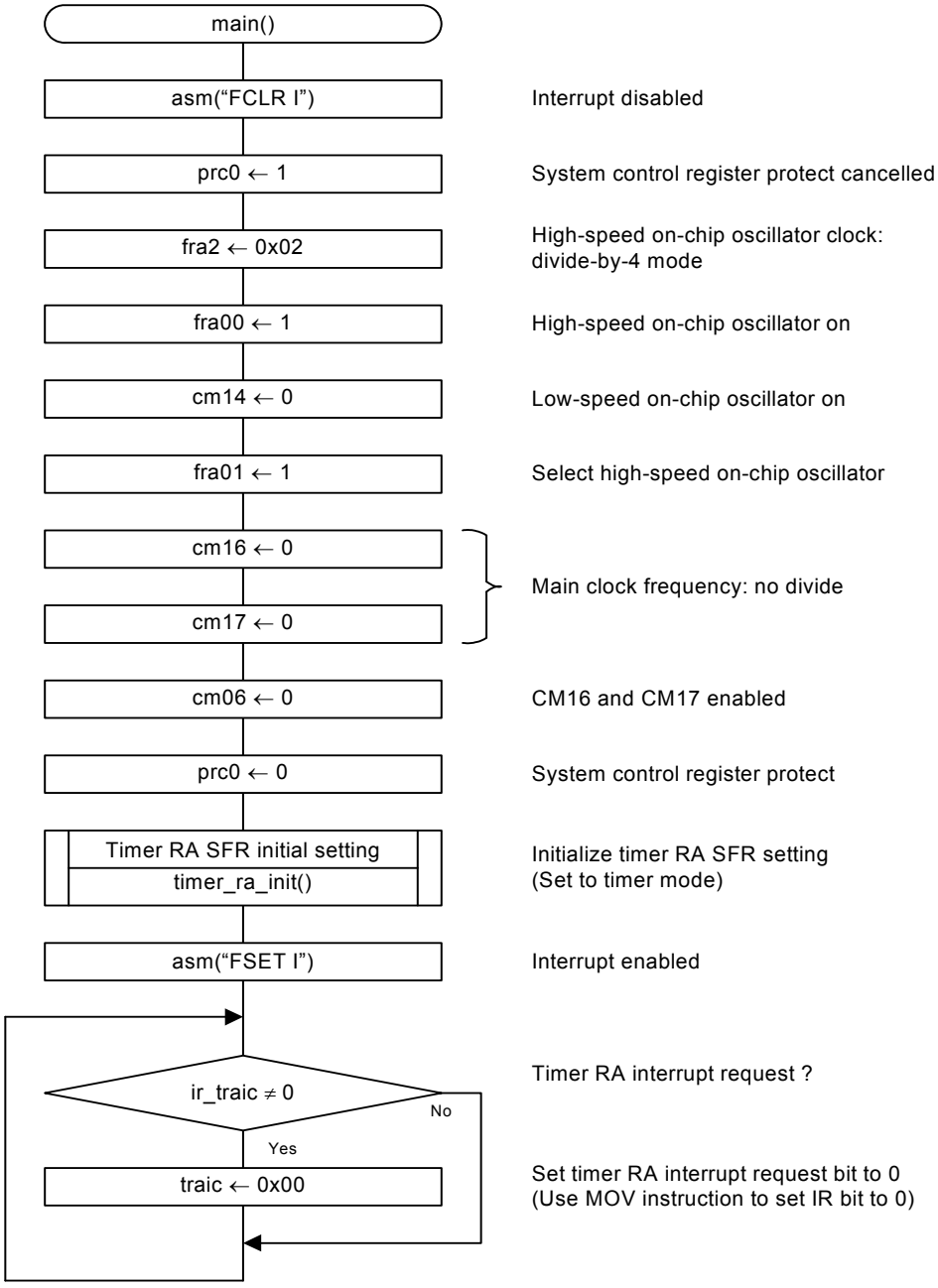
4.1 Function Table

Table 4.1

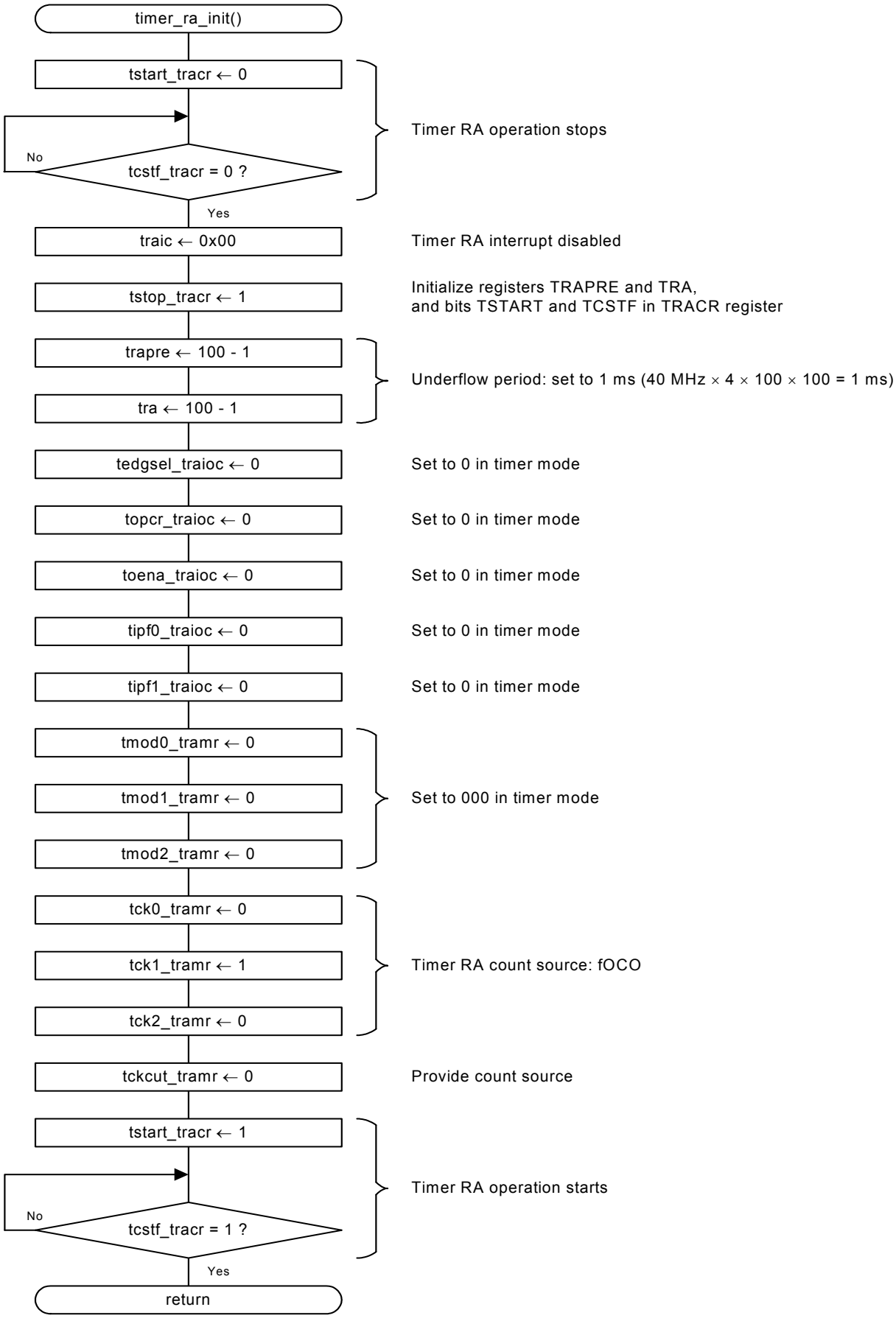
Declaration	void timer_ra_init(void)		
Overview	SFR initial setting associated with timer RA		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Usage
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with time RA		

4.2 Flow Chart

4.2.1 Main functions



4.2.2 Timer RA SFR Initial Setting



5. Reference Document

User's Manual: Hardware
R8C/25 Group Hardware Manual
(Download the latest version from the Renesas Electronics website.)

Technical News/Technical Update
(Download the latest information from the Renesas Electronics website.)

6. Sample Programming Code

Download a sample program on the Renesas Electronics website.

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REVISION HISTORY	R8C/25 Group Timer RA in Timer Mode

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		Page	Summary
1.00	Sep 15, 2006	–	First Edition issued
1.10	June 1, 2012	1	Note on oscillation stabilization wait time added
		–	Previous document number: REJ05B0827

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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