R32C/100 Series

Pulse-Width Measurement Using the Digital Debounce Function of Intelligent I/O

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Abstract

This document describes a method for measuring a pulse width using the digital debounce function of the intelligent I/O.

Products

MCUs: R32C/120 Group, R32C/121 Group, R32C/151 Group, R32C/152 Group, R32C/153 Group, R32C/156 Group, R32C/157 Group, R32C/160 Group, R32C/161 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

The digital debounce function enables to determine the signal level when the pulse becomes longer than the filter width set by a program after the signal is input on a rising or falling edge.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows Digital Debounce Filtering.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Intelligent I/O group 0 (IIO0)	Pulse-width measurement using the digital debounce function

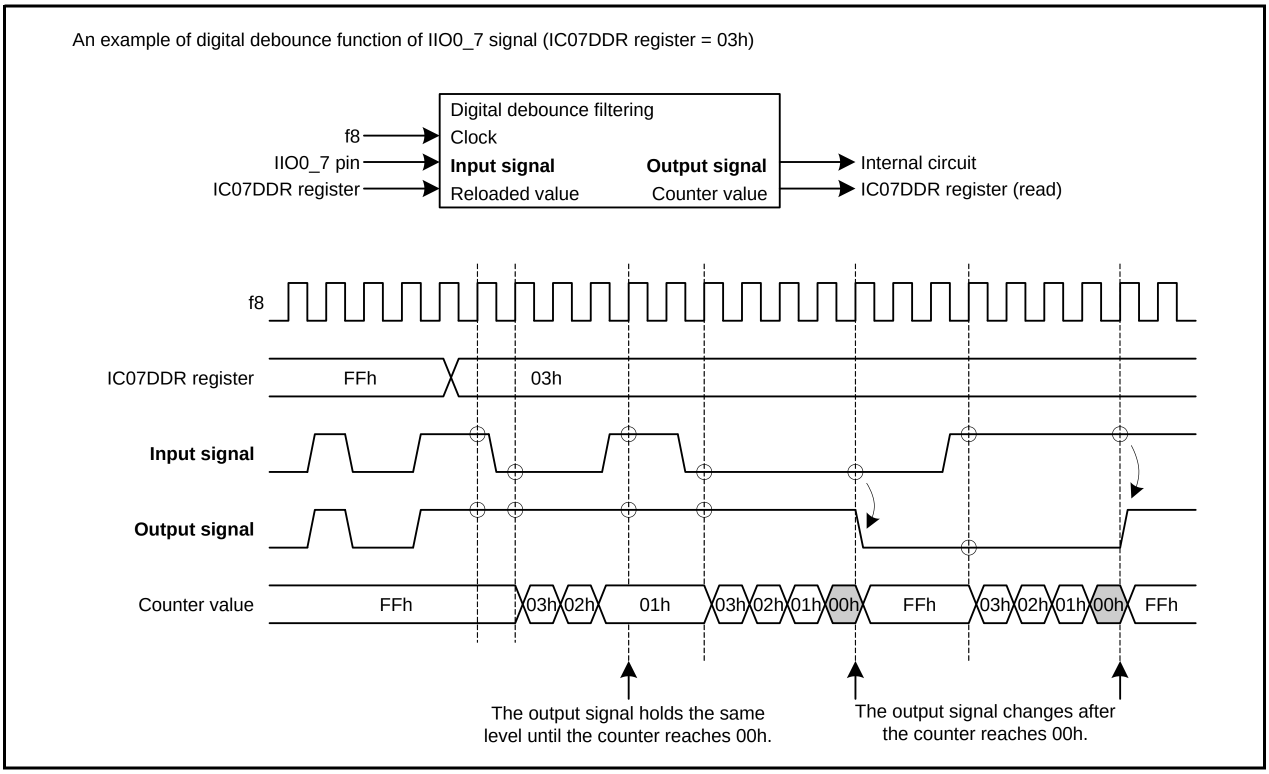


Figure 1.1 Digital Debounce Filtering

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64219JFB (R32C/121 Group)
Operating frequencies	Main clock: 8 MHz PLL clock: 128 MHz Base clock: 64 MHz CPU clock: 64 MHz Peripheral bus clock: 32 MHz Peripheral function clock source: 32 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Reference Application Notes

The application notes associated with this application note are listed below. Refer to the following application notes for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)
- R32C/100 Series How to Use Intelligent I/O Interrupt (REJ05B1416-0100)
- R32C/100 Series Intelligent I/O Single-phase Waveform Output Mode (REJ05B1226-0100)

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P1_7/IIO0_7	Input	Pulse-width measurement using the digital debounce function

5. Software

5.1 Operation Overview

Input the signal pulse to the IIO0_7 pin and measure the pulse width.

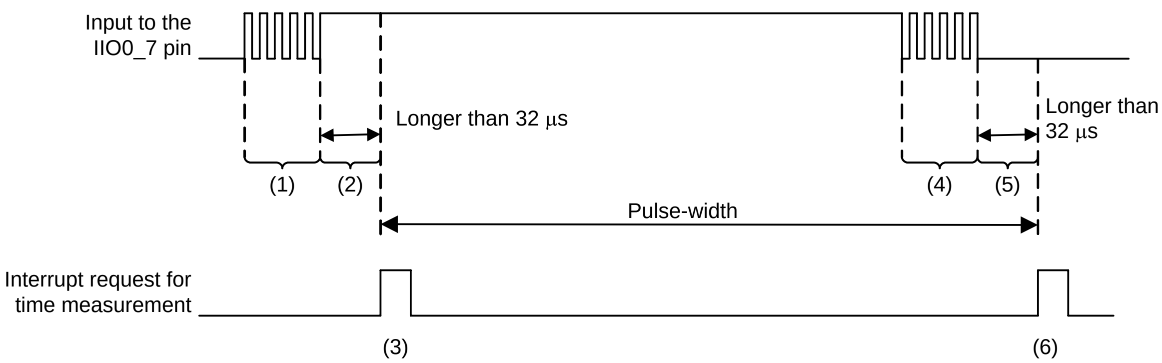
(1) Intelligent I/O settings

Use group 0 channel 7 in time measurement mode. Set both edges as a time measurement trigger. Set the filter width of the digital debounce function to 32 µs (IC07DDR register = 7Fh).

(2) Pulse-width measurement

The time measurement interrupt of channel 7 is used, and the G0TM7 register is read during the time measurement interrupt handling. The difference from the value previously read is the pulse width.

Figure 5.1 shows operation using the sample code.



(1) An external time measurement trigger input cannot be accepted if the pulse width signal is less than 32 µs.
(2) When the signal level at a rising edge becomes longer than the filter width, an external time measurement trigger input can be accepted, and the base timer value is stored in the G0TM7 register.
(3) When time measurement starts, interrupt requests for time measurement are generated. The G0TM7 register is read during the time measurement interrupt handling.
(4) An external time measurement trigger input cannot be accepted if the pulse width signal is less than 32 µs.
(5) When the signal level at a falling edge becomes longer than the filter width, an external time measurement trigger input can be accepted, and the base timer value is stored in the G0TM7 register.
(6) When time measurement starts, interrupt requests for time measurement are generated. The G0TM7 register is read during the time measurement interrupt handling. The difference from the value previously read from (3) is the pulse width.

Figure 5.1 Sample Code Operation

5.2 Notes

In the sample code, the BT0R bit in intelligent I/O interrupt request register 7 becomes 1 (interrupt requested) when the base timer overflows. When the BT0E bit in intelligent I/O interrupt request register 7 is 0 (disabled), the BT0R bit does not need to be set to 0 (no interrupt requested).

5.3 Variable Tables

Table 5.1 lists the Global Variables.

Table 5.1 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	tr_flg	First decision flag of time measurement	main, _intelligent_io_int7
uint16_t	tr_now	Time measurement value (new)	main, _intelligent_io_int7
uint16_t	tr_old	Time measurement value (old)	main, _intelligent_io_int7
uint16_t	tr_pulse	Pulse-width measurement	main, _intelligent_io_int7

5.4 Function Table

Table 5.2 lists the Functions.

Table 5.2 Functions

Function Name	Outline
iio_init	Intelligent I/O initialization
_intelligent_io_int7	Intelligent I/O interrupt 7 handling

5.5 Function Specifications

The following tables list the sample code function specifications.

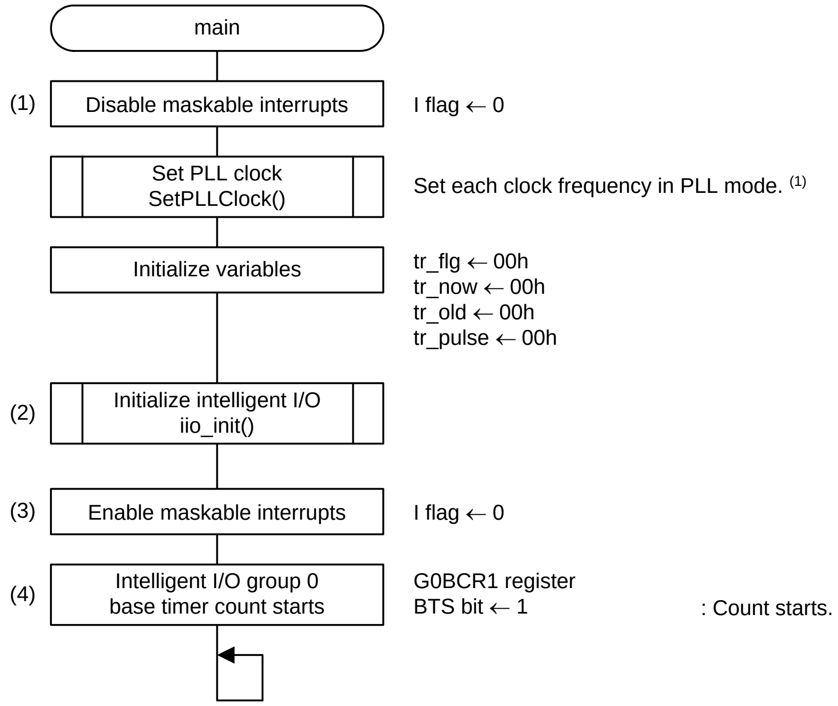
iio_init	
Outline	Intelligent I/O initialization
Header	None
Declaration	void iio_init(void)
Explanation	Initializes the intelligent I/O.
Argument	None
Returned value	None
Remark	

_intelligent_io_int7	
Outline	Intelligent I/O interrupt 7 handling
Header	None
Declaration	void _intelligent_io_int7(void)
Explanation	Enable the intelligent I/O interrupt for channel 7
Argument	None
Returned value	None
Remark	Measure a pulse width using the digital debounce function.

5.6 Flowcharts

5.6.1 Main Processing

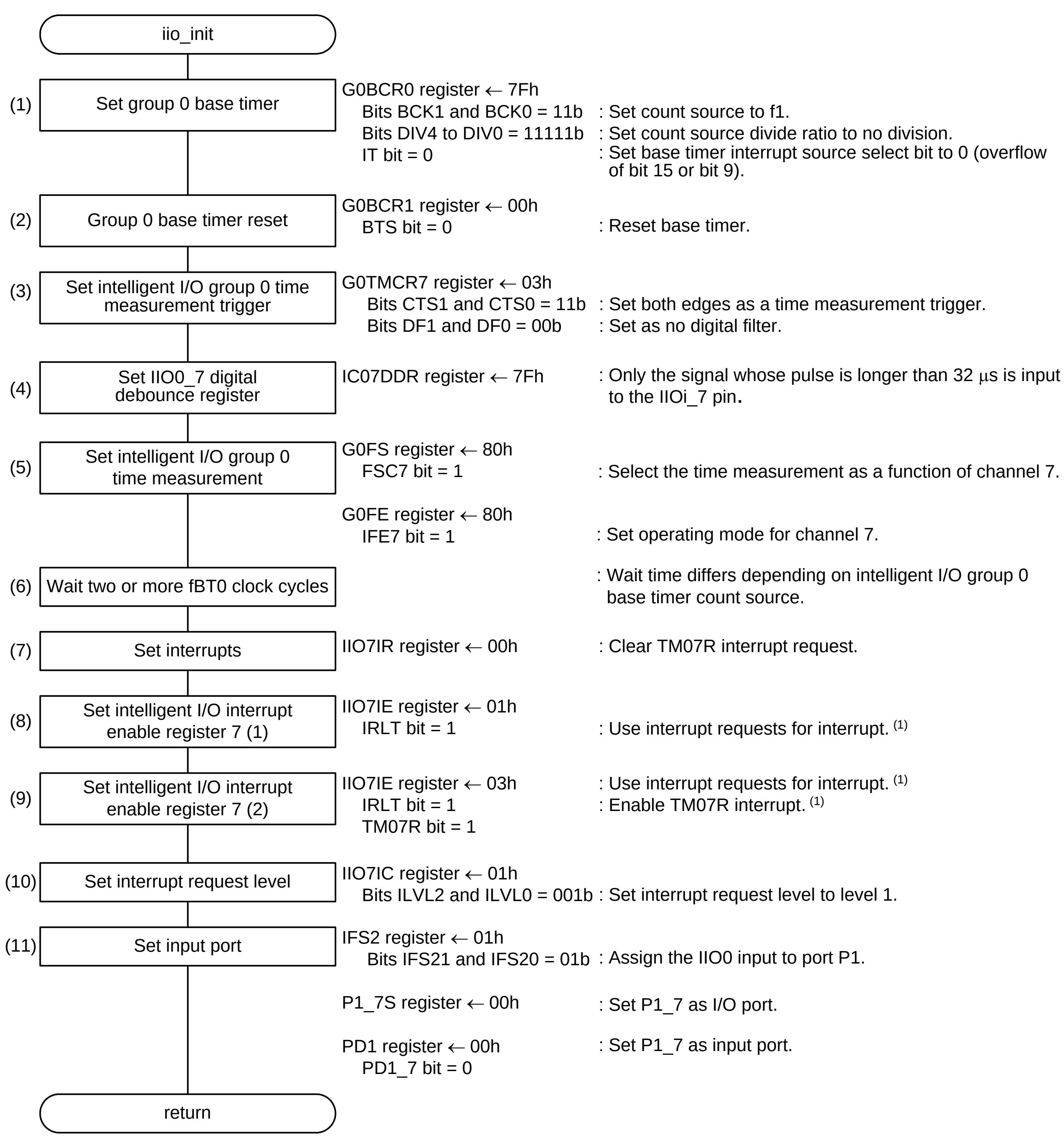
Figure 5.2 shows the Main Processing.



Note:
1. Refer to the hardware user's manual for initializing the clock.

Figure 5.2 Main Processing

Figure 5.2 shows Intelligent I/O Initialization.



Note:
1. To use interrupt requests for interrupt, the IRLT bit should be set to 1, then bit 1 should be set to 1.

Figure 5.3 Intelligent I/O Initialization

5.6.2 Intelligent I/O Interrupt 7 Handling

Figure 5.4 shows Intelligent I/O Interrupt 7 Handling.

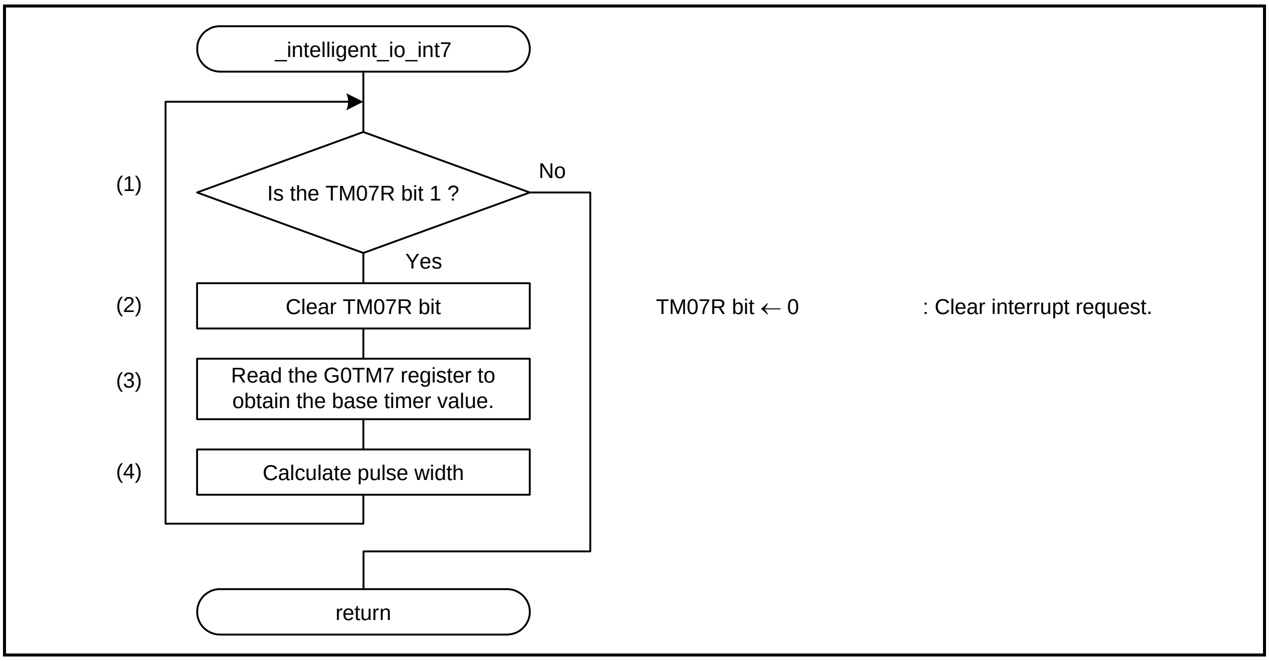


Figure 5.4 Intelligent I/O Interrupt 7 Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/120 Group User's Manual: Hardware Rev.1.10
R32C/121 Group User's Manual: Hardware Rev.1.10
R32C/151 Group User's Manual: Hardware Rev.1.10
R32C/152 Group User's Manual: Hardware Rev.1.10
R32C/153 Group User's Manual: Hardware Rev.1.10
R32C/156 Group User's Manual: Hardware Rev.1.03
R32C/157 Group User's Manual: Hardware Rev.1.03
R32C/160 Group User's Manual: Hardware Rev.1.02
R32C/161 Group User's Manual: Hardware Rev.1.02
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R32C/100 Series Pulse-Width Measurement Using the Digital Debounce Function of Intelligent I/O

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 15, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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