R32C/100 Series

How to Use the Watchdog Timer Automatic Count Start

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Abstract

This document describes how to use the watchdog timer automatic count start in the R32C/100 Series.

Products

R32C/120 Group
R32C/121 Group
R32C/145 Group
R32C/151 Group
R32C/152 Group
R32C/153 Group
R32C/156 Group
R32C/157 Group
R32C/160 Group
R32C/161 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This chapter explains how to reset the MCU using the watchdog timer.
Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Usage Example of the Watchdog Timer.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Watchdog timer	Reset source
Timer A (timer A0)	Write timing to the WDTS register

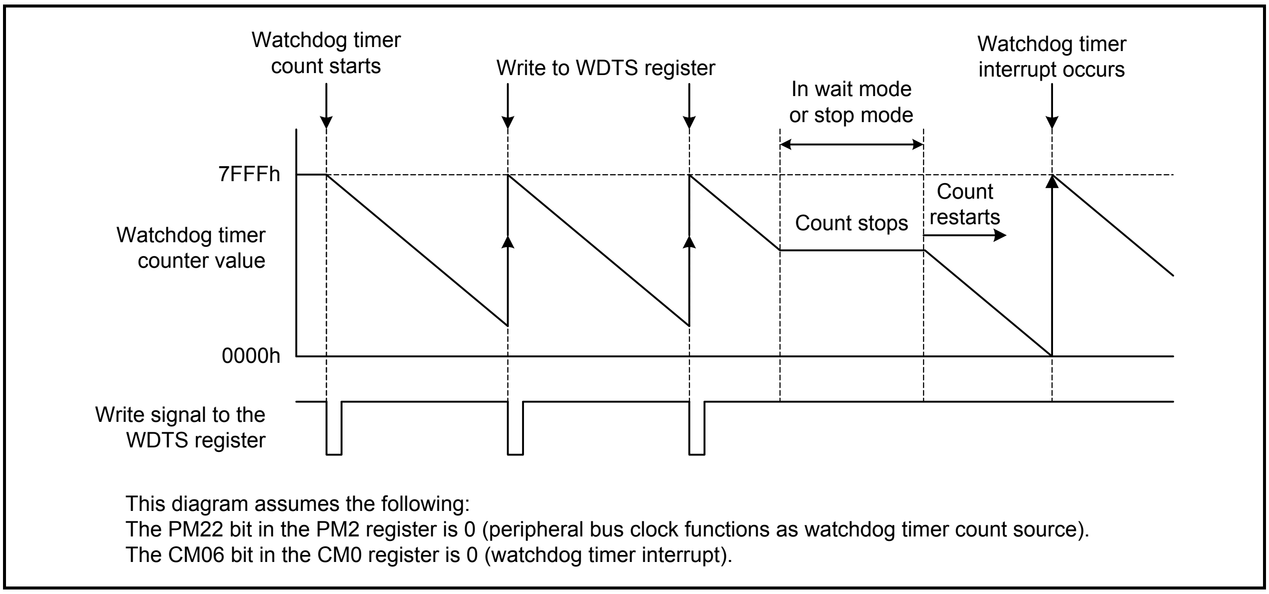

Figure 1.1 Usage Example of the Watchdog Timer

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64219JFB (R32C/121 Group)
Operating frequencies	• Main clock: 8 MHz • PLL clock: 128 MHz • Base clock: 64 MHz • CPU clock: 64 MHz • Peripheral bus clock: 32 MHz • Peripheral function clock source: 32 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir “$(CONFIGDIR)” Default setting is used in the integrated development environment.
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Reference Application Note

The application note listed below is associated with this application note. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Peripheral Functions

This chapter provides supplementary information on the watchdog timer. Refer to the User's Manual (hardware) for general information.

4.1 Watchdog Timer

The watchdog timer monitors program executions and detects defective programs. The 15-bit watchdog counter counts downward with the cycle which is the peripheral bus clock frequency or on-chip oscillator clock frequency divided by the prescaler.
The watchdog timer has two prescalers. One is the on-chip oscillator clock divided by 1, 2, 4, or 8; the other is the peripheral bus clock divided by 16 or 128.
Figure 4.1 shows the Watchdog Timer Block Diagram.

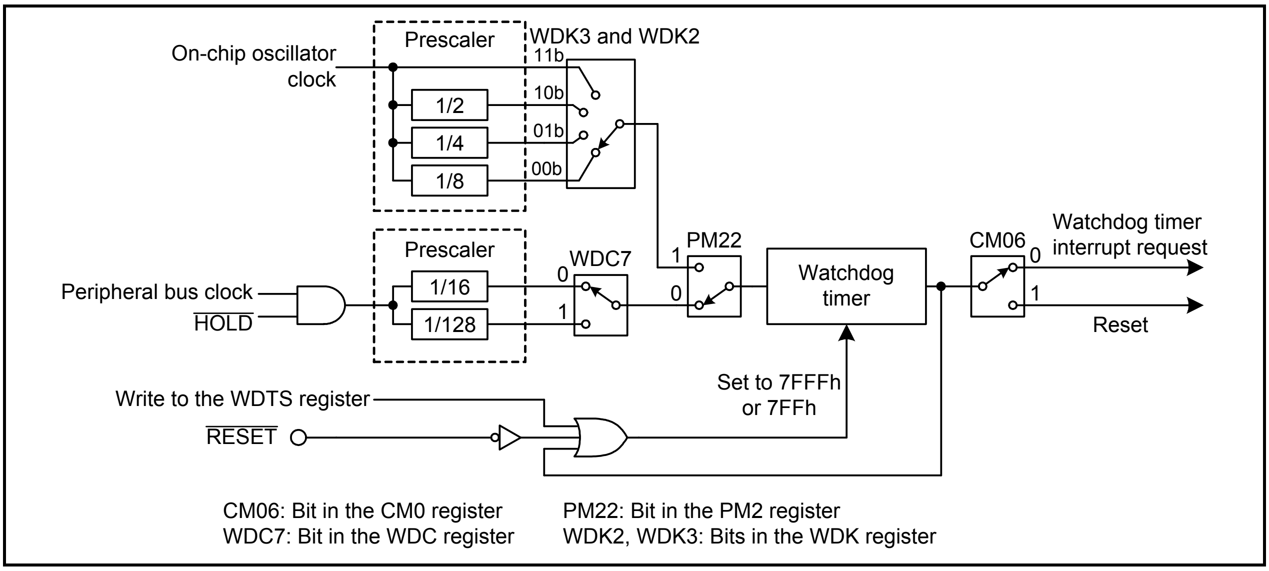

Figure 4.1 Watchdog Timer Block Diagram

The general formula to calculate a watchdog timer period is:

$$\text{Watchdog timer period} = \frac{\text{Prescaler divider factor (16 or 128)} \times 32768}{\text{Peripheral bus clock frequency}}$$

or

$$\text{Watchdog timer period} = \frac{\text{Prescaler divider factor (1, 2, 4, or 8)} \times 2048}{\text{On-chip oscillator clock frequency}}$$

Depending on the timing of when a value is written to the WDTS register, a marginal error of one prescaler output cycle (maximum) may occur in the watchdog timer period.
Table 4.1 lists examples of watchdog timer periods.

Table 4.1 Examples of Watchdog Timer Periods When the Peripheral Bus Clock is 32 MHz and the On-Chip Oscillator is Approximately 125 kHz

Count Source	Period
Peripheral bus clock divided by 16	Approximately 16.4 ms
Peripheral bus clock divided by 128	Approximately 131.1 ms
On-chip oscillator clock with no division	Approximately 16.4 ms
On-chip oscillator clock divided by 2	Approximately 32.8 ms
On-chip oscillator clock divided by 4	Approximately 65.5 ms
On-chip oscillator clock divided by 8	Approximately 131.1 ms

4.2 Setting the Optional Function Select Area

This section describes an example of creating a new project work space after selecting *C source startup Application* in the High-performance Embedded Workshop. The fixed vector table is defined in fvector.c. Figure 4.2 shows the Initial Settings of the Fixed Vector Table.

```
////////////////////////////////////////////////////////////////////////

#pragma interrupt/v _dummy_int      //udi
#pragma interrupt/v _dummy_int      //over_flow
#pragma interrupt/v _dummy_int      //brki
#pragma interrupt/v  0xffffffff
#pragma interrupt/v  0xffffffff
#pragma interrupt/v _dummy_int      //wdt (1)
#pragma interrupt/v _dummy_int
#pragma interrupt/v _dummy_int      //nmi
#pragma interrupt/v start

#pragma interrupt _dummy_int()
void _dummy_int(void);
void _dummy_int(void){}


// Set ID Code Protection
//   _asm("   .id            ""\"#FFFFFFFFFFFFFF\"");

// Set Optional Function Select Area
//_asm("   .ofsa 0FFH"); (2)

Notes:
    1. Set this vector when using the watchdog timer interrupt.
    2. Set this OFS area as shown in Figure 4.3 when using the watchdog timer automatic count start.
```

Figure 4.2 Initial Settings of the Fixed Vector Table

This area cannot be set by a program. Use a flash programmer when rewriting.
Figure 4.3 shows an example of Setting the Optional Function Select Area.

```
_asm("   .ofsa 072H");   /* WDTON = 0                    : Starts counting automatically */
                         /* WPSC1 and WPSC0 = 00b : Divide-by-8 (WDK3 and WDK2 = 00b) */
                         /* CSPM = 0                     : Enabled (PM22 = 1) */
```

Figure 4.3 Setting the Optional Function Select Area

5. Hardware

5.1 Pins Used

Table 5.1 lists the Pins Used and Their Functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
P10_0 to P10_6	Output	Output level changes every 100 ms

6. Software

Write a value to the WDTS every 1 ms period and increment the output value of port P10 every 100 ms period. When the output value reaches 40h, incrementing stops and values are not written to the WDTS register. When the watchdog timer underflows, the MCU initializes the CPU, SFRs, and pins. Then the program is executed from the address listed in the reset vector. The settings are shown below.

Settings

- Set the watchdog timer to automatic count start.
- Set the watchdog timer on-chip oscillator prescaler to divided by 8.
- After a reset, set to count source protect mode (the on-chip oscillator clock is the watchdog timer count source).
- Do not use the watchdog timer interrupt.

6.1 Operation Overview

The sample program performs the following operations:

(1) Program write
When writing a program to an on-chip flash area, set the OFS area to 72h.

(2) MCU reset
As the WDTON bit in the OFS area is set to 0 (start counting automatically), after the MCU is reset, the watchdog timer automatically starts.

(3) Initial setting
Initial settings are made for the watchdog timer, port P10, and timer A0.

(4) Timer A0 interrupt
(4)-1 When the timer A0 interrupt occurs, a value is written to the WDTS register and the watchdog timer is initialized in the timer A0 interrupt processing.The port P10 output value increments every 100 ms.
(4)-2 When the port P10 value is 40h, the WDTS is not written to, and the watchdog timer is not initialized.

(5) Watchdog timer reset
When the watchdog timer underflows, the MCU initializes the CPU, SFRs, and pins. Then the program is executed from the address listed in the reset vector.

Figure 6.1 shows an Operation Example of the Sample Code.

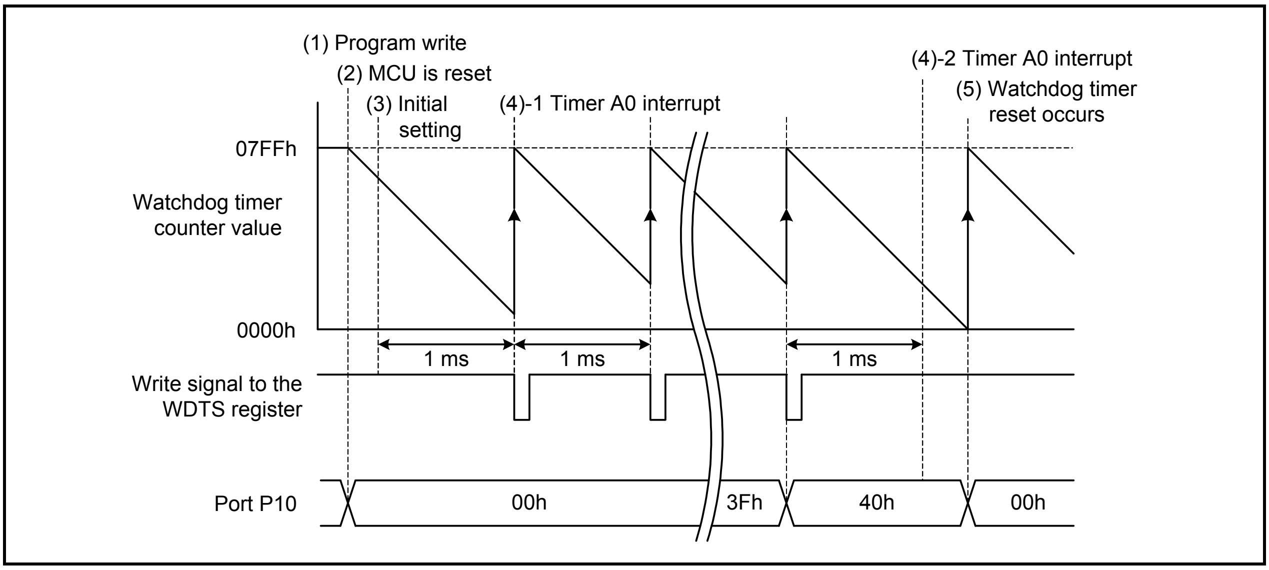

Figure 6.1 Operation Example of the Sample Code

6.2 Constants

Table 6.1 lists the Constants Used in the Sample Code.

Table 6.1 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
D_MAX_P10_CNT	40h	When port P10 becomes 40h, the WDTS register becomes write disabled.
D_MAX_TA0_WAIT	100	This is used for changing the output level of port P10 in 100 ms intervals.

6.3 Variable

Table 6.2 lists the Global Variable.

Table 6.2 Global Variable

Type	Variable Name	Contents	Function Used
uint16_t	cnt_ta0	This counter is used for changing the output level of port P10 in 100 ms intervals.	main, _timer_A0

6.4 Functions

Table 6.3 lists the Functions.

Table 6.3 Functions

Function Name	Outline
timerA0_init	Timer A0 initial setting
_timer_a0	Timer A0 interrupt handling

6.5 Function Specifications

The following tables list the sample code function specifications.

timerA_init	
Outline	Timer A0 initial setting
Header	None
Declaration	void timerA0_init(void)
Description	Set a 1 ms period timer.
Argument	None
Returned value	None
Remarks	

_timer_a0	
Outline	Timer A0 interrupt handling
Header	None
Declaration	void _timer_a0(void)
Description	Write a value to the WDTS every 1 ms period. Increment the output value of port P10 every 100 ms period. When the output value becomes 40h, stop incrementing and do not write values to the WDTS register.
Argument	None
Returned value	None
Remarks	

6.6 Flowcharts

6.6.1 Main Processing

Figure 6.2 shows the Main Processing.

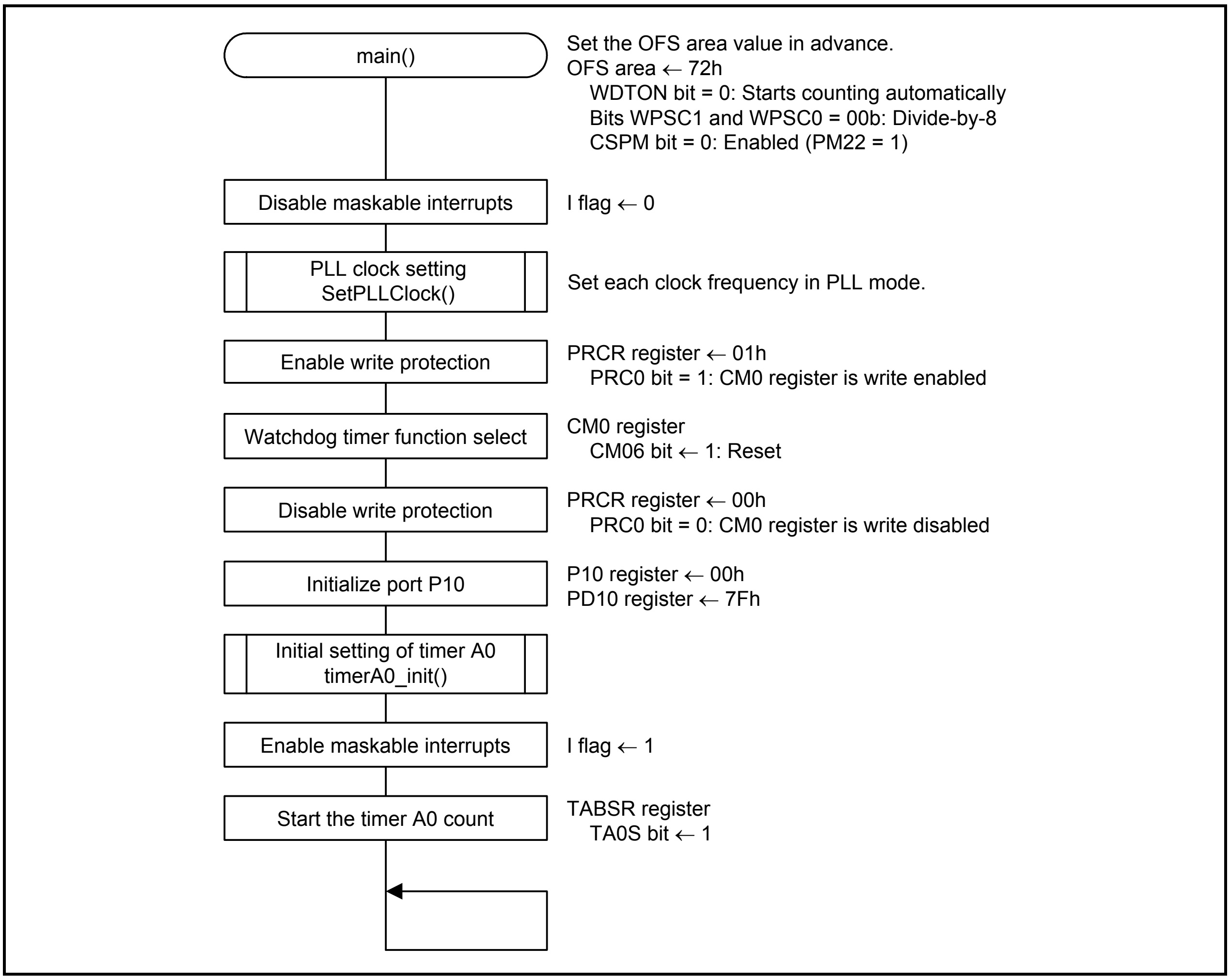

Figure 6.2 Main Processing

6.6.2 Timer A0 Initial Setting

Figure 6.3 shows the Timer A0 Initial Setting.

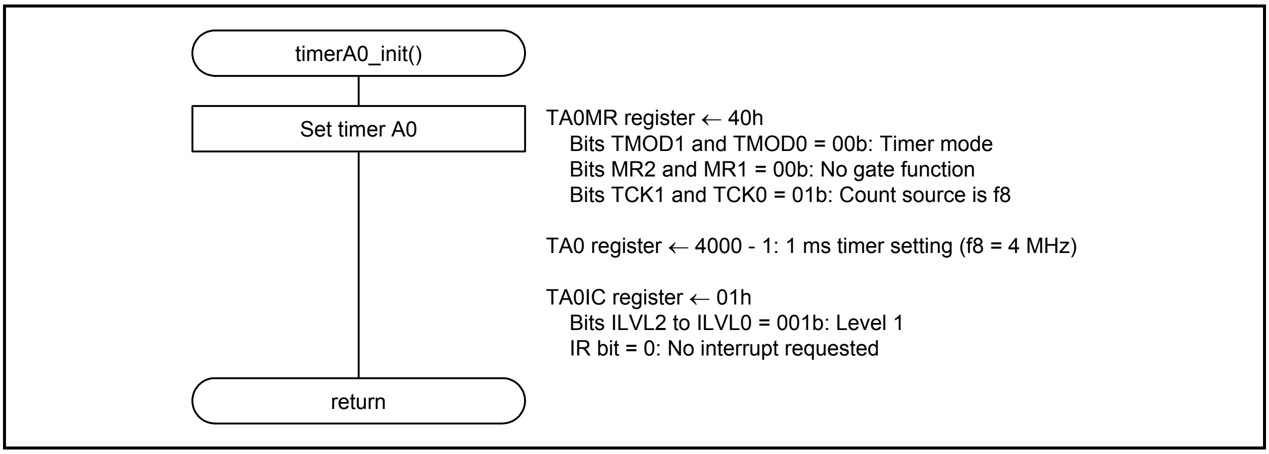

Figure 6.3 Timer A0 Initial Setting

6.6.3 Timer A0 Interrupt Handling

Figure 6.4 shows the Timer A0 Interrupt Handling.

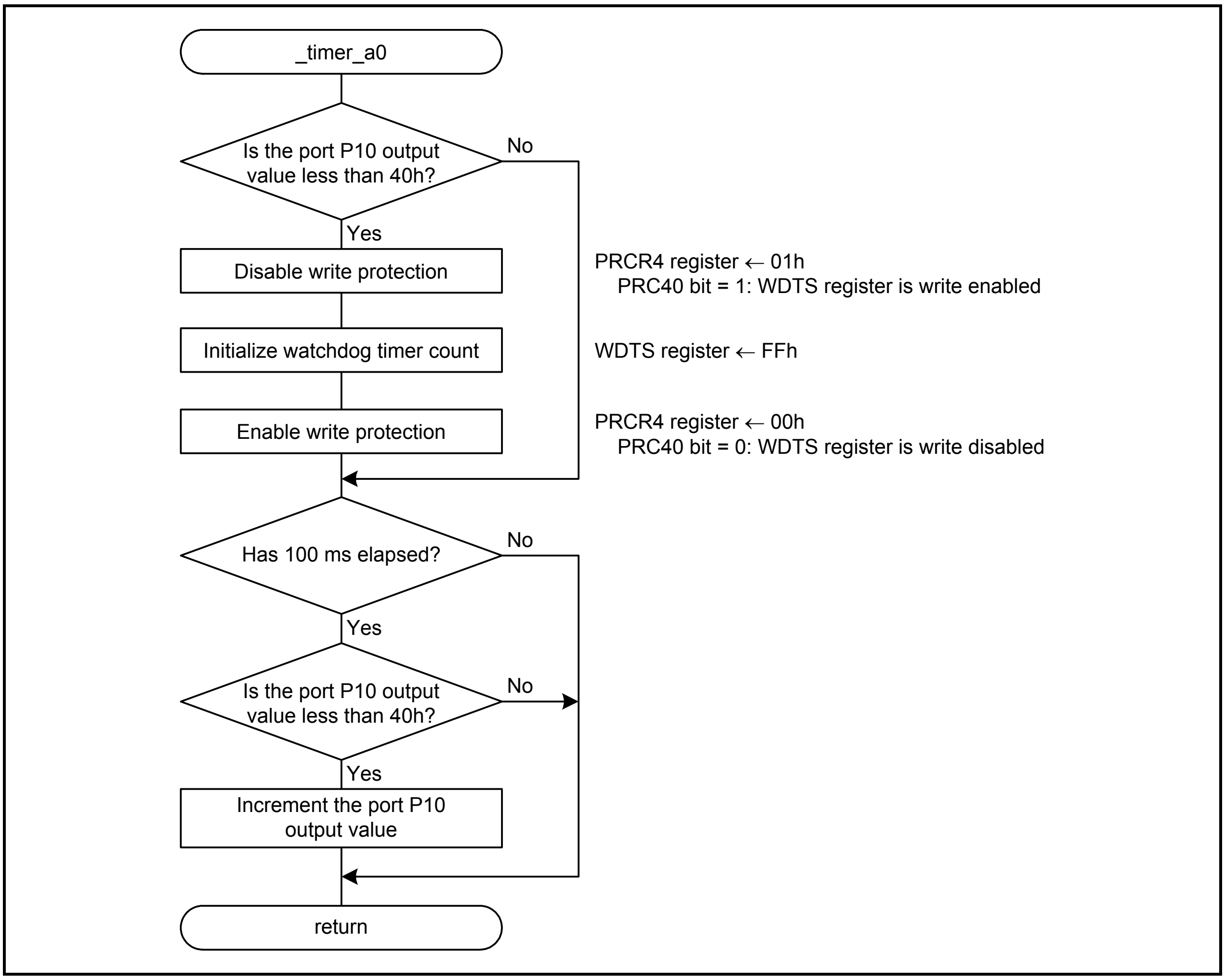

Figure 6.4 Timer A0 Interrupt Handling

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

R32C/120 Group User's Manual: Hardware Rev.1.10
R32C/121 Group User's Manual: Hardware Rev.1.10
R32C/145 Group User's Manual: Hardware Rev.1.00
R32C/151 Group User's Manual: Hardware Rev.1.10
R32C/152 Group User's Manual: Hardware Rev.1.10
R32C/153 Group User's Manual: Hardware Rev.1.10
R32C/156 Group User's Manual: Hardware Rev.1.10
R32C/157 Group User's Manual: Hardware Rev.1.10
R32C/160 Group User's Manual: Hardware Rev.1.02
R32C/161 Group User's Manual: Hardware Rev.1.02
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	R32C/100 Series How to Use the Watchdog Timer Automatic Count Start

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 24, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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