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Renesas Electronics Corporation

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M32C/8A Group

Program Download Function

1. Abstract

This document describes methods of downloading a user program into the internal RAM area in M32C/8A using the program download function and executing the downloaded user program in internal RAM.

2. Introduction

The explanation of this document applies to the following MCUs under the use shown in Table 2.1.

Table 2.1 Product List As of Jan. 2008

Type Number	RENESAS Code	ROM Capacity	RAM Capacity	Remarks
M308A0SGP	PLQP0100KB-A (100P6Q-A)	-	12 KB	ROMless
M308A3SGP (P)	PLQP0100KB-A (100P6Q-A)		24 KB	
M308A5SGP (P)	PLQP0144KA-A (144P6Q-A)			

(P): Under Planning

3. Hardware Configuration (Clock Synchronous/Asynchronous)

Figure 3.1 and 3.2 show pin connections for the program download function in M32C/8A.

Mode Setting

Signal	Value
CNVSS	VSS
$\overline{\text{RESET}}$	VSS → VCC1

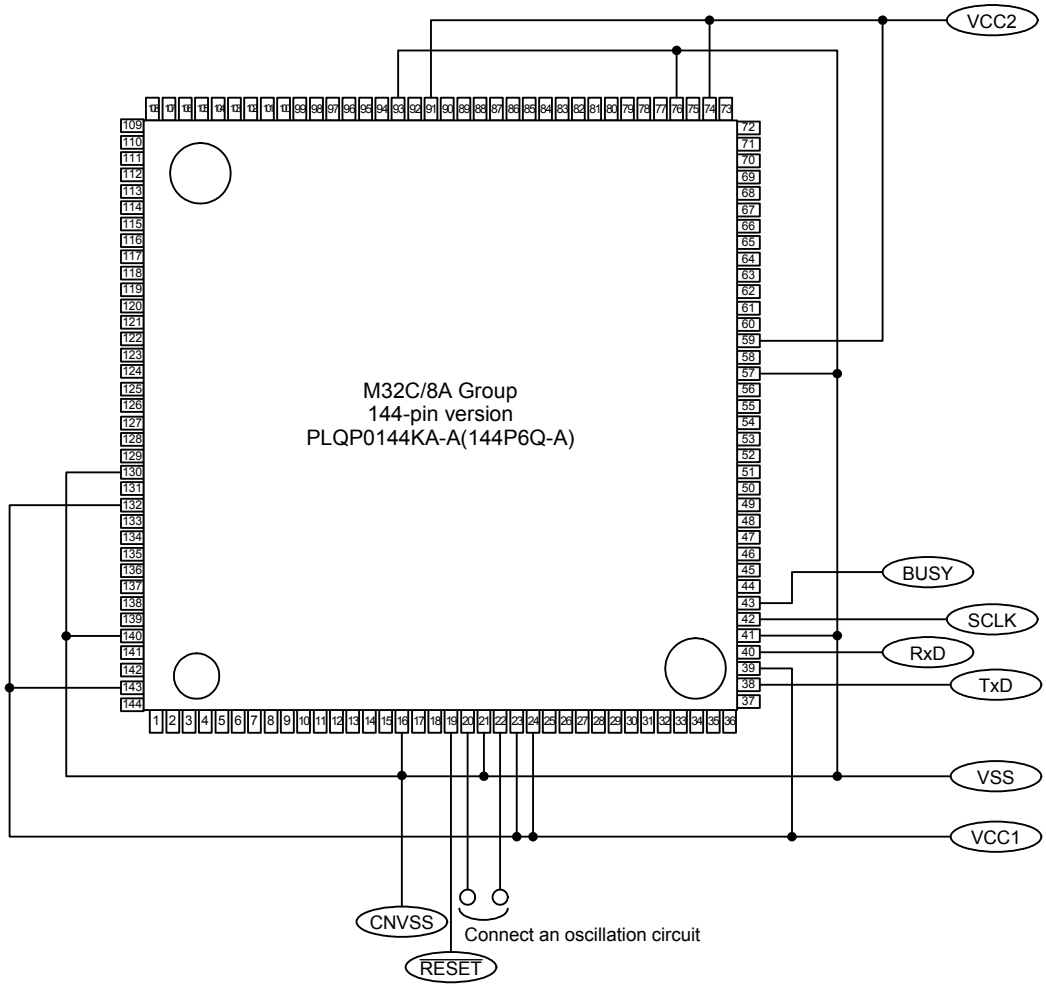


Figure 3.1 Pin Connections for the Program Download Function (144-pin version)

Mode Setting

Signal	Value
CNVSS	VSS
$\overline{\text{RESET}}$	VSS → VCC1

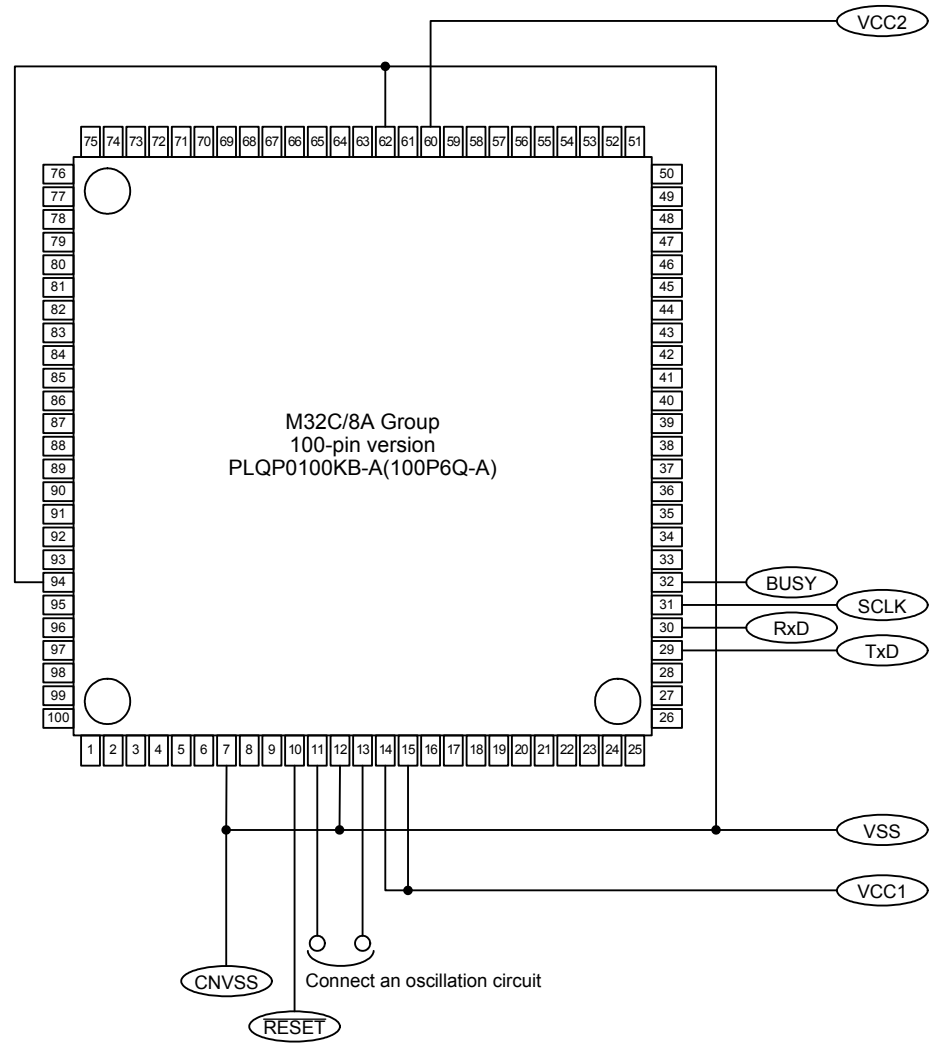


Figure 3.2 Pin Connections for the Program Download Function (100-pin version)

4. Program Download Function

With the program download function, following serial interface modes are used.

- Clock synchronous mode
- Clock asynchronous mode (UART)

Note: Set the operating frequency as below;
Clock synchronous mode: 1 MHz or more
Clock asynchronous mode: 2.4 MHz or more

The program download function starts up by releasing the reset while an “L” signal is applied to the CNVSS pin. Serial data is input using UART1 and transmitted by 8-bit unit. The status of the CLK1 pin at the time of releasing the reset determines either clock synchronous mode or clock asynchronous mode (UART).
To use clock synchronous mode, release the reset while an “H” signal is applied to the CLK1 pin. Four pins of CLK1, RXD1, TXD1, and RTS1 are used in clock synchronous mode. Serial clock is input to the CLK1 pin externally. The RTS1 pin, which is used as the BUSY pin, outputs “L” signal when reception is ready and outputs “H” signal when reception is started.
To use clock asynchronous mode, release the reset while an “L” signal is applied to the CLK1 pin. Two pins of RXD1 and TXD1 are used in clock asynchronous mode.

Pin functions for the program download function lists as follows.

Table 4.1 Pin functions for the Program Download Function

Pin Name	Function	I/O Type	Description
VCC VSS	Power supply input	I	Apply the recommended supply voltage to the VCC1 pin. Apply 0 V to the VSS pin
CNVSS	CNVSS	I	Apply an “L” signal to the pin
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
XIN	Clock input	I	Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT
XOUT	Clock output	O	To use the external clock, input the clock to the XIN pin and leave the XOUT pin open
BYTE	BYTE input	I	Apply an “H” or “L” signal to the pin
AVCC, AVSS	Analog power supply input	I	Connect AVCC to VCC1 Connect AVSS to VSS
VREF	Reference voltage input	I	Reference voltage input pin for the A/D converter
P0_0 to P0_7	Input port P0	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P1_0 to P1_7	Input port P1	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P2_0 to P2_7	Input port P2	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P3_0 to P3_7	Input port P3	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P4_0 to P4_7	Input port P4	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P5_0 and P5_2	Input port P5	I/O	Apply an “H” or “L” signal to the pin, or leave it open
P5_1, P5_3 to P5_7	Input port P5	I	Apply an “H” or “L” signal to the pin, or leave it open
P6_0 to P6_3	Input port P6	I	Apply an “H” or “L” signal to the pin, or leave it open
P6_4	BUSY output	O	Clock Synchronous Mode: BUSY signal output pin Clock Asynchronous Mode: Program operation verify monitor
P6_5	SCLK input	I	Clock Synchronous Mode: Serial clock input pin. This pin needs to be pulled up. Clock Asynchronous Mode: Apply an “L” signal to the pin
P6_6	Data input RXD	I	Serial data input pin
P6_7	Data output TXD	O	Serial data output pin. This pin needs to be pulled up when used in clock synchronous mode.
P7_0 to P7_7	Input port P7	I	Apply an “H” or “L” signal to the pin, or leave it open
P8_0 to P8_4 P8_6, P8_7	Input port P8	I	Apply an “H” or “L” signal to the pin, or leave it open
P8_5	$\overline{\text{NMI}}$ input	I	Apply an “H” signal
P9_0 to P9_7	Input port P9	I	Apply an “H” or “L” signal to the pin, or leave it open
P10_0 to P10_7	Input port P10	I	Apply an “H” or “L” signal to the pin, or leave it open
P11_0 to P11_7	Input port P11	I	Apply an “H” or “L” signal to the pin, or leave it open(1)
P12_0 to P12_7	Input port P12	I	Apply an “H” or “L” signal to the pin, or leave it open(1)
P13_0 to P13_7	Input port P13	I	Apply an “H” or “L” signal to the pin, or leave it open(1)
P14_0 to P14_7	Input port P14	I	Apply an “H” or “L” signal to the pin, or leave it open(1)
P15_0 to P15_7	Input port P15	I	Apply an “H” or “L” signal to the pin, or leave it open(1)

I: Input O: Output I/O: Input and output
NOTE:
1.These pins are provided in the 144-pin package only.

4.1 Clock Synchronous Mode

In clock synchronous mode, using four-wire clock synchronous serial I/O (UART1). To enter clock synchronous mode, release the reset while an “H” signal is applied to the CLK1 pin.

4.1.1 Data Transfer Method and Timing Characteristics

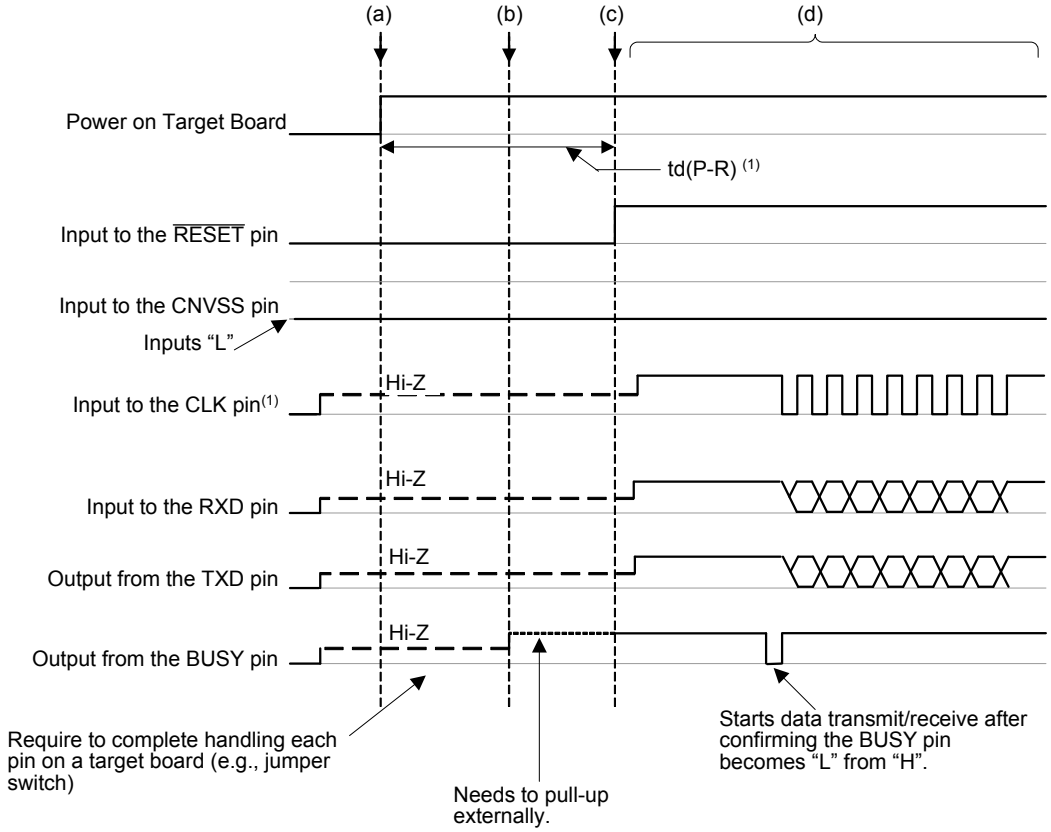
M32C/8A communicates binary format data with 8-bits unit and LSB first. When receiving, the program download command and the download program are loaded into the internal RAM at the rising edge of serial clock input to the CLK1 pin. The BUSY pin becomes “H” during busy period such as processing or receiving. So start the next transfer after the BUSY pin becomes “L”.

4.1.2 Input Timing

Figure 4.1 shows the input/output timing diagram. The program download procedure in clock synchronous mode is shown as follows;

(1) Turn on a target board (Refer to Figure 4.1 (a)) and set input pins to status shown in Figure 4.1 (b).
(2) M32C/8A starts communications in clock synchronous mode by applying “H” to the $\overline{\text{RESET}}$ pin from the status of (1). Apply the CLK1 pin to “H” in M32C/8A after the $\overline{\text{RESET}}$ pin becomes “H”.
(3) M32C/8A becomes the reception waiting status when the initialization is completed and the BUSY pin becomes “L”.
(4) M32C/8A becomes receiving status when data reception is started and the BUSY pin becomes “H”. When reception and data process are completed, the BUSY pin becomes “L” and waits for next data reception.
(5) The program download command is transmitted from a program transmit board and M32C/8A writes them into the internal RAM.
(6) When the checksum values match after completion of writing into the internal RAM, M32C/8A executes the transmitted program from executing start address in the internal RAM. When the checksum values do not match, M32C/8A initializes the internal RAM then waits for (3) process in this procedure.

(a) Turn on a target board
(b) Turn on a program transmit board
(c) M32C/8A starts communications in clock synchronous mode by releasing the reset while an "H" signal is applied to the $\overline{\text{RESET}}$ pin
(d) Input download function command



Note
1. Internal power supply stabilization time

Figure 4.1 Timing Diagram of pin input/output in M32C/8A (Clock Synchronous Mode)

4.2 Clock Asynchronous Mode (UART)

In clock asynchronous mode, using two-wire clock asynchronous serial I/O (UART1). To enter clock asynchronous mode, release the reset while an “L” signal is applied to the CLK1 pin.

4.2.1 Data Transfer Method and Timing Characteristics

M32C/8A communicates binary format data with 8-bits unit, LSB first, one stop bit, and parity disabled.

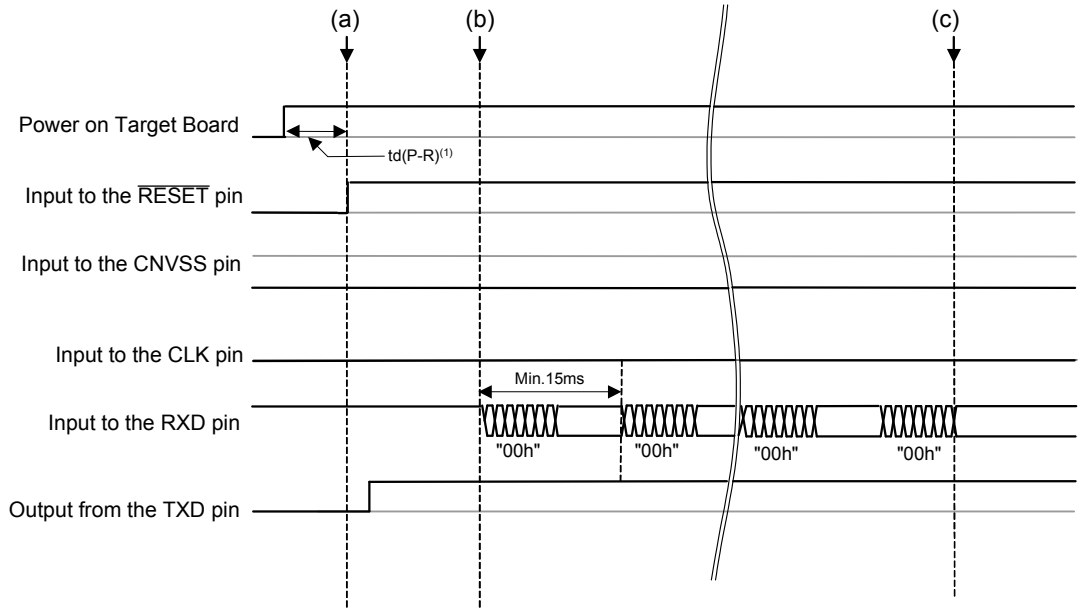
4.2.2 Data Transmit Procedure

Figure 4.2 shows the input timing diagram. The data transmit procedure is shown as follows;

(1) Turn on a target board and release the reset (Refer to Figure 4.2 (a)).
(2) Transmit the standard time data “00h“ 16 times for intervals of 15 ms or more at 9600 bps from a program transmit board. M32C/8A sets UART1 baud rate register to a value corresponding to operating frequency by receiving “00h“ 16 times and completes initial communication .
(3) The program download command is transmitted from a program transmit board and M32C/8A writes them into the internal RAM.
(4) When the checksum values match after completion of writing into the internal RAM, M32C/8A executes the transmitted program from executing start address in the internal RAM. When the checksum values do not match, M32C/8A initializes the internal RAM then waits for (3) process in this procedure .

When a communication error occurs, execute (2) in the procedure again after resetting a target board.

(a) Release the reset on a target board and communication is started in clock asynchronous mode
(b) Initial communication is started
(c) Initial communication is completed after "00h" is received 16 times.



Note:
1. Wait for *td(P-R)* (internal power supply stabilization time) or more after the voltage applied to the VCC1 pin rises above 3.0 V.

Figure 4.2 Timing Diagram of pin input in M32C/8A (Clock Asynchronous Mode)

5. Program Download Command

5.1 Program Download Command

With the program download command, a download program and a checksum value of the download program are transmitted. Table 5.1 shows the transmit data.

A download program is stored from address 600h in the internal RAM.
After receiving the program download command, M32C/8A calculates a checksum value from a download program and compares the calculated checksum value with the checksum value in the transmitted program. When the calculated checksum value matches the checksum value in the transmitted program, a download program stored in the internal RAM is executed. When the two checksum values do not match, M32C/8A resets the internal RAM and goes back to the command waiting status.
When M32C/8A resets after the program download command is executed, the download program is remained in the internal RAM.

Note: The first 8 bytes of the download program is allocated as data area for a version number. Set a version number in the download program.
e.g.) .byte 'VER.1.00'

(Transmit Procedure)

(1) A command code "FAh" is transmitted at the first byte in a transmit data.
(2) The low-order byte of a program size is transmitted at the second byte and the high-order byte of a program size is transmitted at the third byte in a transmit data.
(3) A checksum value is transmitted at the fourth byte in a transmit data.
(4) Program data is transmitted from the fifth byte and the subsequent bytes in a transmit data. The transmittable program size varies depending on the capacity of the internal RAM (Refer to 5.3 Memory Map).

(Calculation of the checksum value)
The checksum value is the eight low-order bits of the total value of program data transmitted from the fifth byte.

Table 5.1 Transmit and Receive Data of the Program Download Function

Pins	1st byte	2nd byte	3rd byte	4th byte	5th byte	(N + 4)th byte
	command	Program size (N)		Checksum	Program data	Program data
RXD (Program transmit board → MCU)	FAh	Low-order of program size	High-order of program size	Checksum value	Program data (first byte)	Program data (N-th byte)
TXD (MCU → Program transmit board)						

5.2 Storing Address for Download Program

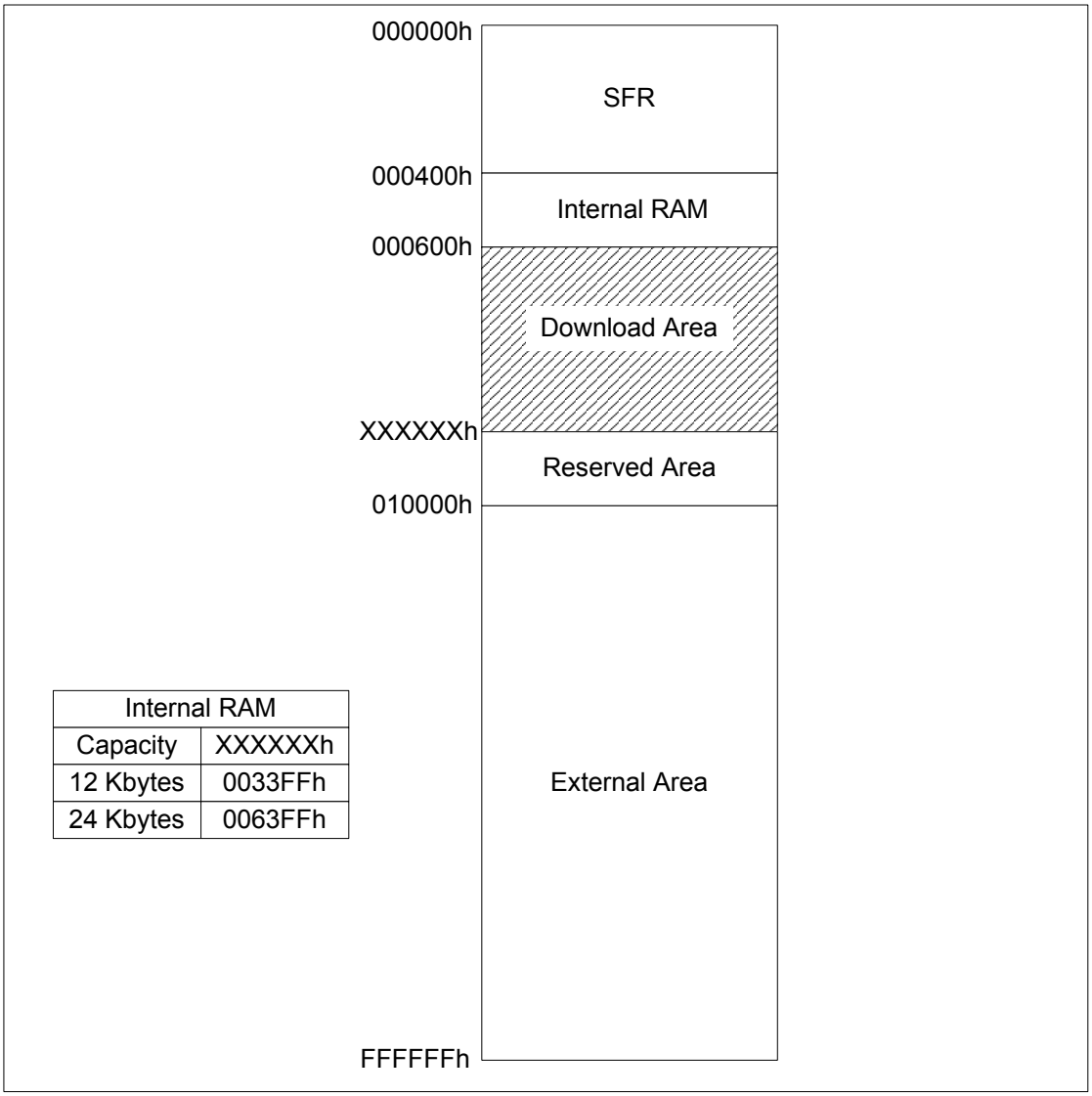
The download program is stored from the storing address in the internal RAM shown in Table 5.2. The first 8 bytes of the download program is allocated for the version number. Therefore, as shown in Table 5.2, adding 8 bytes to the Storing Address value indicates the value of the Executing Start Address.

Table 5.2 Download Address in M32C/8A

Group	Storing Address	Executing Start Address
M32C/8A	600h	608h

5.3 Memory Map

Figure 5.1 shows a download area on the memory in M32C/8A.



Internal RAM	
Capacity	XXXXXXh
12 Kbytes	0033FFh
24 Kbytes	0063FFh

Figure 5.1 Download Area

6. Example of Download Program

Configure a version number at the beginning of the download program shown in Figure 6.1.

```
        .section    rom    ,code
        .org        0600h

    Load:
        .byte       'VER.1.00'

    RESET:
            User Program starts here.
```

Figure 6.1 Example of Download Program

7. Reference Document

Hardware Manual
M32C/8A Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Technology Web site.)

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REVISION HISTORY	M32C/8A Group Program Download Function

Rev.	Date	Description	
		Page	Summary
1.10	Mar 05, 2008	–	First Edition issued

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