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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# M32C/85 Group

## Procedure to Use the PLL Clock as the CPU Clock Source

### 1. Abstract

This application note describes a procedure to use the PLL clock as the CPU clock source.

### 2. Introduction

This application note is applied to the following condition:

Applicable MCU:M32C/85 Group

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFR (Special Function Registers) as the M32C/85 Group. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

### 3. Detailed Description

The PLL-synthesized main clock becomes the PLL clock. To select the PLL clock as the CPU clock source, multiply and divide the main clock by given values.

Table 1 lists the PLL clock settings.

Table 1. PLL Clock Settings

The PLC02 to PLC00 bits in the PLC0 register (to select the programmable counter)	The PLC12 bit in the PLC1 register (to select a PLL clock division)	Multiply	m=f(XIN)
			PLL clock
011 (multiply-by-6)	0 (divide-by-2)	Multiply-by-3	3 m
	1 (divide-by-3)	Multiply-by-2	2 m
100 (multiply-by-8)	0 (divide-by-2)	Multiply-by-4	4 m
	1 (divide-by-3)	Multiply-by-8/3	8/3 m

Figure 1 shows a flowchart to select the PLL clock as the CPU clock source.

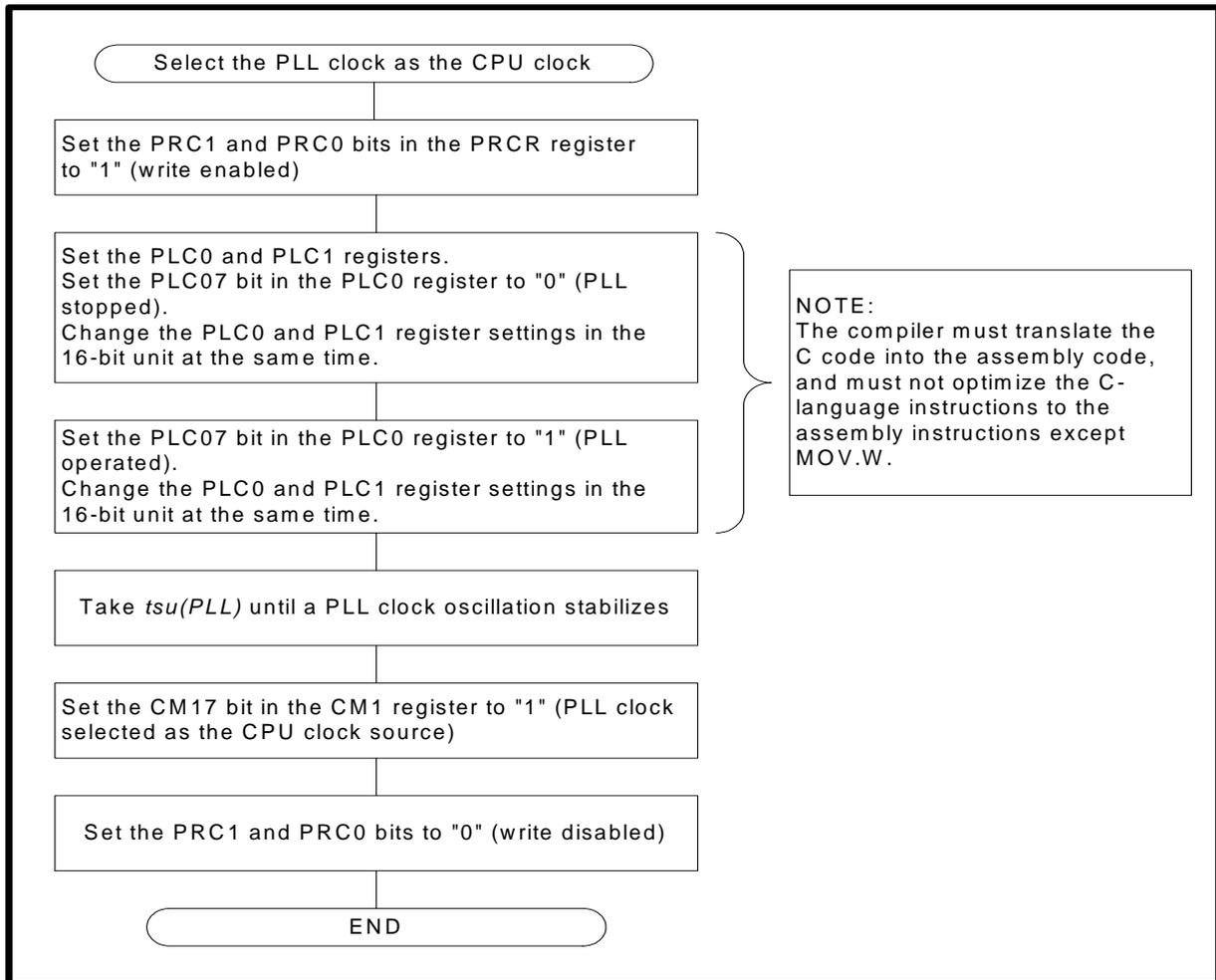


Figure 1. Flowchart to Select the PLL Clock as the CPU Clock Source

#### 4. Sample Program

```

/*****FILE COMMENT*****/
* System Name      : M32C/85 Program Collection
* File Name       : rjj05b0719_src.c
* Version        : 1.00
* Contents       : Procedure to use PLL clock as CPU clock source
* Customer      :
* Model         :
* Order        :
* CPU          : M32C/85 Group
* Compiler     : NC308WA (V.5.20 Release 1)
* OS           : Nothing
* Programmer   :
* Note        :
*****/
* Copyright,2005 RENESAS TECHNOLOGY CORPORATION
* AND RENESAS SOLUTIONS CORPORATION
*****/
* History   : 2005.2.28 Ver 1.00
/*****FILE COMMENT*****/

/*****/
/*  include file          */
/*****/
#include "sfr32c85.h"

/*****/
/*  define                */
/*****/
typedef unsigned short  USHORT16;

#define plc_reg          (volatile)plc  /* PLL control register 0,1 */
#define PLL_WAIT_1MS    800U           /* 1msec @8MHz */
#define PLL_WAIT_CNT    5U             /* 5msec */

/*****/
/*  Declaration of function prototype */
/*****/
void main(void);

/*****/
/*  main                  */
/*****/
void main(void){

    USHORT16  i,j;
  
```



```

for (i = 0; i < PLL_WAIT_CNT; i++) {          /* about 5ms wait */
    for (j = 0; j < PLL_WAIT_1MS; j++) {      /* Main clock 8MHz */
        }
    }

cm1 = 0xa0;
/* System clock control register 1           */
/* 10100000B                                 */
/* | | | | | | | |                            */
/* | | | | | | | +----- (CM10):All clock stop control bit */
/* | | | | | | |         0:Clock oscillates                */
/* | | | +++++----- (b4-b1):Reserved bit (Set to "0")    */
/* | | +----- (b5):Reserved bit (Set to "1")             */
/* | +----- (b6):Reserved bit (Set to "0")              */
/* +----- (CM17):CPU clock select bit 1                 */
/*         1:PLL clock                                     */

prcr = 0x00;                                     /* Protect on */

while(1) {
}
}

```

5. Reference

Hardware Manual

M32C/85 Group Hardware Manual Rev.1.03

(Use the latest version on the home page: <http://www.renesas.com/en/m16c>)

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	2005.09.16	-	First edition issued

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