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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group
Operation of Watchdog Timer

1.0 Abstract
The following is an operation of the watchdog timer.

2.0 Introduction
Operation (1) Writing to the watchdog timer start register initializes the watchdog timer to $7FFF_{16}$ and causes it to start a down count.

(2) With a count in progress, writing to the watchdog timer start register again initializes the watchdog timer to $7FFF_{16}$ and causes it to resume counting.

(3) Either executing the WAIT instruction or going to the stopped state causes the watchdog timer to hold the count in progress and to stop counting. The watchdog timer resumes counting after returning from the execution of the WAIT instruction or from the stopped state.

(4) If the watchdog timer underflows, it is initialized to $7FFF_{16}$ and continues counting. At this time, a watchdog timer interrupt occurs.

Figure 1 shows the operation timing

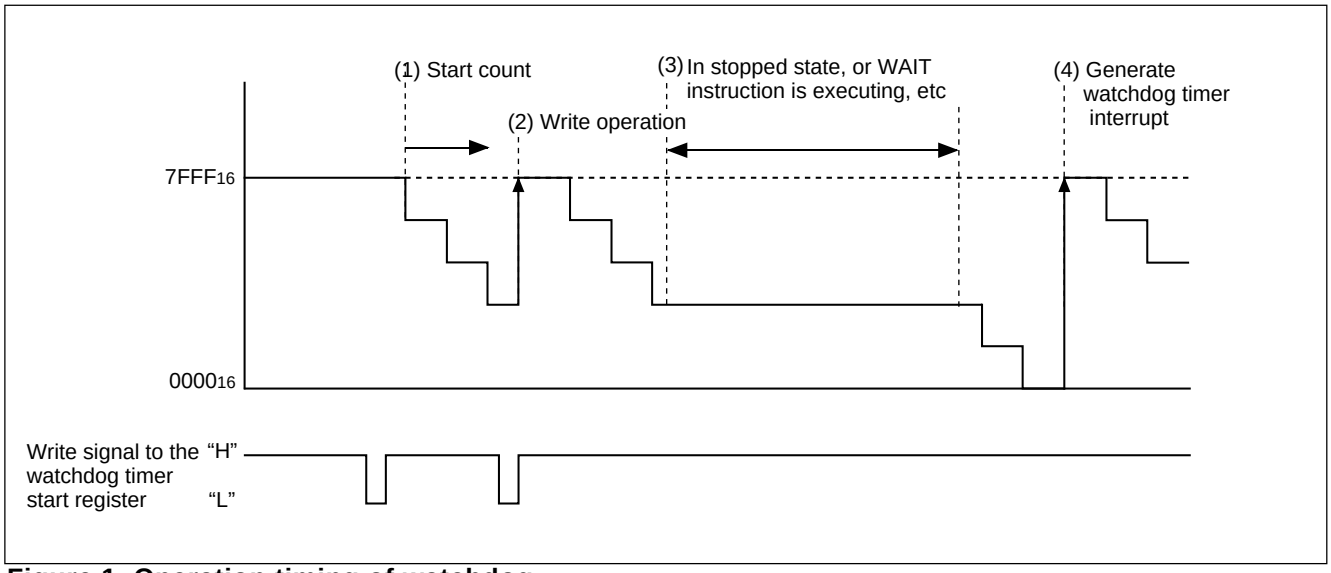
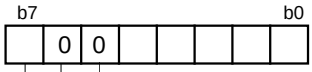


Figure 1. Operation timing of watchdog

3.0 Set-up procedure

Setting watchdog timer control register

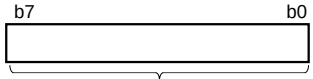


Watchdog timer control register [Address 000F16]
WDC

Reserved bit
Must always be set to “0”

Prescaler select bit
0 : Divided by 16
1 : Divided by 128

Setting watchdog timer start register

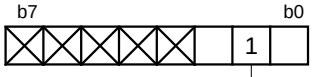


Watchdog timer start register [Address 000E16]
WDTS

The watchdog timer is initialized and starts counting with a write instruction to this register. The watchdog timer value is always initialized to “7FFF16” regardless of the value written.

Generating watchdog timer interrupt

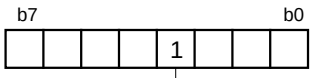
Clearing the protect



Protect register [Address 000A16]
PRCR

Enables writing to processor mode registers 0 and 1 (addresses 000416 and 000516)
1 : Write-enabled

Software reset



Processor mode register 0 [Address 000416]
PM0

Software reset bit
The device is reset when this bit is set to “1”. The value of this bit is “0” when read.

4.0 Programming Code

```
;***************************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0064_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of Watchdog Timer
;   HISTORY   : 2003.05.16  Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;
;***************************************************************************************
;***************************************************************************************
;       Include
;***************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;***************************************************************************************
;       Symbol definition
;***************************************************************************************
RAM_TOP         .EQU    00400H      ;Start address of RAM
RAM_END         .EQU    00FFFH      ;End address of RAM
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
;
;***************************************************************************************
;       Program area
;***************************************************************************************
;=======================================================================
;       Start up
;=======================================================================
        .SECTION    PROGRAM, CODE   ;Declares section name and section type
        .ORG        ROM_TOP         ;Declares start address
RESET:
        LDC      #RAM_END+1, ISP    ;Sets initial value in stack pointer
;
        MOV.B    #03H, prcr         ;Removes protect
                                    ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0    ; Single-chip mode
        MOV.B    #00000000B, pm1    ; No expansion, No wait
                                    ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0    ; Xcin-Xcout High
        MOV.B    #00100000B, cm1    ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr         ;Protects all registers
;
;=======================================================================
;       Watchdog timer
;=======================================================================
        MOV.B    #10000000B,wdc     ;Setting watchdog timer control register
;                 |++-------------;Reserved bit (Must always be set to "0")
;                 +---------------;Prescaler select bit(1:Divided by 128)
;                                  (WDT cycle Approx. 262.1msec @16MHz)
        MOV.B    #1, wdts           ;Setting watchdog timer start register
;
```

```
MAIN:
        ; In the program, write to the watchdog timer start register before
        ; the watchdog timer underflows.
        ; With a count in progress,
        ; writing to the watchdog timer start register again
        ; initializes the watchdog timer and causes it to resume counting.
        ;
        ; When the watchdog timer underflows, a watchdog timer interrupt occurs.
        JMP      MAIN
;
;=============================================================================
;       Interrupt program
;=============================================================================
;-----------------------------------------------------------------------------
;       WDT interrupt occur (Detect a runaway program)
;-----------------------------------------------------------------------------
INT_WDT:
        MOV.B    #02H, prcr    ;Clear the protect
;                  +----------;Enables writing to processor mode registers 0 and 1
RS_LOOP:
        BSET     pm03          ;Software Reset
        JMP      RS_LOOP
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*****************************************************************************
;       Setting of fixed vector
;*****************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    INT_WDT  ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

http://www.renesas.com/

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
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User's Manual

M16C/62A group Rev. 1.0
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