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April 1st, 2010
Renesas Electronics Corporation

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M16C/65 Group

Operation of Timer A (pulse width modulation mode, 8-bit PWM mode)

1. Abstract

In pulse width modulation mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up	
Count source	<input type="radio"/>	Internal count source (f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/fOCO-F/fOCO-S/fc32)
PWM mode	<input type="checkbox"/>	16-bit PWM
	<input type="radio"/>	8-bit PWM
Count start condition	<input type="radio"/>	External trigger input (falling edge of input signal to the TAIIN pin)
	<input type="checkbox"/>	External trigger input (rising edge of input signal to the TAIIN pin)
	<input type="checkbox"/>	Timer overflow (TB2/TAj/TAK overflow)
Output polar control	<input type="radio"/>	Output waveform "H" active
	<input type="checkbox"/>	Output waveform "L" active (output reversed)

Note: $j = i - 1$, but $j = 4$ when $i = 0$; $k = i + 1$, but $k = 0$ when $i = 4$.

4. Operation

- (1) If the TAIIN pin input level changes from "H" to "L" with the count start flag set to "1", the counter performs a down count on the count source. Also, the TAIOUT pin outputs an "H" level.
- (2) The TAIOUT pin output level changes from "H" to "L" when a set time period elapses. At this time, the timer Ai interrupt request bit goes to "1".
- (3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.
- (4) Setting the count start flag to "0" causes the counter to stop and to hold its value. Also, the TAIOUT pin outputs an "L" level.

Note:

- The period of PWM pulses becomes $(m + 1) \times (2^8 - 1) / f_i$, and the "H" level pulse width becomes $n \times (m + 1) / f_i$. If "00h" is set in the eight higher-order bits of the timer Ai register, the pulse width modulator does not work, and the TAIOUT pin outputs "L" level, therefore the timer Ai interrupt request is not generated.
 (f_i : frequency of the count source f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/fOCO-S/fc32; m : values set to timer Ai register's low-order address n : values set to timer Ai register's high-order address)
- When a trigger is generated, the TAIOUT pin outputs "L" level of same amplitude as "H" level of the set PWM pulse, after which it starts PWM pulse output.

Figure 1 shows the operation timing.

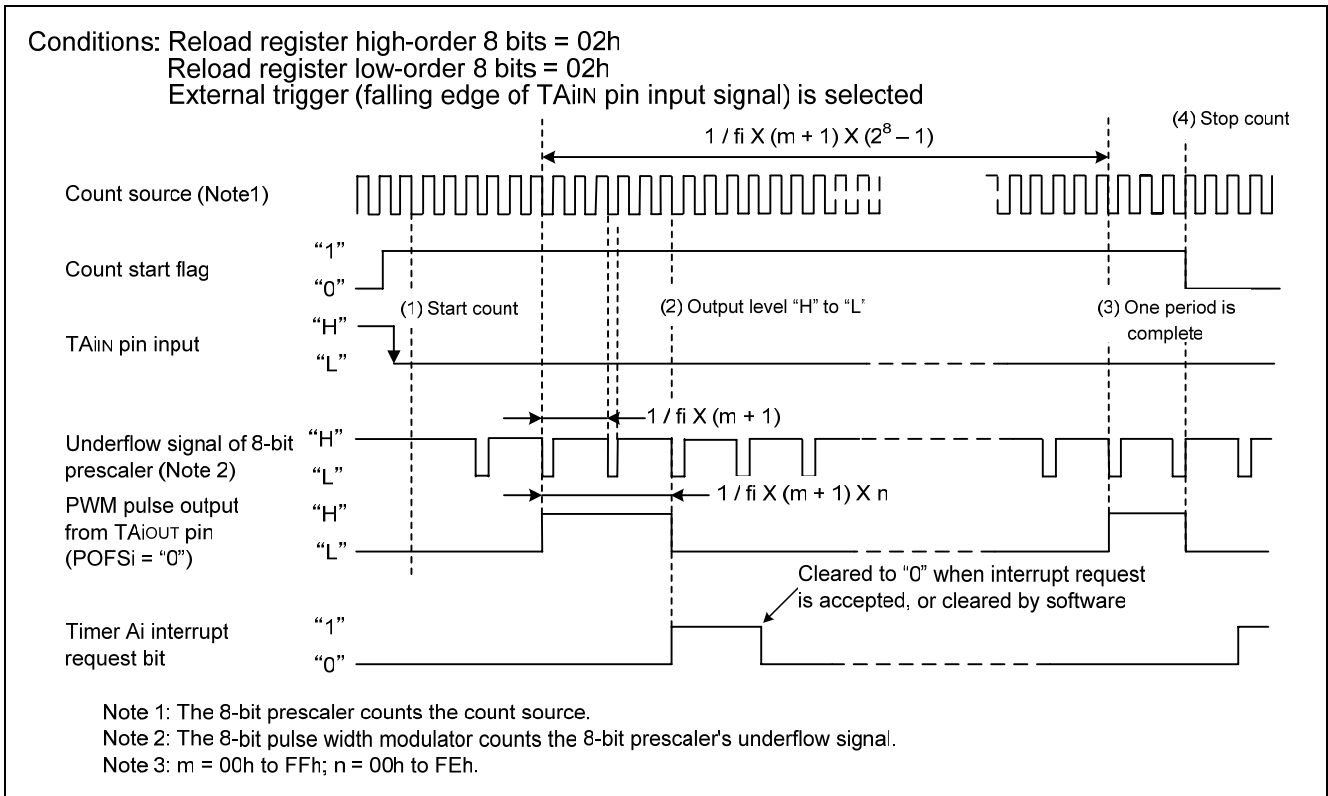


Figure 1. Operation timing of pulse width modulation mode, with 8-bit PWM mode selected

5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

Table 2. Count Source Selection of Timer A

TCKDIV00 register (Note 1)	TACSj register (Note 2)				TAiMR register		Count source	Count source period
	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		
								f(XiN):20MHz f(XciN):32.768kHz f(oco-F):about 20MHz f(oco-s):about 125kHz
0	0	-	-	-	0	0	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns
0	0	-	-	-	0	1	f8TIMAB	400ns
0	0	-	-	-	1	0	f32TIMAB	1600ns
0	0	-	-	-	1	1	fc32	976.56µs
0	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns
0	1	0	0	1	-	-	f8TIMAB	400ns
0	1	0	1	0	-	-	f32TIMAB	1600ns
0	1	0	1	1	-	-	f64TIMAB	3200ns
0	1	1	0	0	-	-	foco-F	about 50ns
0	1	1	0	1	-	-	foco-s	about 8µs
0	1	1	1	0	-	-	fc32	976.56µs
1	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	about 50ns/100ns
1	1	0	0	1	-	-	f8TIMAB	about 400ns
1	1	0	1	0	-	-	f32TIMAB	about 1600ns
1	1	0	1	1	-	-	f64TIMAB	about 3200ns

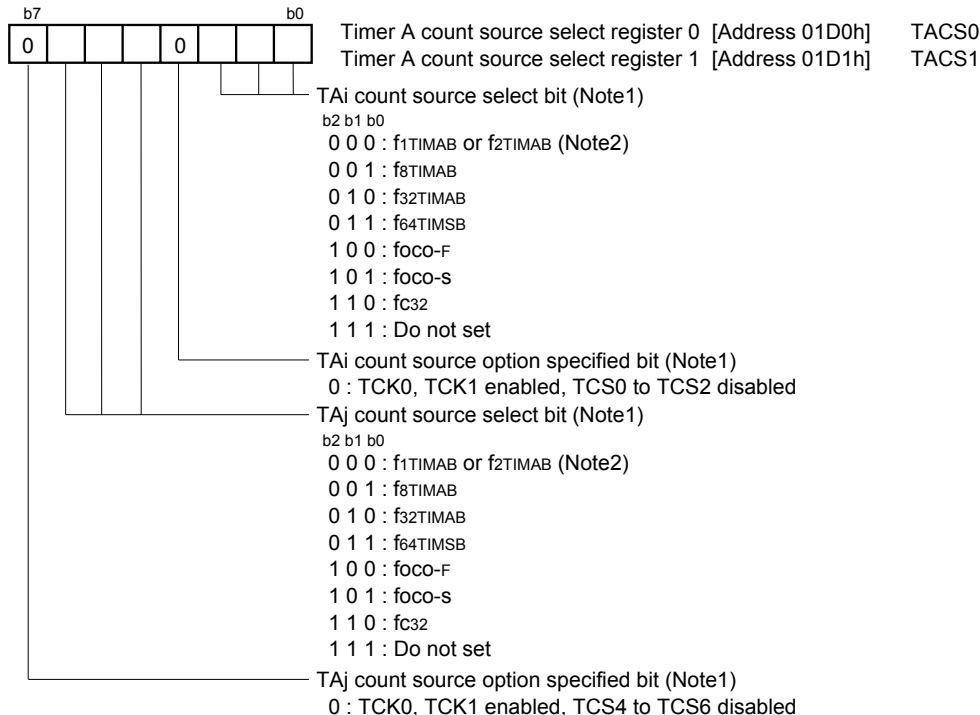
Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Selecting timer count source

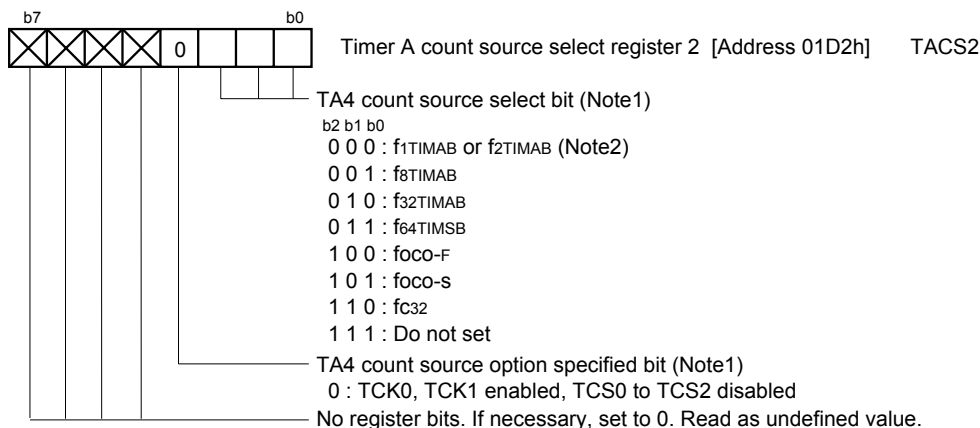
TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count source.



TACS0 register: i = 0, j = 1, TACS1 register: i = 2, j = 3

Note 1: About the count source period, please refer to Table 2.

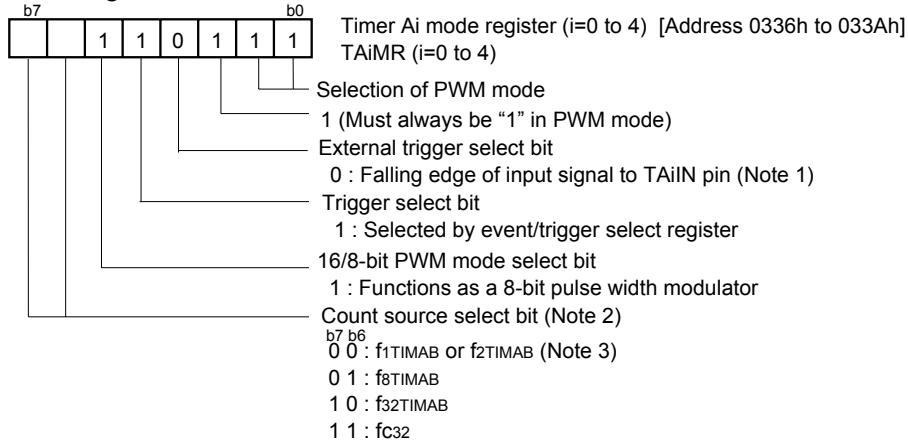
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f₁TIMAB. When the PCLK0 bit is "0", the selected clock source is f₂TIMAB.



Note 1: About the count source period, please refer to Table 2.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f₁TIMAB. When the PCLK0 bit is "0", the selected clock source is f₂TIMAB.

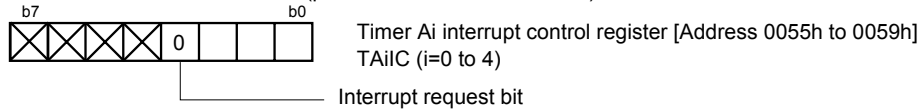
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■
Selecting PWM mode and functions



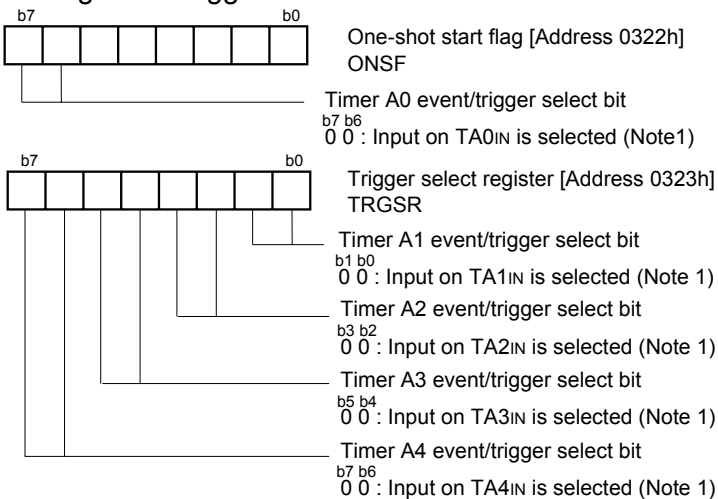
Note 1: Valid when bits TAI_{TGH} and TAI_{TGL} bit in the ONSF register or TRGSR register are set to 00b (TAiIN pin input). Please set the port direction bit for the TAiIN pin to 0 (input mode).
 Note 2: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
 Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

■
Clearing timer Ai interrupt request bit

Refer to 'Precaution for Timer A (pulse width modulation mode)'

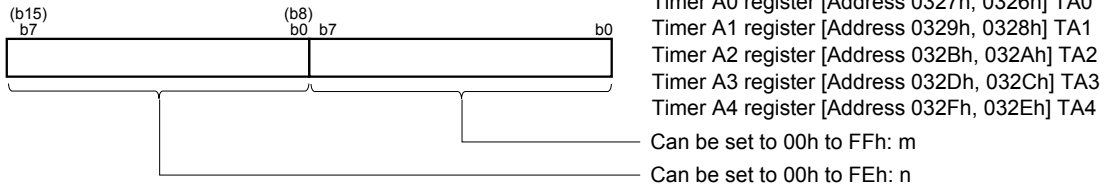


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Setting event/trigger select bit

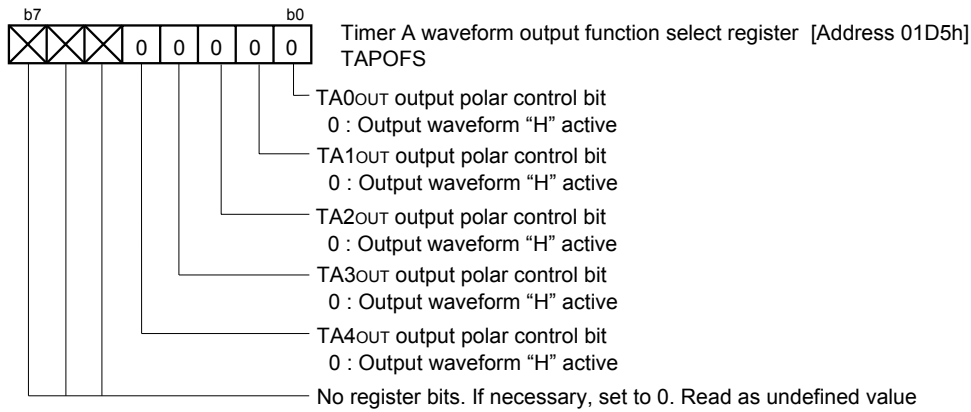


Note 1: Set the port direction bits for the pins TA0IN to TA4IN to 0 (input mode).
■

Setting PWM pulse's period and "H" level width

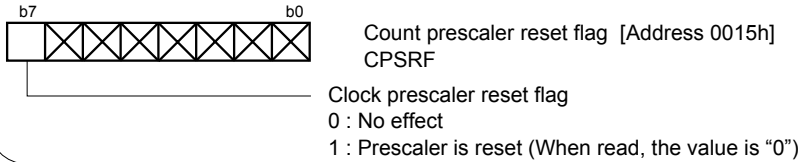


Selecting waveform output function

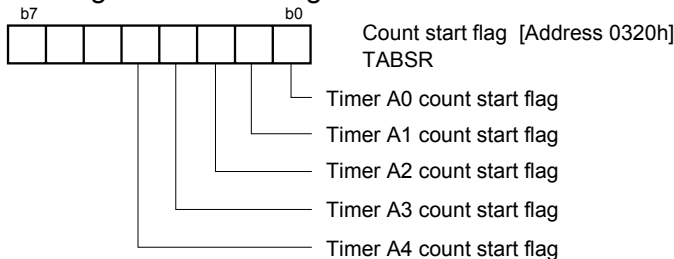


Setting clock prescaler reset flag

(This function is effective when fc32 is selected as the count source. Reset the prescaler for generating fc32 by dividing the XCIN by 32.)



Setting count starts flag



Start count

6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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Revision

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