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April 1st, 2010
Renesas Electronics Corporation

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M16C/65 Group

Operation of Timer A (2-phase pulse signal process in event counter mode, free-run type, multiply-by-4, and Z-phase input)

1. Abstract

In this mode, timer A3 counter can be set to “0” by selecting Z-phase input. Operations of the case which selecting the rising edge by the INT2 polarity select bit are described below. Figure 1 shows the operation timing. A reference program is an example which is based on the setting procedure in this application note, using INT2 interrupt.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Settings

The Z-phase input function can be used only when the timer A3 event counter mode, 2-phase pulse signal process, free running, and multiply-by-4 mode are selected. The Z-phase is input from a ZP pin.

4. Operation

- (1) Setting the count start flag to “1” causes the counter to count the effective edges of the count source.
- (2) Even if an underflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer A3 interrupt request bit goes to “1”.
- (3) Even if an overflow occurs, the content of the reload register is not reloaded to the counter, but the count continues. At this time, the timer A3 interrupt request bit goes to “1”.
- (4) When a rising edge is input to Z-phase (ZP pin (INT2 input)), the timer count value is set to “1”. At this time, the timer A3 interrupt request bit goes to “1”.

Note:

- The Z-phase is input when the INT2 input edge is detected. The edge polarity is selected by the POL bit in the INT2IC register.
- The Z-phase must have a pulse width greater than 1 cycle of the timer A3 count source.
- Set the direction register for TA3IN and TA3OUT pins to “0”.
- Note that a timer A3 interrupt request occurs successively two times when a timer A3 underflows and an INT2 input reloads at the same timing. Do not use the timer A3 interrupt request when this function is used.

Figure 1 shows the operation timing.

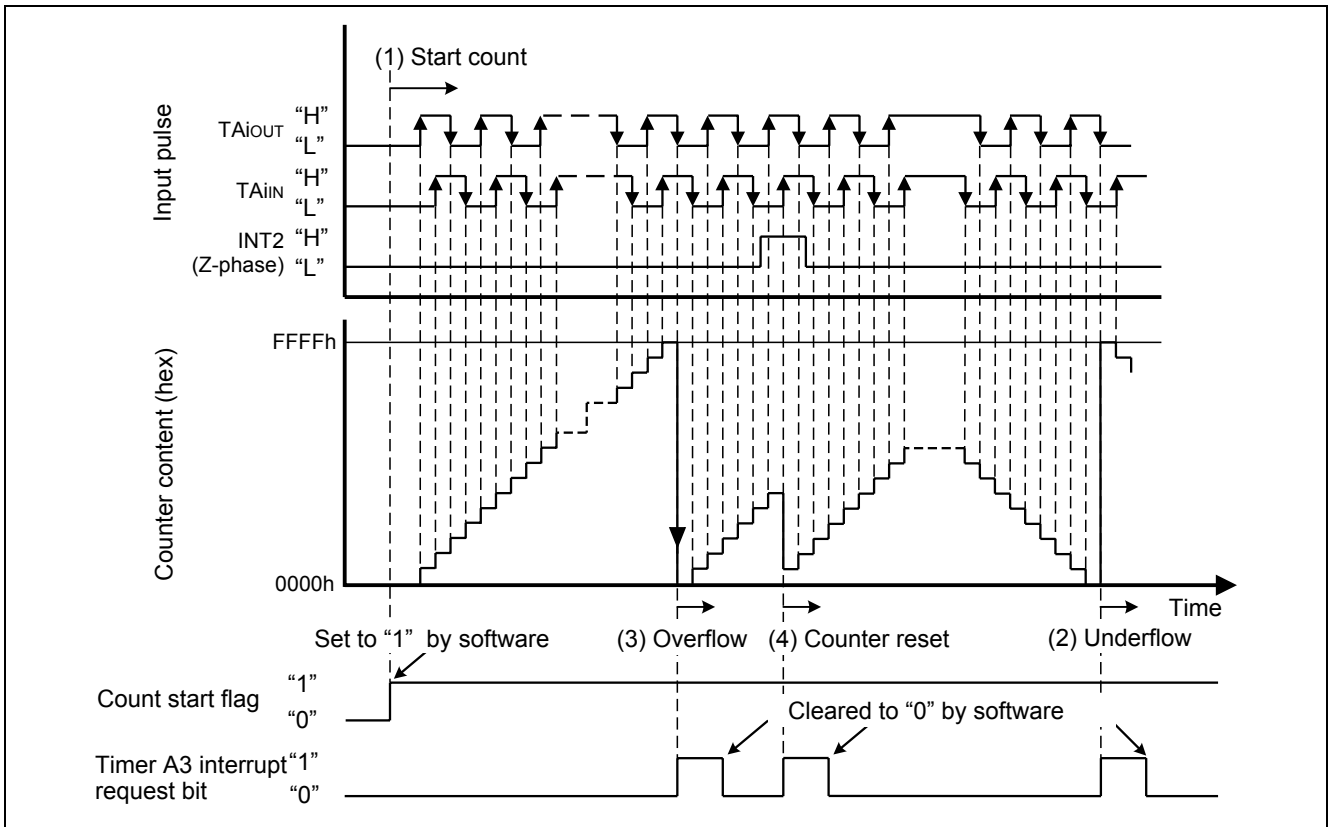
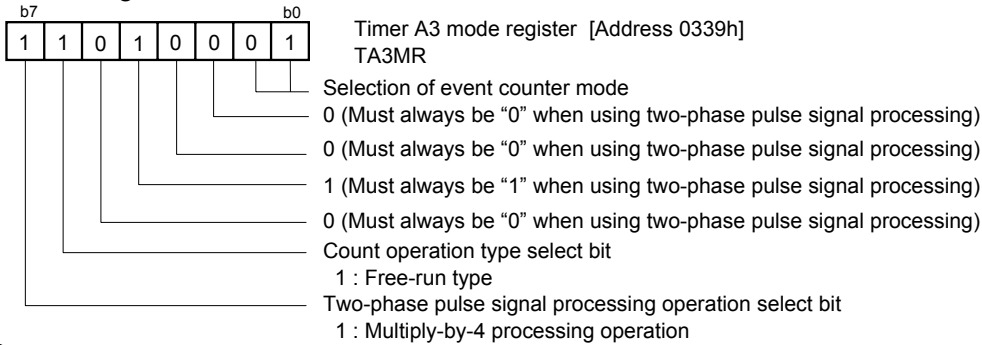


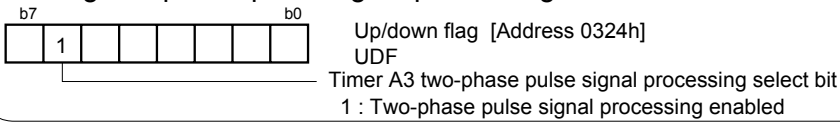
Figure 1. Operation timing of 2-phase pulse signal process in event counter mode, free run type, multiply-by-4, and Z-phase input selected

5. Set-up procedure

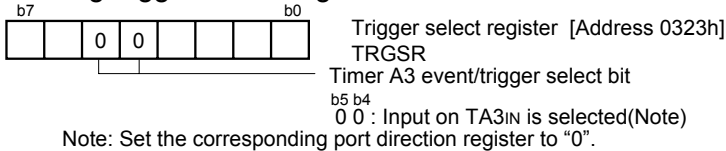
Selecting event counter mode and functions



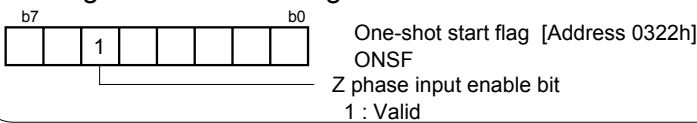
Setting two-phase pulse signal processing select bit



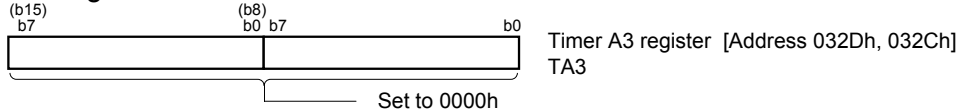
Setting trigger select register



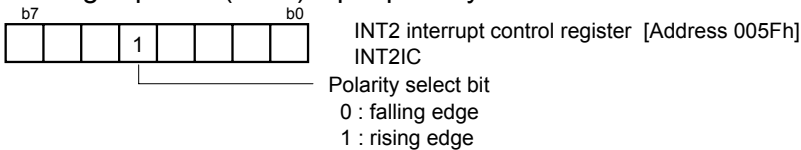
Setting one-shot start flag



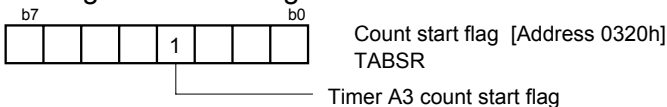
Setting counter value



Setting Z-phase (INT2) input polarity



Setting count start flag



Start count

6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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Revision

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		Page	Point
1.00	2009.10	-	First edition issued

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