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# M16C/65 Group

### Operation of SI/O3,4

#### 1. Abstract

In transmitting data in this mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

#### 2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



#### 3. Chosen functions

#### Table 1. Chosen functions

ltem	Set-up		Item	Set-up	
Transfer clock	0	Internal clock	Souti initial value set function	0	Not use
source		(f1SIO/f2SIO/f8SIO/f32SIO)			
		External clock (CLKi pin)			Used
Transfer	0	LSB first	SOUTI output control function		High-impendance
format		MSB first	(Souti status after transmission)	0	Last bit level retained

#### 4. Operation

(1) Transfer begins upon writing the SI/Oi transmit data. The transmit data is sent out from the SOUTi pin synchronously with falling edges of the transfer clock.

(2) When SOUT finishes sending one byte of data, the interrupt request bit is set to "1".

(3) When the SM26 bit or the SM27 bit in the S34C2 register is set to "1" (last bit level retained), after the transfer is completed, SOUT holds the last data.

Note:

• Data can only be written to the SI/Oi transmit/receive register (i = 3, 4; addresses 0270h, 0274h) when the device is idle neither sending nor receiving data.



Figure 1 shows the operation timing.

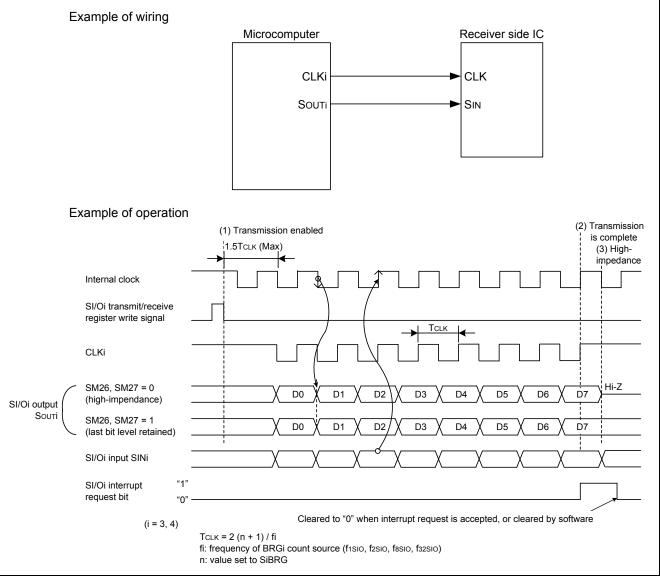


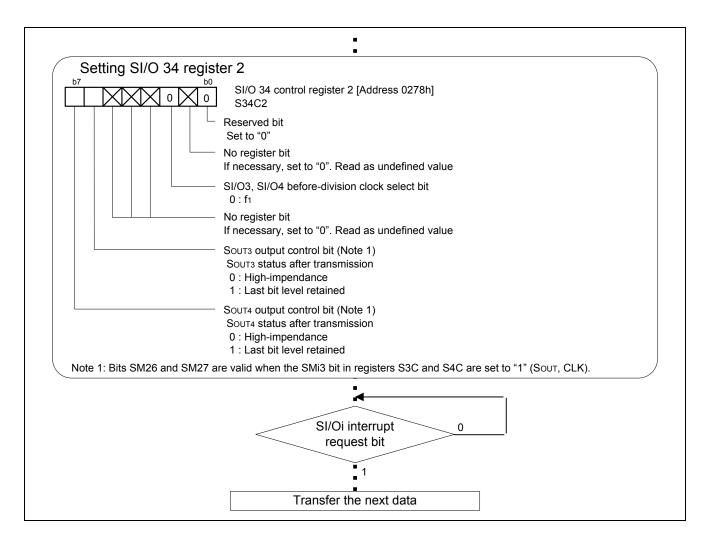
Figure 1. Operation timing of transmission in SI/O3, 4 mode



#### 5. Set-up procedure

	(act to units such ad state)							
	(set to write-enabled state)							
Protect register [Address 000Ah] PRCR								
Enables writing to port P9 direction register (address 03F3h) and SI/Oi								
control register (i=3, 4) (addresses 0272h and 0276h) 1 : Write-enabled								
• Setting SI/Oi transmit/receive control register (i = 3, 4) (Note 1)								
b7 b0 1 0	SI/Oi transmit/receive control register (i = 3, 4) [Address 0272h, 0276h] SiC (i = 3, 4)							
	Internal synchronous clock select bit							
	b1 b0							
	0 0 : Selecting fisio or f2sio 0 1 : Selecting fasio							
	1 0 : Selecting f32SIO							
	1 1 : Do not be set							
	Soυτi output disable bit 0 : Soυτi output							
	SI/Oi port select bit							
	1 : Souti output, CLK function							
	CLK polarity select bit							
	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge							
	1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge							
	Transfer format select bit 0 : LSB first							
	Synchronous clock select bit 1 : Internal clock							
	Souti initial value set bit (Effective when bit 6 = 0)							
	0 : L output 1 : H output							
Note 1: Be sure to set the protect register and SI/Oi control register successively.								
Setting SI/Oi bit rate g	enerator (i = 3, 4)							
	SI/Oi bit rate generator (i = 3, 4) [Address 0273h, 0277h]							
SiBRG (i = 3, 4) Can be set to 00h to FFh (Note 1)								
Note 1: Write to SI/Oi bit rate generator when transmission/reception is halted. Use the MOV instruction to write into the SiBRG register.								
Writing transmit data								
b7 b(								
SI/Oi transmit/receive register (i=3, 4) [Address 0270h, 0274h] SiTRR (i=3, 4)								
	Setting transmission data (Note 1)							
Note 1: Write to SI/Oi transmit	e SiTRR register each time 1-byte data is received, even when data is only received.							







#### 6. Reference

Hardware manual

M16C/65 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update

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#### Revision

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Nev.	issue uale	Page	Point	
1.00	2009.10	-	First edition issued	

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