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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Serial I/O (transmission in UART mode)

1.0 Abstract

In transmitting data in UART mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up		Item	Set-up	
Transfer clock source (Note 1)	O	Internal clock (f_1 / f_8 / f_{32})	Sleep mode (Note 1)	O	Sleep mode off
		External clock (CLKi pin)			Sleep mode selected
$\overline{\text{CTS}}$ function	O	$\overline{\text{CTS}}$ function enabled	Data logic select function (Note 2)	O	No reverse
		$\overline{\text{CTS}}$ function disabled			Reverse
Transmission interrupt factor	O	Transmission buffer empty	TxD, RxD I/O polarity reverse bit (Note 2)	O	No reverse
		Transmission complete			Reverse
			Bus collision detection function (Note 2)	O	Not selected
					Selected

Note 1: UART0, UART1 only.

Note 2: UART2 only.

2.0 Introduction

Operation

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register readies the data transmissible status.

(2) When input to the $\overline{\text{CTSi}}$ pin goes to “L”, transmission starts (the $\overline{\text{CTSi}}$ pin needs to be controlled on the reception side).

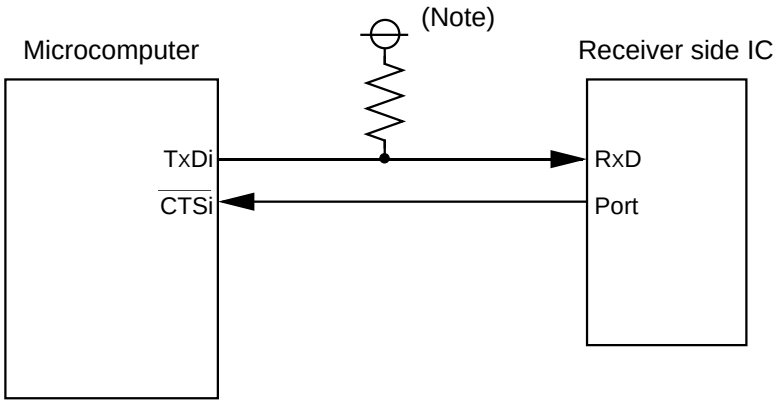
(3) Transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxDi pin. Then, data is transmitted, bit by bit, in sequence: LSB, ····, MSB, parity bit, and stop bit(s).

(4) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to “1”, which indicates that transmission is completed. At this time, the UARTi transmit interrupt request bit goes to “1”. The transfer clock stops at “H” level.

(5) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

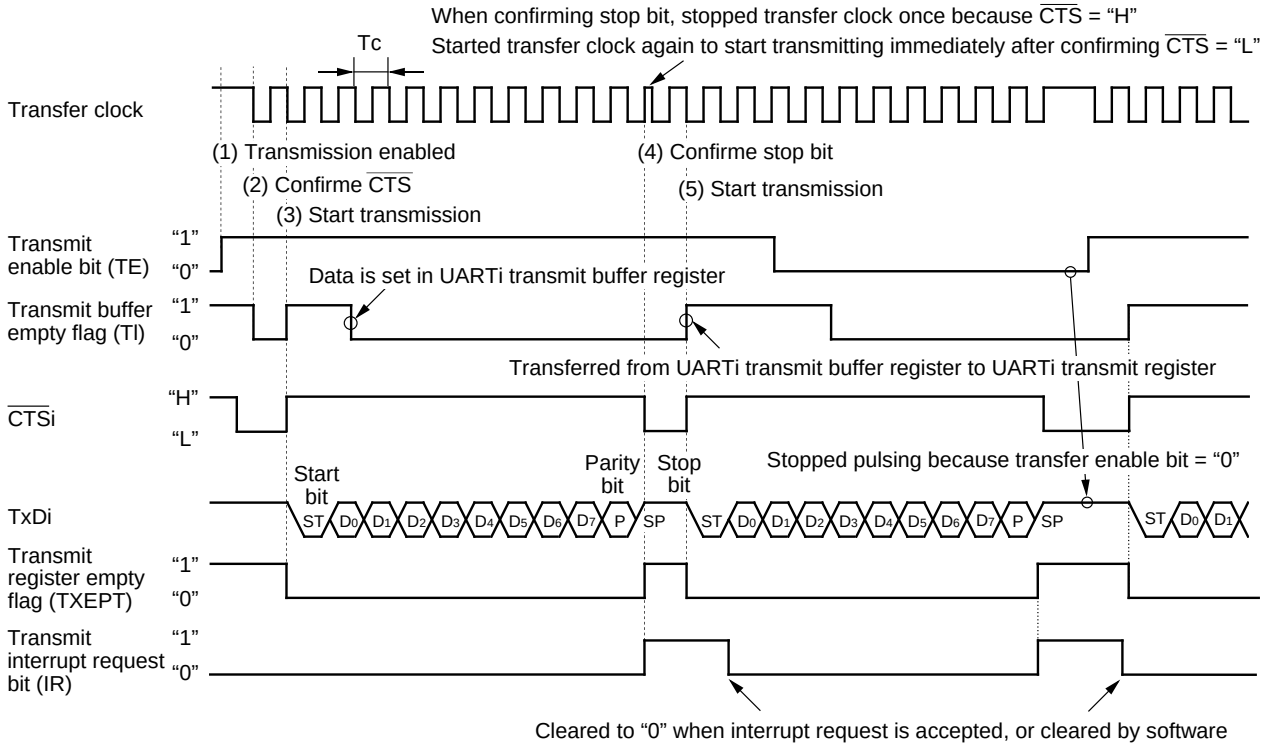
Figure 1 shows the operation timing

Example of wiring



Note: Since TxD2 pin is N-channel open drain, this pin needs pull-up resistor.

Example of operation



Shown in ( ) are bit symbols.

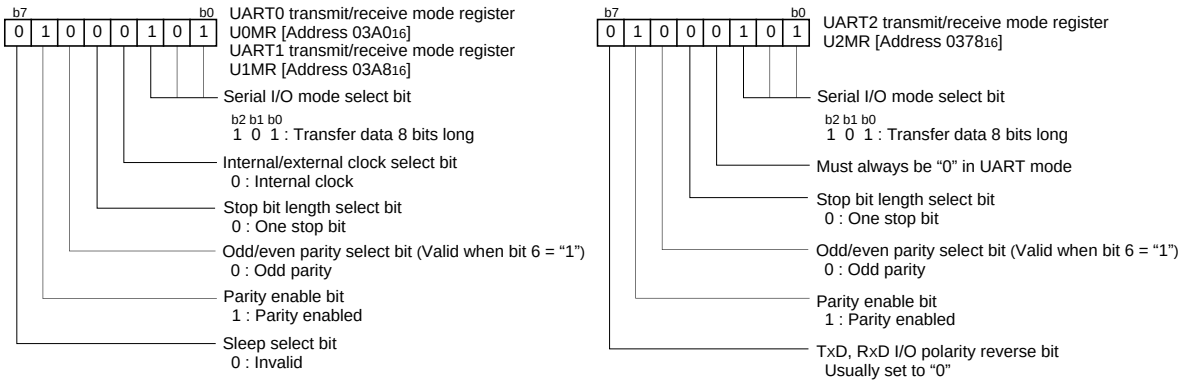
The above timing applies to the following settings :
- Parity is enabled.
- One stop bit.
- CTS function is selected.
- Transmit interrupt cause select bit = "1".

Tc = 16 (n + 1) / fi or 16 (n + 1) / fEXT
fi : frequency of BRGi count source (f1, f8, f32)
fEXT : frequency of BRGi count source (external clock)
n : value set to BRGi

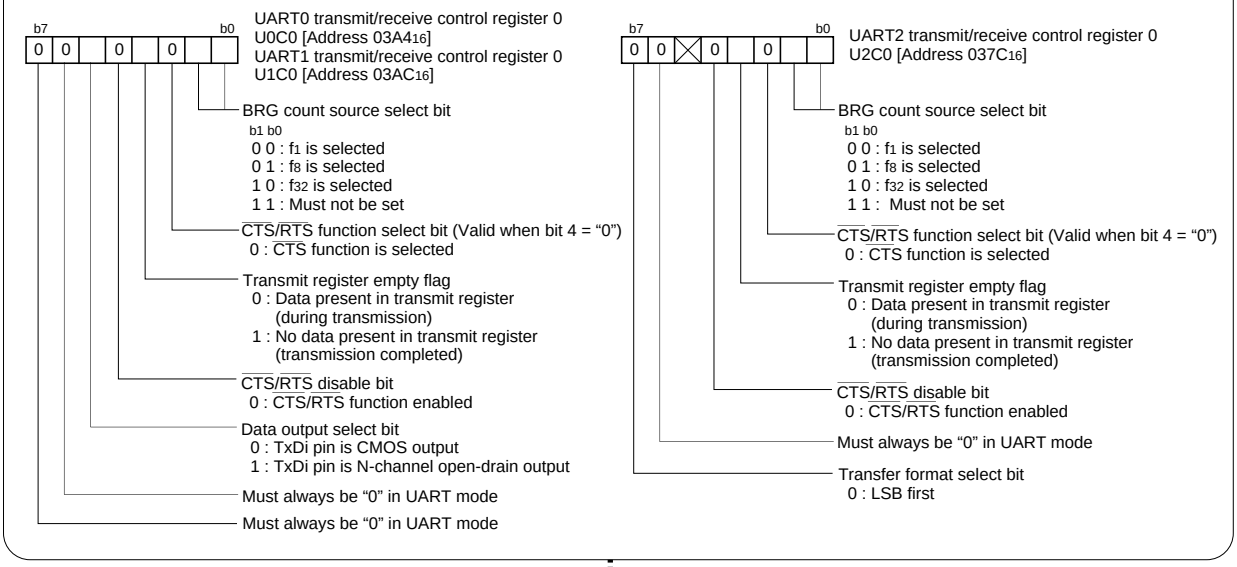
Figure 1. Operation timing of transmission in UART mode

3.0 Set-up procedure

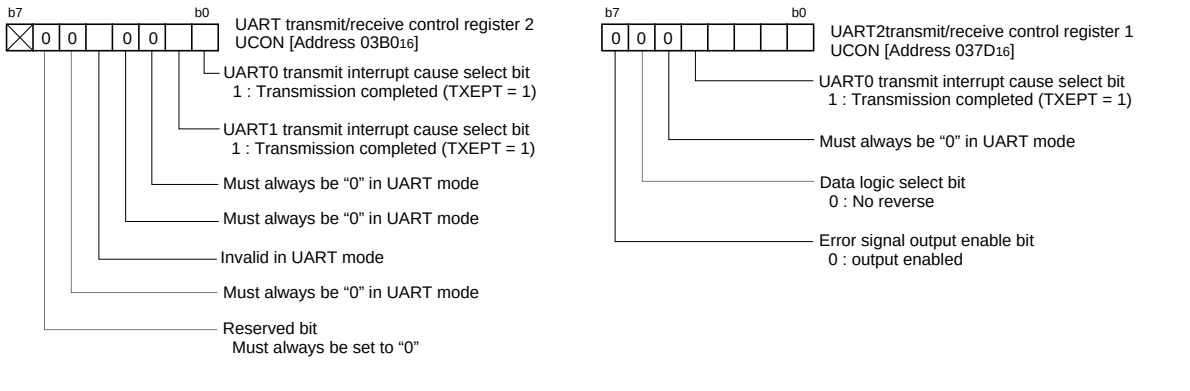
Setting UARTi transmit/receive mode register (i=0 to 2)



Setting UARTi transmit/receive control register 0 (i = 0 to 2)



Setting UART transmit/receive control register 2 and UART2 transmit/receive control register 1



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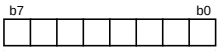
Setting UARTi bit rate generator (i = 0 to 2)

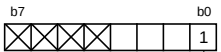


UARTi bit rate generator (i = 0 to 2) [Address $03A1_{16}$, $03A9_{16}$, 0379_{16}]
UiBRG (i = 0 to 2)

Can be set to 00_{16} to FF_{16} (Note)

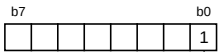
Note: Write to UARTi bit rate generator when transmission/reception is halted.

Transmission enabled



UART0 transmit/receive control register 1
U0C1 [Address $03A5_{16}$]
UART1 transmit/receive control register 1
U1C1 [Address $03AD_{16}$]

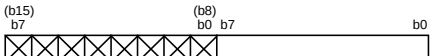
Transmit enable bit
1 : Transmission enabled



UART2 transmit/receive control register 1
U2C1 [Address $037D_{16}$]

Transmit enable bit
1 : Transmission enabled

Writing transmit data



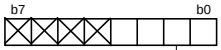
UART0 transmit buffer register [Address $03A3_{16}$, $03A2_{16}$] U0TB
UART1 transmit buffer register [Address $03AB_{16}$, $03AA_{16}$] U1TB
UART2 transmit buffer register [Address $037B_{16}$, $037A_{16}$] U2TB

Setting transmission data

When $\overline{CTSi}$ input level = "L"

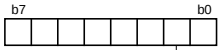
Start transmission

Checking the status of UARTi transmit/receive control (i = 0 to 2)



UART0 transmit/receive control register 1
U0C1 [Address $03A5_{16}$]
UART1 transmit/receive control register 1
U1C1 [Address $03AD_{16}$]

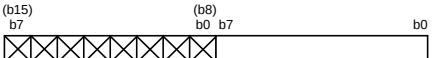
Transmit buffer empty flag
0 : Data present in transmit buffer register
1 : No data present in transmit buffer register
(Writing next transmit data enabled)



UART2 transmit/receive control register 1
U2C1 [Address $037D_{16}$]

Transmit buffer empty flag
0 : Data present in transmit buffer register
1 : No data present in transmit buffer register
(Writing next transmit data enabled)

Writing next transmit data



UART0 transmit buffer register [Address $03A3_{16}$, $03A2_{16}$] U0TB
UART1 transmit buffer register [Address $03AB_{16}$, $03AA_{16}$] U1TB
UART2 transmit buffer register [Address $037B_{16}$, $037A_{16}$] U2TB

Setting transmission data

Transmission is complete

4.0 Programming Code

```
;***********************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0048_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of Serial I/O
;               (transmission in UART mode)
;   HISTORY   : 2003.05.16  Ver 1.00
;
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;
;***********************************************************************************
;***********************************************************************************
;       Include
;***********************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;***********************************************************************************
;       Symbol definition
;***********************************************************************************
RAM_TOP          .EQU    00400H     ;Start address of RAM
RAM_END          .EQU    00FFFH     ;End address of RAM
ROM_TOP          .EQU    0F8000H    ;Start address of ROM
FIXED_VECT_TOP   .EQU    0FFFDCH    ;Start address of fixed vector
;
;***********************************************************************************
;       Allocation of work RAM area
;***********************************************************************************
        .SECTION    WORKRAM, DATA
        .ORG        RAM_TOP
WORKRAM_TOP:
C_POWER          .EQU    3
C_DATA_SIZE      .EQU    (1<< C_POWER)  ;Data size
v_Trans_data:    .BLKB   C_DATA_SIZE    ;Area of send data for sample
WORKRAM_END:
;
;***********************************************************************************
;       Program area
;***********************************************************************************
;=================================================================================
;       Start up
;=================================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
        MOV.B    #03H, prcr        ;Removes protect
                                   ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0   ; Single-chip mode
        MOV.B    #00000000B, pm1   ; No expansion, No wait
                                   ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0   ; Xcin-Xcout High
        MOV.B    #00100000B, cm1   ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr        ;Protects all registers
;
```

```
        ; Clears WORKRAM area
        MOV.W    #0, R0
        MOV.W    #(RAM_END-RAM_TOP)/2, R3
        MOV.W    #WORKRAM_TOP, A1
        SSTR.W

        ; Makes transmit data for sample ( 1 to C_DATA_SIZE )
        MOV.B    #1, R0L               ;1st data
        MOV.W    #0, A0                ;Initialize offset address
MAKE_DATA:                             ;
        MOV.B    R0L, v_Trans_data[A0] ;
        ADD.B    #1, R0L               ;
        ADD.W    #1, A0                ;
        CMP.W    #C_DATA_SIZE, A0      ;
        JLTU     MAKE_DATA             ;
;
;=============================================================================
;       Serial I/O (transmission in UART mode)
;=============================================================================
        MOV.B    #01000101B, u0mr  ;Setting UART0 transmit/receive mode register
;                 |||||+++---------;Serial I/O mode select bit (101:Transfer data 8 bits long)
;                 ||||+------------;Internal/external clock select bit (0:Internal clock)
;                 |||+-------------;Stop bit length select bit (0:One stop bit)
;                 ||+--------------;Odd/even parity select bit (0:Odd parity)
;                 |+---------------;Parity enable bit (1:Parity enabled)
;                 +----------------;Sleep select bit (0:Invalid)
        MOV.B    #00001000B, u0c0  ;Setting UART0 transmit/ receive control register 0
;                 ||||||++---------;BRG count source select bit (00:f1 is selected)
;                 |||||+-----------;CTS function is selected (Valid when bit 4="0") (Note)
;                 ||||+------------;Transmit register empty flag (Write disable)
;                 |||+-------------;CTS/RTS disable bit (0:CTS/RTS function enabled)
;                 ||+--------------;Data output select bit (0:TxDi pin is CMOS output)
;                 ++---------------;Must always be "0" in UART mode
        BCLR     pd6_0             ;(Note) CTS:Set the corresponding port direction register to "0"
        MOV.B    #00000001B, ucon  ;Setting UART transmit/receive control register 2
;                  ||||||+---------;UART0 transmit interrupt cause select
;                  ||||||           (1:Transmission completed)
;                  |||||+----------;UART1 transmit interrupt cause select
;                  |||++-----------;Must always be "0" in UART mode
;                  ||+-------------;Invalid in UART mode
;                  |+--------------;Must always be "0" in UART mode
;                  +---------------;Reserved bit (Must always be set to "0")
        MOV.B    #103, u0brg       ;Setting UART0 bit rate generator (Approx. 9600bps @16MHz,f1)

        MOV.B    #00000001B, u0c1  ;Transmission enabled
;                        +---------;Transmission enabled
;
```

```
;=======================================================================
;       Main program
;=======================================================================
        MOV.W    #0, A0                ;Initialize offset
WRITE_DATA:
        MOV.B    v_Trans_data[A0], u0tb;Writing transmit data
;
WAIT_TRANS:
        BTST     ti_u0c1               ;Checking the status of UART0 transmit buffer empty flag
        JNC      WAIT_TRANS
;
PREPARE_NEXT_DATA:
        ADD.W    #1, A0
        AND.W    #(C_DATA_SIZE-1), A0
        JNZ      WRITE_DATA
;
COMPLETE_TRANS:
        JMP      COMPLETE_TRANS
;
;=======================================================================
;       Dummy interrupt processing program
;=======================================================================
dummy:
        REIT
;
;***********************************************************************************
;
;       Setting of fixed vector
;***********************************************************************************
;
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
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User's Manual

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