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April 1st, 2010
Renesas Electronics Corporation

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M16C/Tiny Series

Operation of Serial I/O (Transmission in Clock-Synchronous Serial I/O Mode)

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table1. Operations of the checked items are described below.

Table 1. Choosed Functions

Item	Set-up		Item	Set-up	
Transfer clock source	Yes	Internal clock (f_1/f_2/f_8/f_{32})	Transmission interrupt factor	Yes	Transmission buffer empty
		External clock (CLKi pin)			Transmission complete
$\overline{CTS}$ function	Yes	$\overline{CTS}$ function enabled	Output transfer clock to multiple pins (Note 1)	Yes	Not selected
		$\overline{CTS}$ function disabled			Selected
CLK polarity	Yes	Output transmission data at the falling edge of the transfer clock	Data logic select (Note 2)	Yes	No reverse
					Reverse
		Output transmission data at the rising edge of the transfer clock	TxD, RxD I/O polarity reverse function (Note 2)	Yes	No reverse
					Reverse
Transfer format	Yes	LSB first	UART1 pin remapping function (Note 3)	Yes	UART1 pins assigned to $P6_7$ to $P6_4$
		MSB first			UART1 pins assigned to $P7_3$ to $P7_0$

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{CTS}$/RTS function can not be utilized. Set the UART1 $\overline{CTS}$/RTS disable bit to “1”.

Note 2: UART2 only

Note 3: It is possible to select it only with M16C/26A, M16C/28, and M16C/29.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

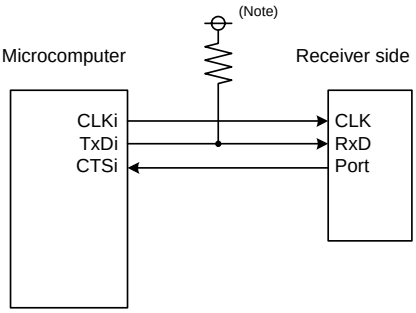
This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/26, M16C/26A, M16C/28, M16C/29 microcomputers. However, some functions may have been modified.
Refer to the User’s Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Operation of Serial I/O

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.
(2) When input to the $\overline{\text{CTSi}}$ pin goes to “L” level, transmission starts (the $\overline{\text{CTSi}}$ pin must be controlled on the reception side).
(3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to “1”. Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.
(4) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that transmission is completed. The transfer clock stops at “H” level.
(5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

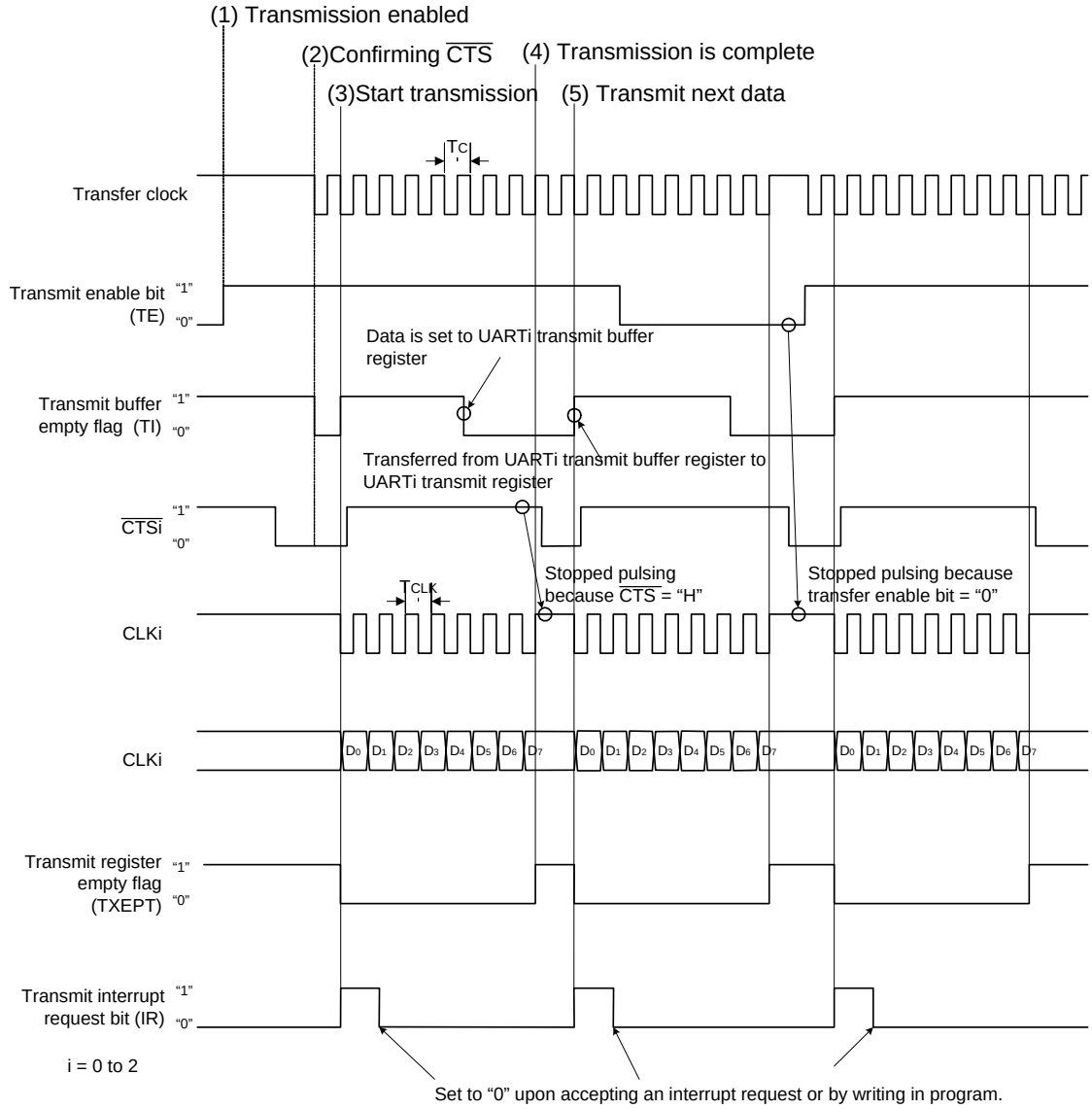
Figure 1 shows the operation timing.

Example of wiring



Note : Since TXD2 pin is N-channel open drain, this pin needs pull-up resistor (M16C/26).

Example of operation



Shown in ( ) are bit symbols.

The above timing applies to the following settings:
- Internal clock is selected.
- $\overline{\text{CTS}}$ function is selected.
- CLK polarity select bit = "0".
- Transmit interrupt cause select bit = "0".

$Tc = T_{CLK} = 2(n + 1) / fi$
fi: frequency of BRGi count source (f1, f2, f8, f32)
n: value set to BRGi

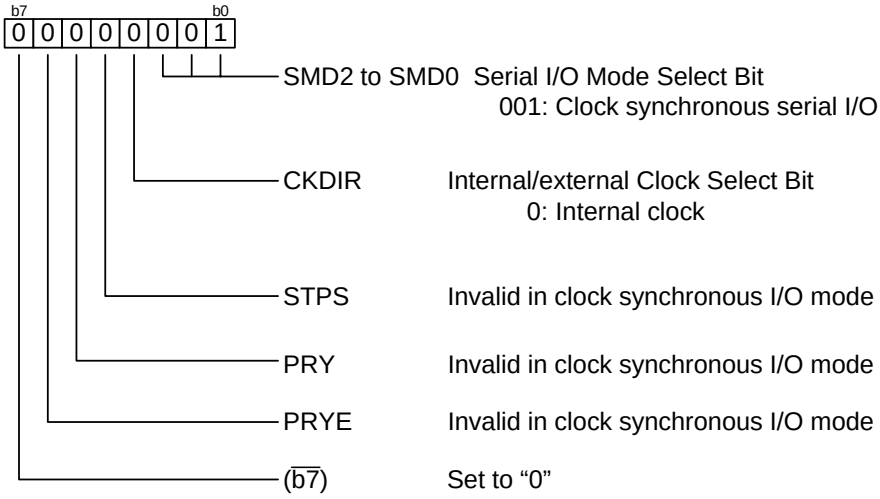
Figure 1. Operation Timing of Transmission in Clock-Synchronous Serial I/O Mode

3.1 Register Setting

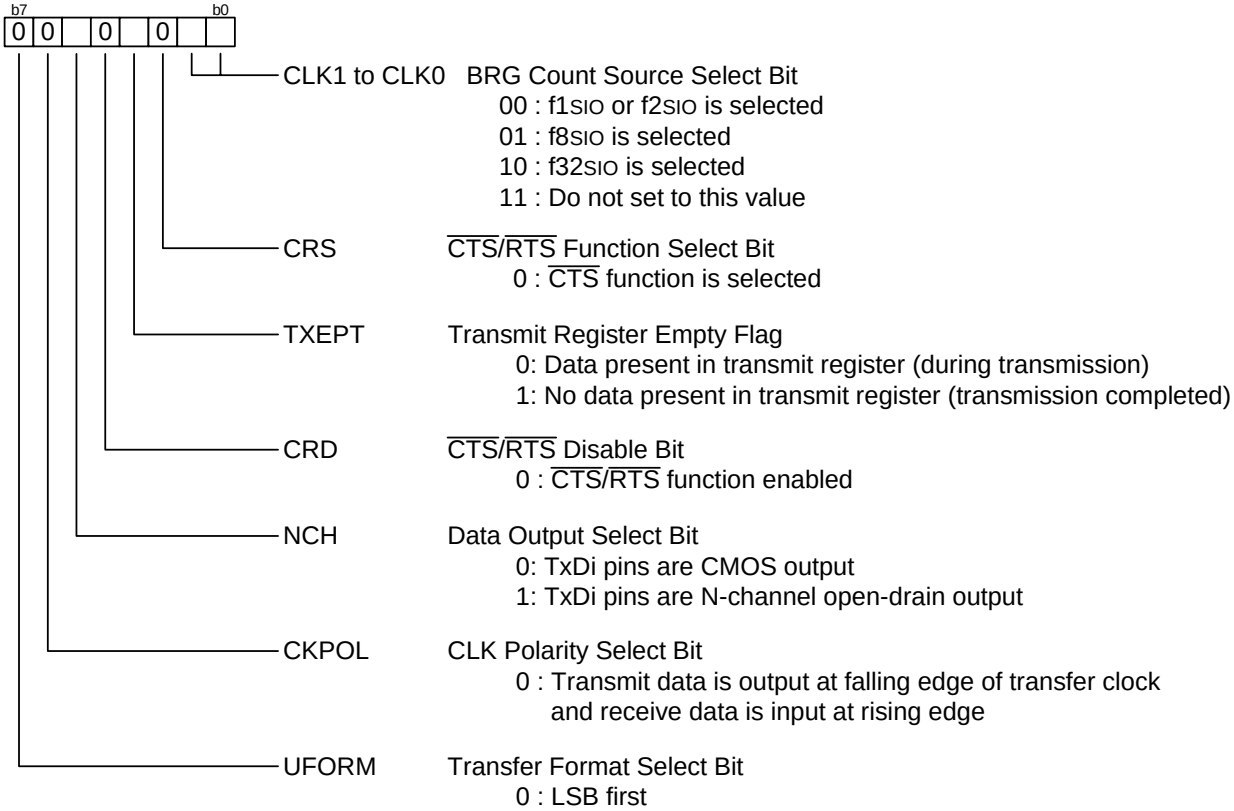
To enable the operation defined in “Section 3. Operation of timer A”, the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual.

3.1.1 UART0, 1

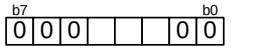
(1) Setting UARTi transmit/receive mode register (i=0, 1)



(2) Setting UARTi transmit/receive control register 0 (i=0,1)



(3) Setting UART transmit/receive control register 2



U0IRS — UART0 Transmit Interrupt Cause Select Bit
0 : Transmit buffer empty (TI = 1)

U1IRS — UART1 Transmit Interrupt Cause Select Bit
0 : Transmit buffer empty (TI = 1)

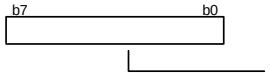
CLKMD0 — UART1 CLK/CLKS Select Bit 0
Effective when CLKMD1 = "1"

CLKMD1 — UART1 CLK/CLKS Select Bit 1
0 : CLK output is only CLK1

RCSP — Separate UART0 $\overline{CTS}/\overline{RTS}$ Bit
0 : $\overline{CTS}/\overline{RTS}$ shared pin
1 : $\overline{CTS}/\overline{RTS}$ separated ($\overline{CTS}_0$ supplied from the $P6_4$ pin)

($\overline{b7}$) — Set to "0"

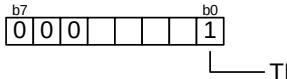
(4) Setting UARTi baud rate generation register (i=0,1)



Can be set to 00_{16} to FF_{16} (Note)

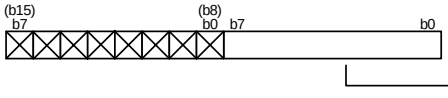
Note: Write to UARTi baud rate generation register when transmission/reception is halted.

(5) Transmission enabled (UARTi transmit/receive control register 1) (i=0,1))



TE — Transmit Enable Bit
1 : Transmission enabled

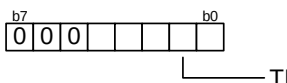
(6) Writing transmit data (UARTi transmit buffer register (i=0,1))



Setting transmission data

Start transmission When CTSi input level = "L"

(7) Checking the status of UARTi transmit buffer register (i=0,1)

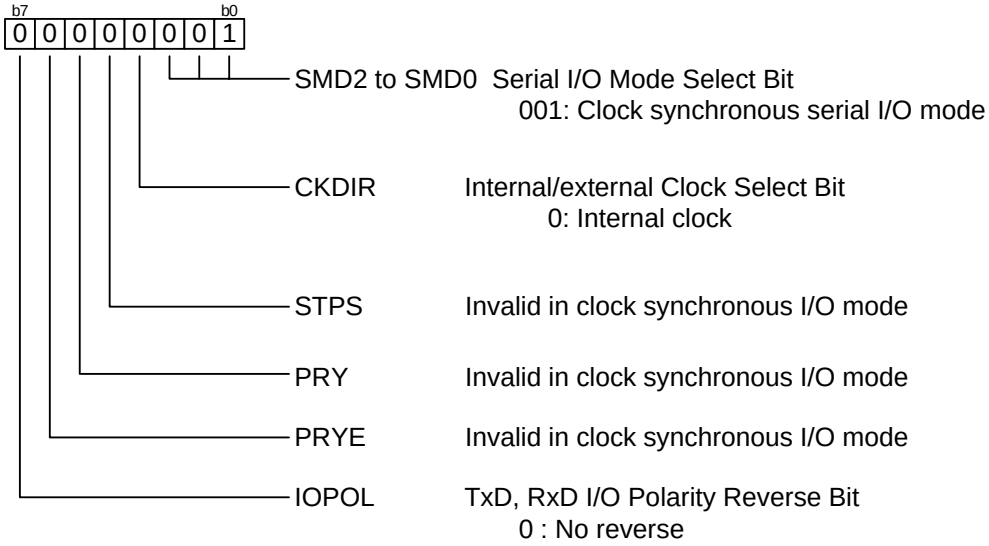


TI — Transmit Buffer Empty Flag
0 : Data present in UiTB register
1 : No data present in UiTB register

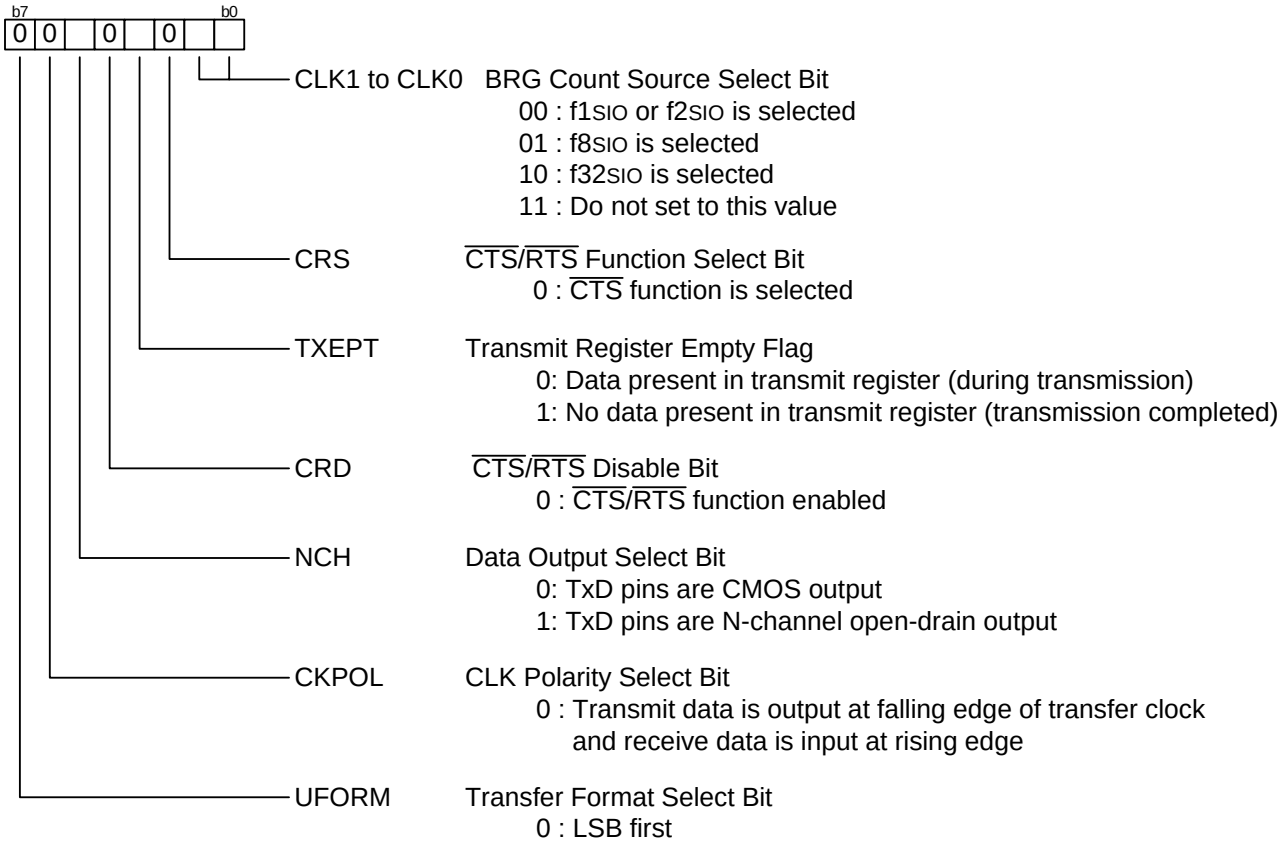
It returns to (6) when continuously transmitting.

3.1.2 UART2

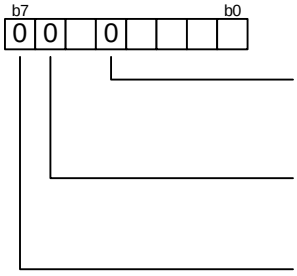
(1) Setting UART2 transmit/receive mode register



(2) Setting UART2 transmit/receive control register 0



(3) Setting UART2 transmit/receive control register 1

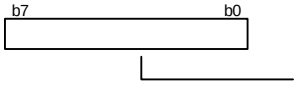


UART2 Transmit Interrupt Cause Select Bit
0 : Transmit buffer empty (TI = 1)

Data Logic Select Bit
0 : No reverse

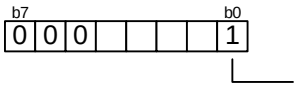
Error Signal Output Enable Bit
Set to “0” in clock synchronous serial I/O mode

(4) Setting UART2 baud rate generation register



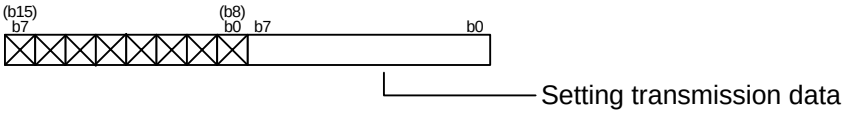
Note: Write to UART2 baud rate generation register when transmission/reception is halted.

(5) Transmission enabled (UART2 transmit/receive control register 1)



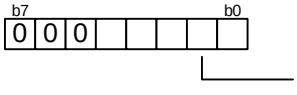
Transmit Enable Bit
1 : Transmission enabled

(6) Writing transmit data (UART2 transmit buffer register)



Start transmission When CTSi input level = “L”

(7) Checking the status of UART2 buffer register



Transmit Buffer Empty Flag
0 : Data present in U2TB register
1 : No data present in U2TB register

It returns to (6) when continuously transmitting.

4. Sample Program

4.1 UART0

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART0                         *
 *               (Clock synchronous serial I/O transfer)    *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/*************************
 *   include file        *
 *************************/
#include "sfr28.h"

/*************************
 *   Function Definition *
 *************************/

/*************************
 *   main                *
 *************************/
void main(void) {

    unsigned short   trans_data = 0;

    pd6_0 = 0;

    u0mr = 0x01; /* UART0 transmint/receive mode register setting
                 Clock synchronous serial I/O mode
                 Internal clokc select
            */

    u0c0 = 0x00; /* UART0 transmint/receive control register 0 setting
                 ~CTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    ucon = 0x00; /* UART transmint/receive control register 2 setting
             UART0 tansmit interrupt cause is selected to "Transmit buffer empty(TI=1)"
             ~CTS/~RTS shared pin
             */

    u0brg = 10-1;    /* Setting UART0 bit rate generator (1MHz @20MHz f1) */

    u0c1 = 0x01; /* UART transmint/receive control register 1 setting
                 Transmit enabled
            */

    while (1) {

        u0tb = trans_data;   /* Writing transmit data */

        while (!ti_u0c1) {   /* Check & wait the status of UART0 transmit buffer empty flag */
        }

        trans_data++;
        trans_data = 0xFF & trans_data;

    }
}
```

4.1.1 UART2

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART2                         *
 *               (Clock synchronous serial I/O transfer)    *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/***************************
 *   include file          *
 ***************************/
#include "sfr28.h"

/***************************
 *   Function Definition   *
 ***************************/

/***************************
 *   main                  *
 ***************************/
void main(void) {

    unsigned short   trans_data = 0;

    pd7_3 = 0;

    u2mr = 0x01; /* UART2 transmint/receive mode register setting
                 Clock synchronous serial I/O mode
                 Internal clokc select
            */

    u2c0 = 0x00; /* UART2 transmint/receive control register 0 setting
                 ~CTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    u2c1 = 0x00; /* UART2 transmint/receive control register 1 setting
             UART2 tansmit interrupt cause is selected to "Transmit buffer empty(TI=1)"
             ~CTS/~RTS shared pin
             */

    u2brg = 10-1;    /* Setting UART2 bit rate generator (1MHz @20MHz f1) */

    u2c1 = 0x01; /* UART transmint/receive control register 1 setting
                 Transmit enabled
            */

    while (1) {

        u2tb = trans_data;   /* Writing transmit data */

        while (!ti_u2c1) {   /* Check & wait the status of UART2 transmit buffer empty flag */
        }

        trans_data++;
        trans_data = 0xFF & trans_data;

    }
}
```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual
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		Page	Summary
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