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Renesas Electronics Corporation

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M16C/64 Group

Operation of serial I/O (transmission in clock-synchronous serial I/O mode)

1. Abstract

In transmitting data in clock-synchronous serial I/O mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up		Item	Set-up	
Transfer clock source	<input type="radio"/>	Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Transmission interrupt factor	<input type="radio"/>	Transmission buffer empty
		External clock (CLKi pin)			Transmission complete
CTS function	<input type="radio"/>	CTS function enabled	Output transfer clock to multiple pins (Note 1)	<input type="radio"/>	Not selected
		CTS function disable			Selected
CLK polarity	<input type="radio"/>	Output transmission data at the falling edge of the transfer clock	Data logic select function	<input type="radio"/>	No reverse
		Output transmission data at the rising edge of the transfer clock			Reverse
Transfer format	<input type="radio"/>	LSB first	TxD, RxD I/O polarity reverse bit	<input type="radio"/>	No reverse
		MSB first			Reverse

Note 1: This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit to “1”.

4. Operation

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register makes data transmissible status ready.

(2) When input to the $\overline{\text{CTS}}_i$ pin goes to “L” level, transmission starts (the $\overline{\text{CTS}}_i$ pin must be controlled on the reception side).

(3) In synchronization with the first falling edge of the transfer clock, transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the UARTi transmit interrupt request bit goes to “1”. Also, the first bit of the transmission data is transmitted from the TxDi pin. Then the data is transmitted bit by bit from the lower order in synchronization with the falling edges.

(4) When transmission of 1-byte data is completed, the transmit register empty flag goes to “1”, which indicates that transmission is completed. The transfer clock stops at “H” level.

(5) If the next transmission data is set in the UARTi transmit buffer register while transmission is in progress (before the eighth bit has been transmitted), the data is transmitted in succession.

(transmission in clock-synchronous serial I/O mode)

Figure 1 shows the operation timing.

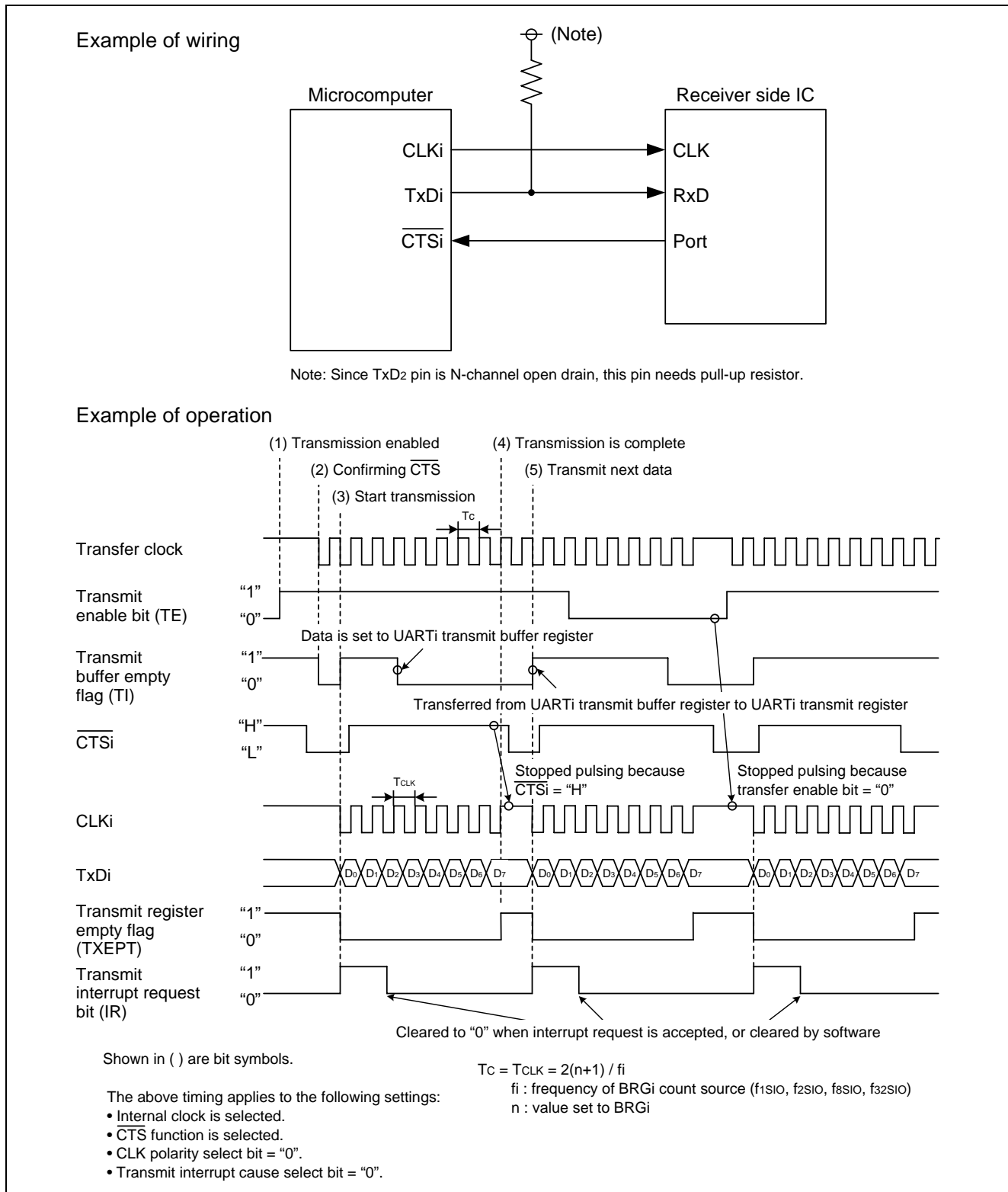
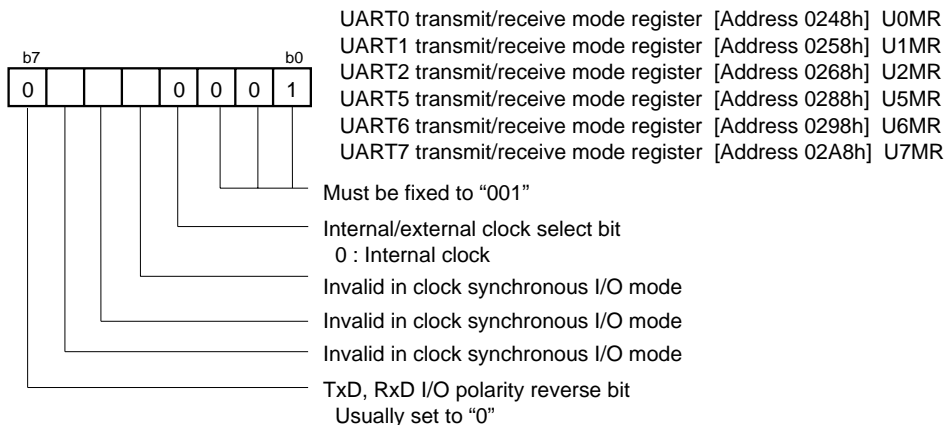


Figure 1. Operation timing of transmission in clock-synchronous serial I/O mode

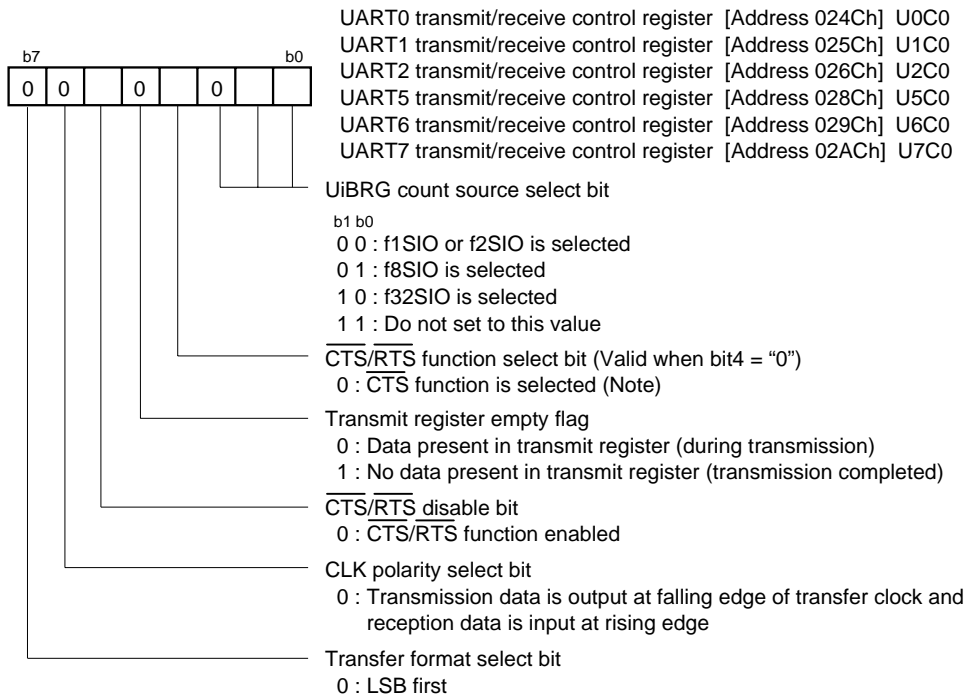
(transmission in clock-synchronous serial I/O mode)

5. Set-up procedure

Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)

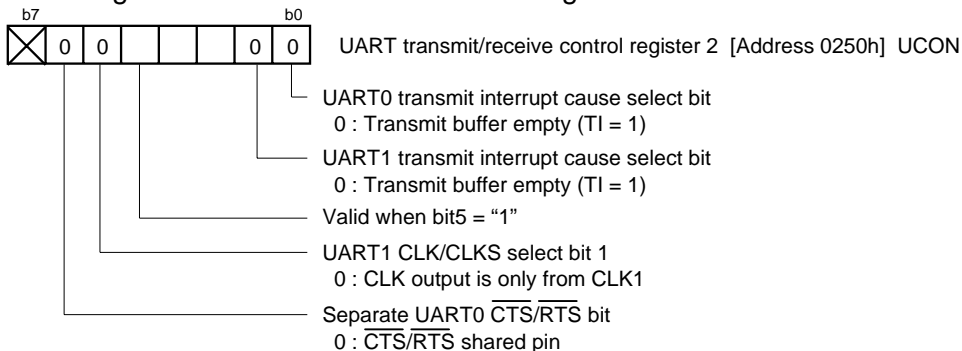


Setting UARTi transmit/receive control register (i = 0 to 2, 5 to 7)

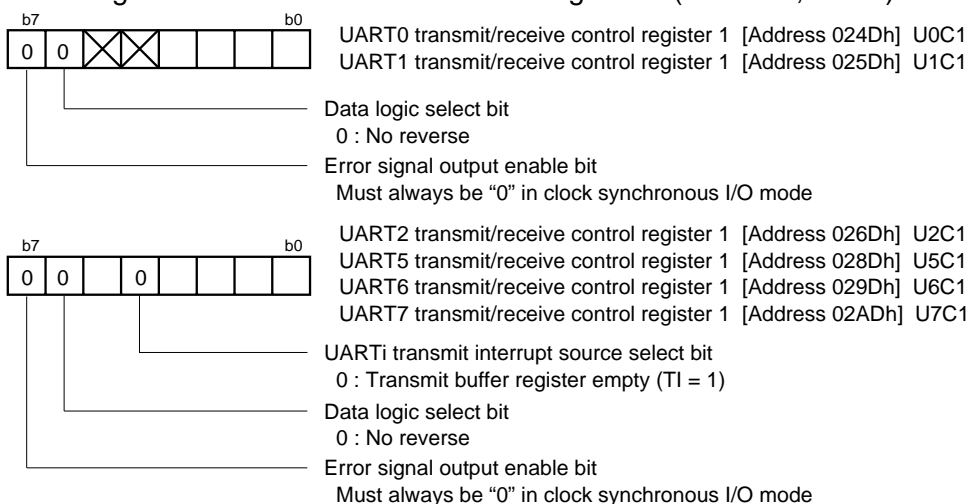


Note : Set the corresponding port direction register to "0".

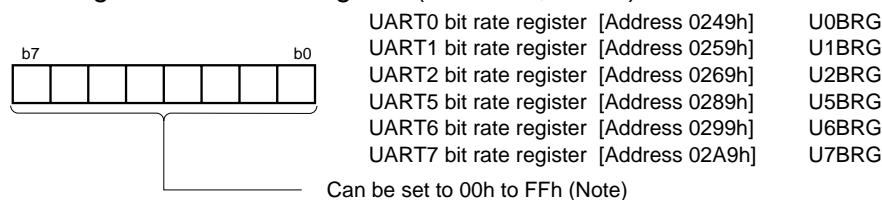
Setting UART transmit/receive control register 2



Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)



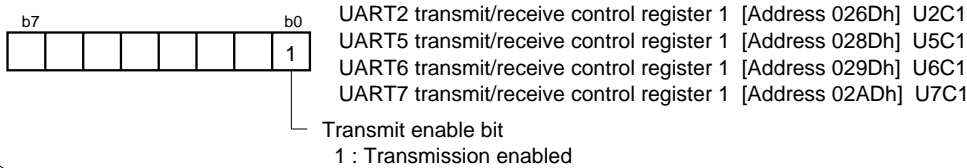
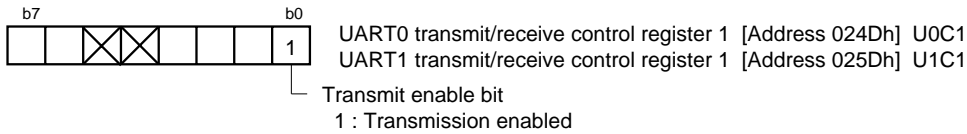
Setting UARTi bit rate register (i = 0 to 2, 5 to 7)



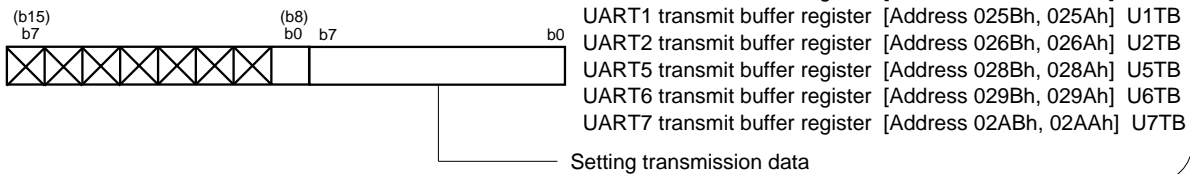
Note : Write to UARTi bit rate register when transmission/reception is halted.

(transmission in clock-synchronous serial I/O mode)

Transmission enabled



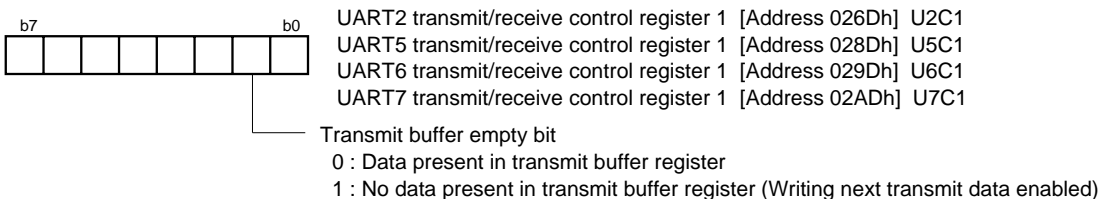
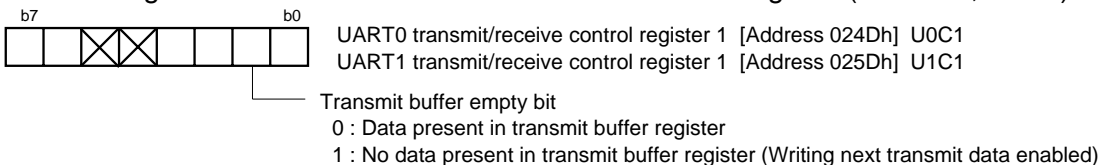
Writing transmit data



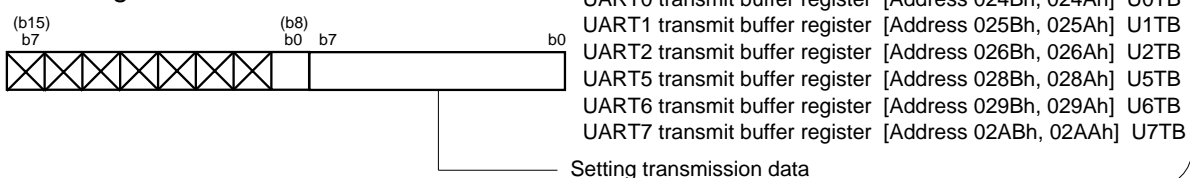
When $\overline{\text{CTS}}_i$ input level = "L"

Start transmission

Checking the status of UART $_i$ transmit/receive control register (i = 0 to 2, 5 to 7)



Writing next transmit data



Transmission is complete

6. Reference

Hardware manual

M16C/64 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

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Revision

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