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April 1st, 2010
Renesas Electronics Corporation

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M16C/Tiny Series

Operation of Serial I/O (Transmission in Clock-Asynchronous Serial I/O Mode)

1. Abstract

In transmitting data in clock-asynchronous serial I/O mode, choose functions from those listed in Table1. Operations of the checked items are described below.

Table 1. Choosed Functions

Item	Set-up		Item	Set-up	
Transfer clock source	Yes	Internal clock ($f_1/f_2/f_8/f_{32}$)	$\overline{CTS}/\overline{RTS}$ separated function	Yes	$\overline{CTS}/\overline{RTS}$ shared pin
		External clock (CLKi pin)			$\overline{CTS}/\overline{RTS}$ separated
$\overline{CTS}$ function	Yes	$\overline{CTS}$ function enabled	Data logic select (Note 2)	Yes	No reverse
		$\overline{CTS}$ function disabled			Reverse
Transmission interrupt factor	Yes	Transmission buffer empty	TxD, RxD I/O polarity reverse function (Note 2)	Yes	No reverse
		Transmission complete			Reverse

Note 1: UART0 only
Note 2: UART2 only.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/26, M16C/26A, M16C/28, M16C/29 Group

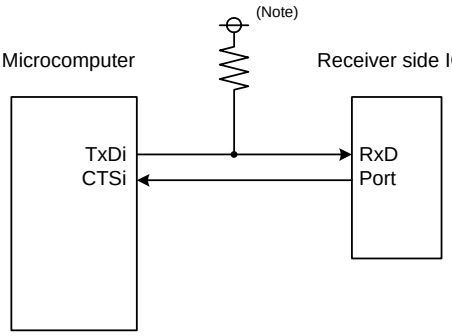
This program can also be used when operating other microcomputers within the M16C family, provided they have the same SFR (Special Function Registers) as the M16C/26, M16C/26A, M16C/28, M16C/29 microcomputers. However, some functions may have been modified.
Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Operation of Serial I/O

(1) Setting the transmit enable bit to “1” and writing transmission data to the UARTi transmit buffer register readies the data transmissible status.
(2) When input to the $\overline{CTSi}$ pin goes to “L”, transmission starts (the $\overline{CTSi}$ pin needs to be controlled on the reception side).
(3) Transmission data held in the UARTi transmit buffer register is transmitted to the UARTi transmit register. At this time, the first bit (the start bit) of the transmission data is transmitted from the TxDi pin. Then, data is transmitted, bit by bit, in sequence: LSB, ····, MSB, parity bit, and stop bit(s).
(4) When the stop bit(s) is (are) transmitted, the transmit register empty flag goes to “1”, which indicates that transmission is completed. At this time, the UARTi transmit interrupt request bit goes to “1”. The transfer clock stops at “H” level.
(5) If the transmission condition of the next data is ready when transmission is completed, a start bit is generated following to stop bit(s), and the next data is transmitted.

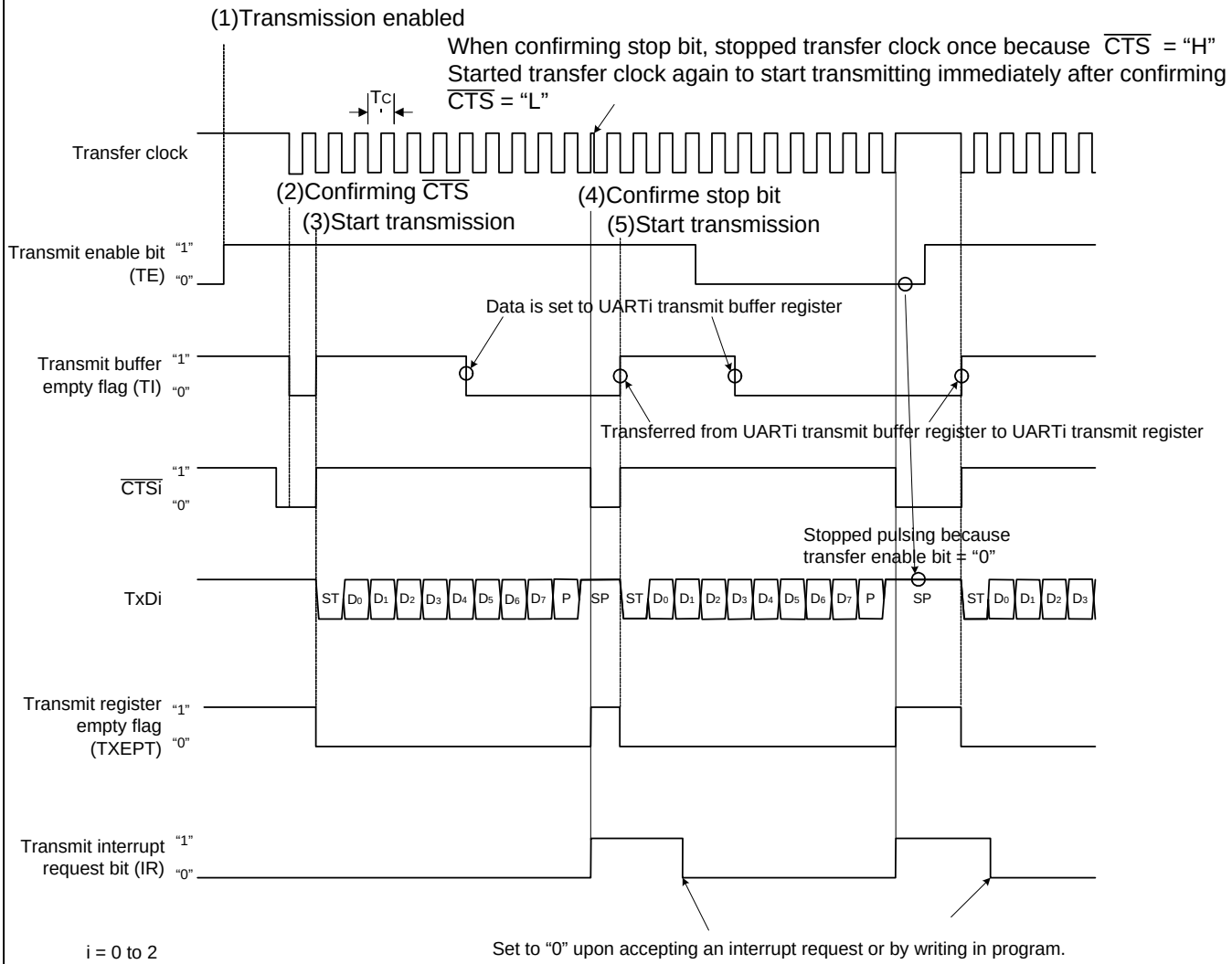
Figure 1 shows the operation timing.

Example of wiring



Note : Since TXD2 pin is N-channel open drain, this pin needs pull-up resistor. (M16C/26)

Example of operation



i = 0 to 2

Shown in ( ) are bit symbols.
The above timing applies to the following settings:

- Parity is enabled.
- One stop bit.
- CTS function is selected.
- Transmit interrupt cause select bit = "1".

$T_C = 16(n+1)/fi$ or $16(n+1)/f_{EXT}$
fi : frequency of BRGi count source (f_1, f_2, f_8, f_{32})
f_{EXT} : frequency of BRGi count source (external clock)
n : value set to BRGi

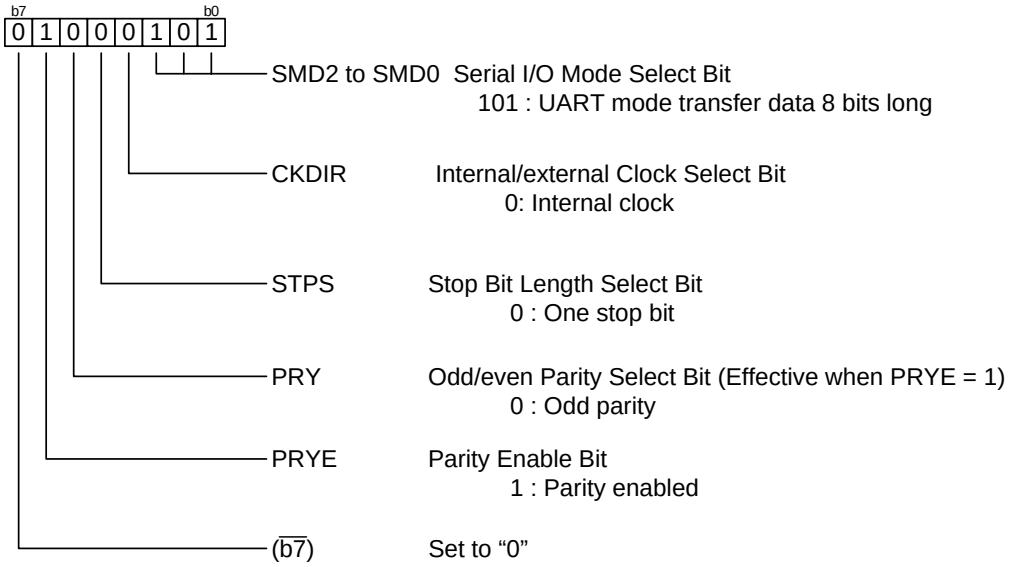
Figure 1. Operation Timing of Transmission in Clock-asynchronous Serial I/O Mode

3.1 Register Setting

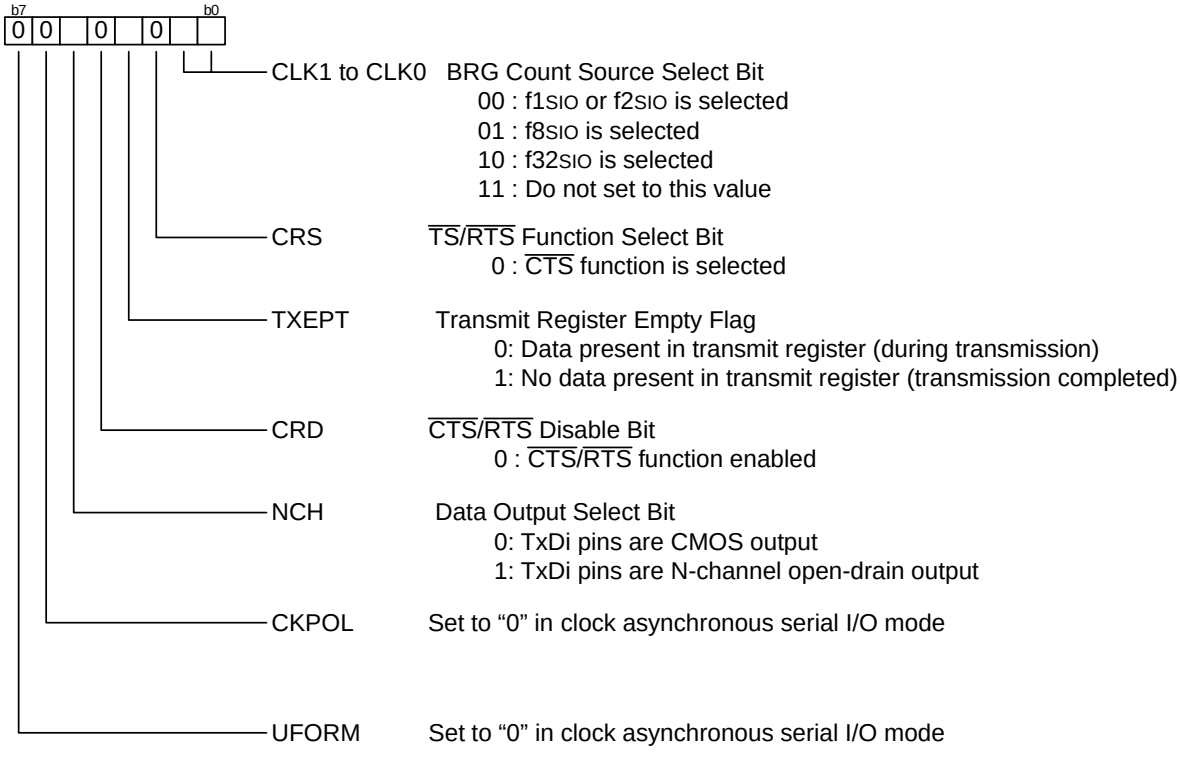
To enable the operation defined in “Section 3. Operation of timer A”, the following register settings must be taken place step by step. For detail configuration of each register, please refer to M16C/26 Group hardware manual, M16C/26A Group hardware manual, M16C/28 Group hardware manual, M16C/29 Group hardware manual.

3.1.1 UART0, 1

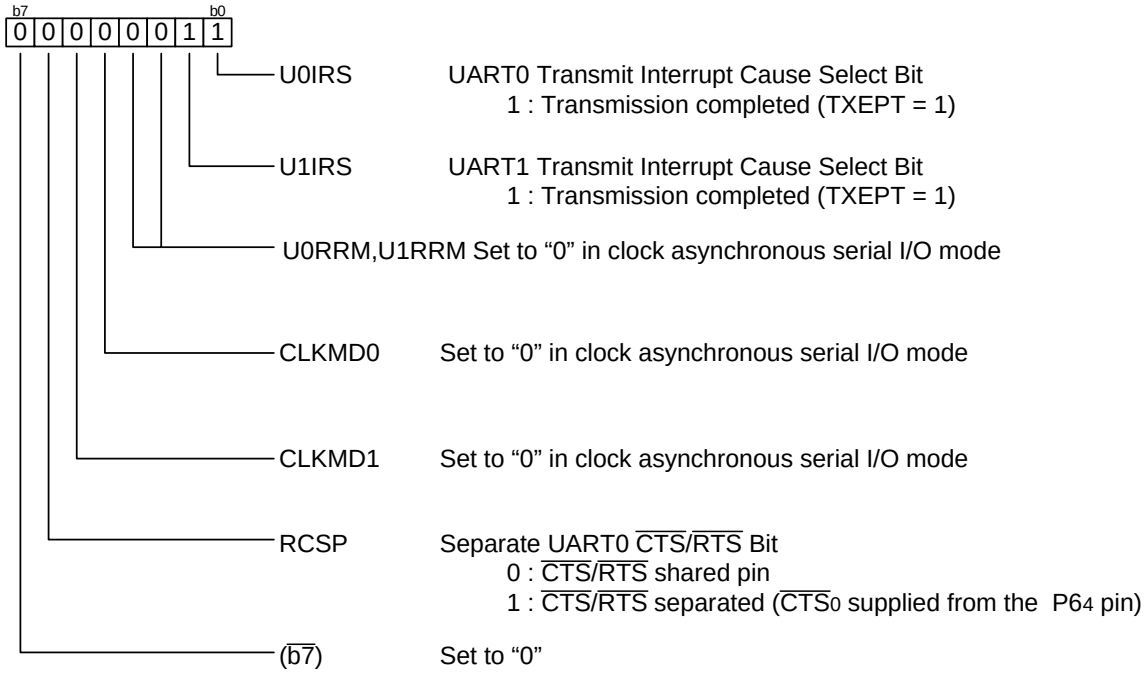
(1) Setting UARTi transmit/receive mode register (i=0, 1)



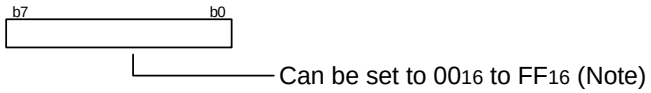
(2) Setting UARTi transmit/receive control register 0 (i=0,1)



(3) Setting UART transmit/receive control register 2



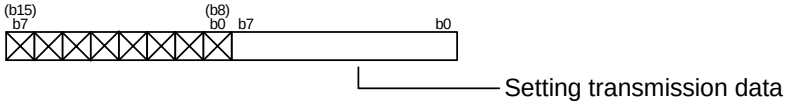
(4) Setting UARTi baud rate generation register (i=0,1)



Note: Write to UARTi baud rate generation register when transmission/reception is halted.

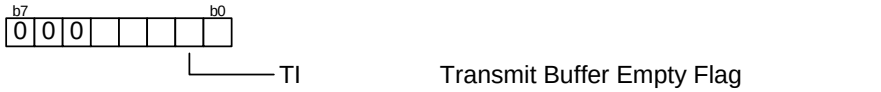
(5) Transmission enabled (UARTi transmit/receive control register 1) (i=0,1))

(6) Writing transmit data (UARTi transmit buffer register (i=0,1))



Start transmission When CTSi input level = “L”

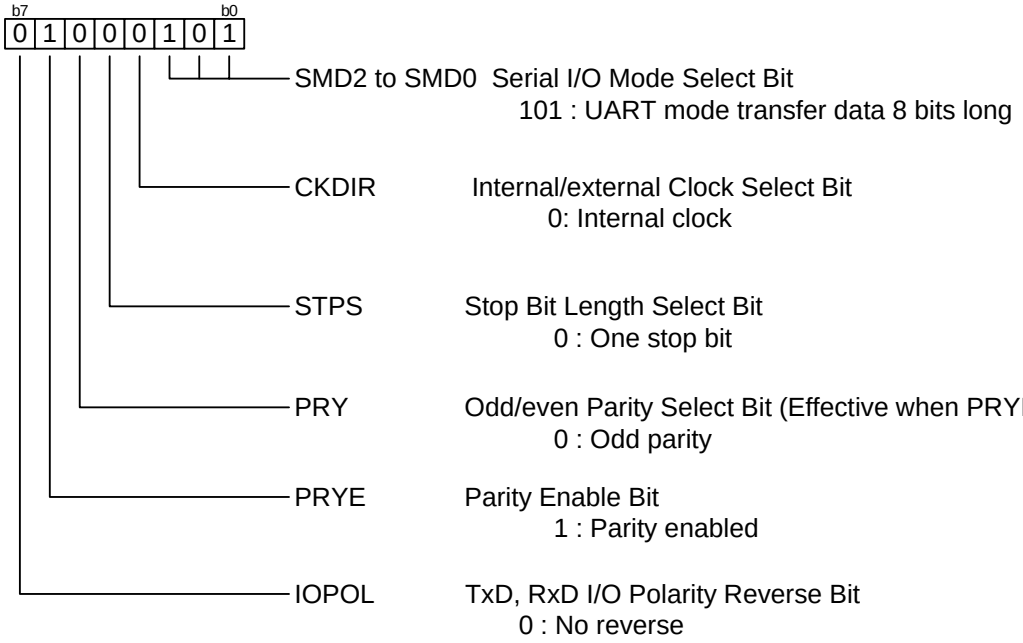
(7) Checking the status of UARTi transmit buffer register (i=0,1)



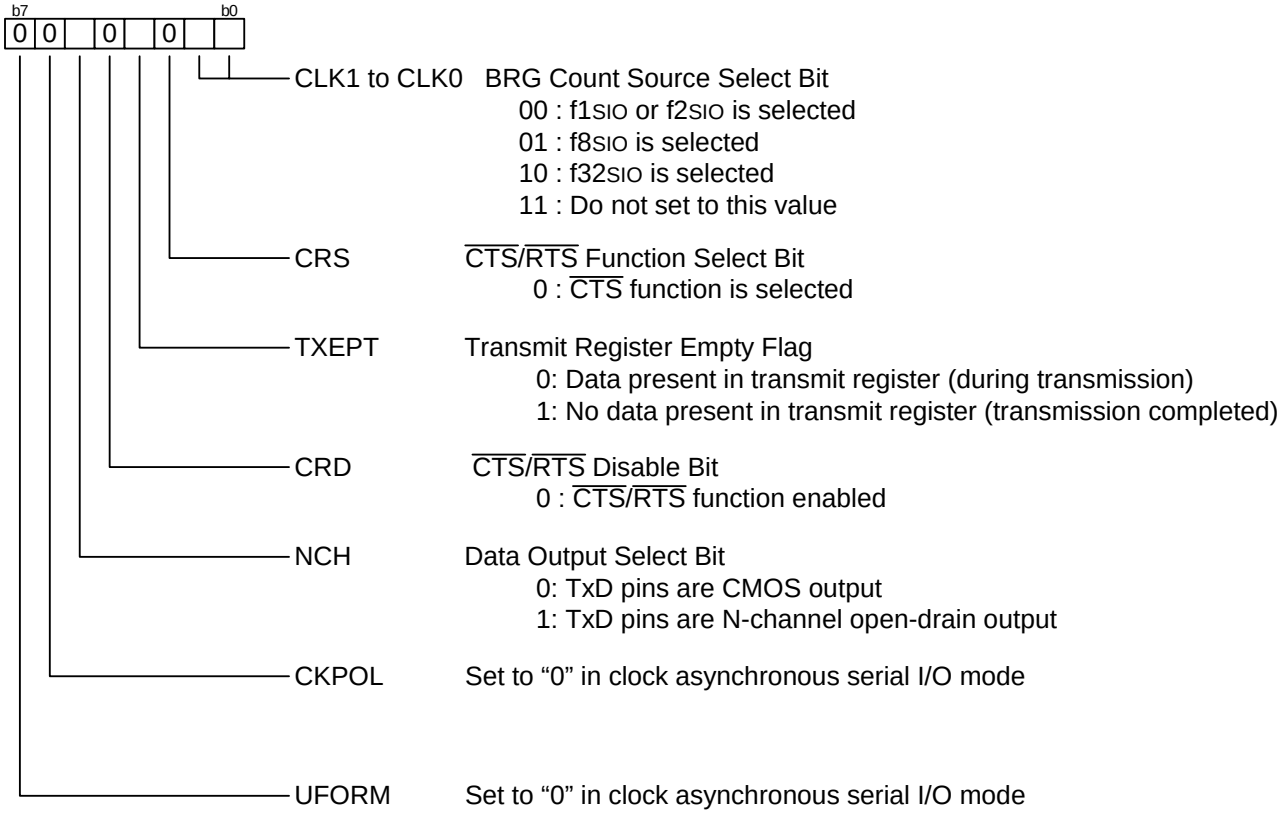
It returns to (6) when continuously transmitting.

3.1.2 UART2

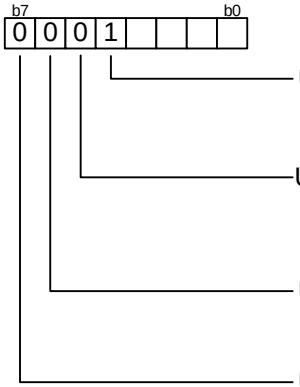
(1) Setting UART2 transmit/receive mode register



(2) Setting UART2 transmit/receive control register 0



(3) Setting UART2 transmit/receive control register 1



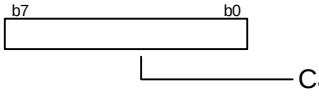
UART2 Transmit Interrupt Cause Select Bit
1 : Transmit is completed (TXEPT = 1)

Set to “0” in clock asynchronous serial I/O mode

Data Logic Select Bit
0 : No reverse

Error Signal Output Enable Bit
Set to “0” in clock asynchronous serial I/O mode

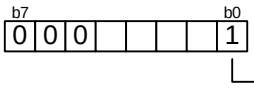
(4) Setting UART2 baud rate generation register



Can be set to 00_{16} to FF_{16} (Note)

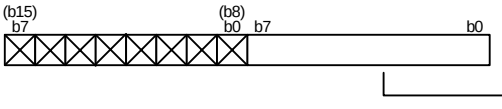
Note: Write to UART2 baud rate generation register when transmission/reception is halted.

(5) Transmission enabled (UART2 transmit/receive control register 1)



Transmit Enable Bit
1 : Transmission enabled

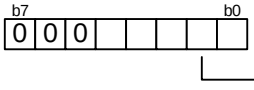
(6) Writing transmit data (UART2 transmit buffer register)



Setting transmission data

Start transmission When CTS2 input level = “L”

(7) Checking the status of UART2 buffer register



Transmit Buffer Empty Flag
0 : Data present in U2TB register
1 : No data present in U2TB register

It returns to (6) when continuously transmitting.

4. Sample Program

4.1 UART0

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART0                         *
 *                (Clock asynchronous serial I/O transfer)  *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/*************************
 *   include file        *
 *************************/
#include "sfr28.h"

/*************************
 *   Function Definition *
 *************************/

/*************************
 *   main                *
 *************************/
void main(void) {

    unsigned short   trans_data = 0;

    u0mr = 0x45; /* UART0 transmint/receive mode register setting
                 UART mode transfer data 8 bits long
                 Internal clokc select
                 One stop bit
                 Parity enabled (odd parity)
            */

    pd6_0 = 0;

    u0c0 = 0x00; /* UART0 transmint/receive control register 0 setting
                 ~CTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    ucon = 0x01; /* UART transmint/receive control register 2 setting
                 UART0 tansmit interrupt cause is selected to "Transmission comoleted(TXEPT=1)"
                 ~CTS/~RTS shared pin
            */

    u0brg = 129; /* Setting UART0 bit rate generator (Approx 9600bps @20MHz f1) */

    u0c1 = 0x01; /* UART transmint/receive control register 1 setting
                 Transmit enabled
            */

    while (1) {

        u0tb = trans_data;   /* Writing transmit data */

        while (!ti_u0c1) {   /* Check & wait the status of UART0 transmit buffer empty flag */
        }

        trans_data++;
        trans_data = 0xFF & trans_data;

    }
}
```

4.2 UART2

```
/************************************************************
 *                                                          *
 *   FILE NAME :                                            *
 *   CPU       : M16C/Tiny series                           *
 *   Function  : Operation of UART2                         *
 *                (Clock asynchronous serial I/O transfer)  *
 *   Version   : 1.00                                       *
 *                                                          *
 *   Copyright (C)2004, Renesas Technology Corp.            *
 *   Copyright (C)2004, Renesas Solutions Corp.             *
 *                                                          *
 ************************************************************/
/***************************
 *   include file          *
 ***************************/
#include "sfr28.h"

/***************************
 *   Function Definition   *
 ***************************/

/***************************
 *   main                  *
 ***************************/
void main(void) {

    unsigned short   trans_data = 0;

    u2mr = 0x45; /* UART2 transmint/receive mode register setting
                 UART mode transfer data 8 bits long
                 Internal clokc select
                 One stop bit
                 Parity enabled (odd parity)
            */

    pd7_3 = 0;

    u2c0 = 0x00; /* UART2 transmint/receive control register 0 setting
                 ~CTS function select
                 ~CTS/~RTS function enabled
                 TxD0 pin is CMOS output
                 Transmission data is output at falling edge of transfer
                 clock and reception data is input at rising edge
                 LSB first
            */

    u2c1 = 0x10; /* UART transmint/receive control register 1 setting
                 UART2 tansmit interrupt cause is selected to "Transmission comoleted(TXEPT=1)"
            */

    u2brg = 129; /* Setting UART0 bit rate generator (Approx 9600bps @20MHz f1) */

    u2c1 = 0x11; /* UART transmint/receive control register 1 setting
                 UART2 tansmit interrupt cause is selected to "Transmission comoleted(TXEPT=1)"
                 Transmit enabled
            */

    while (1) {

        u2tb = trans_data;   /* Writing transmit data */

        while (!ti_u2c1) {   /* Check & wait the status of UART0 transmit buffer empty flag */
        }

        trans_data++;
        trans_data = 0xFF & trans_data;

    }
}
```

5. Reference

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Hardware Manual

M16C/26, M16C/26A, M16C/28, M16C/29 Group Hardware Manual
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Rev.	Date	Description	
		Page	Summary
1.10	2005.05.30	-	First edition issued

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