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April 1st, 2010
Renesas Electronics Corporation

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M16C/62A Group

Operation of Serial I/O (reception used for SIM interface)

1.0 Abstract

In receiving data in UART mode (used for SIM interface), choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Choosed functions

Item	Set-up	
Transfer data format	O	Direct format
		Inverse format

2.0 Introduction

Operation (1) Setting the transmit enable bit and receive enable bit to “1” readies data-receivable status.

(2) When the first bit (the start bit) of reception data is received from the RxD2 pin, data is received, bit by bit, in sequence: LSB, ····, MSB, and stop bit(s).

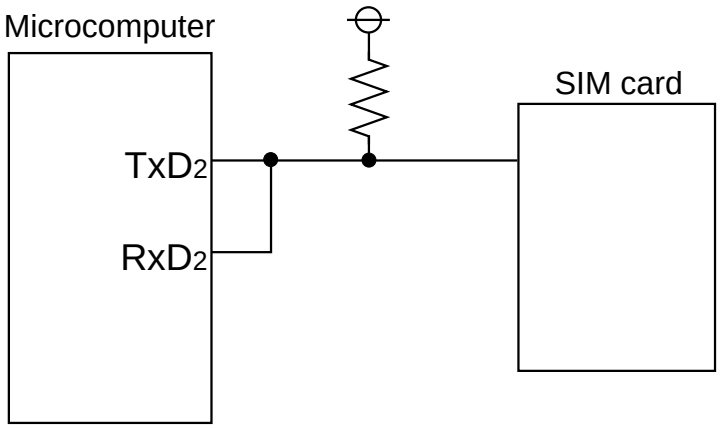
(3) When the stop bit(s) is (are) received, the content of the UART2 receive register is transmitted to the UART2 receive buffer register.
At this time, the receive complete flag goes to “1” to indicate that the reception is completed, the UART2 receive interrupt request bit goes to “1”, and output from the $\overline{RTS}$ pin goes to “H” level.

(4) The receive complete flag goes to “0” when the lower-order byte of the UART2 buffer register is read.

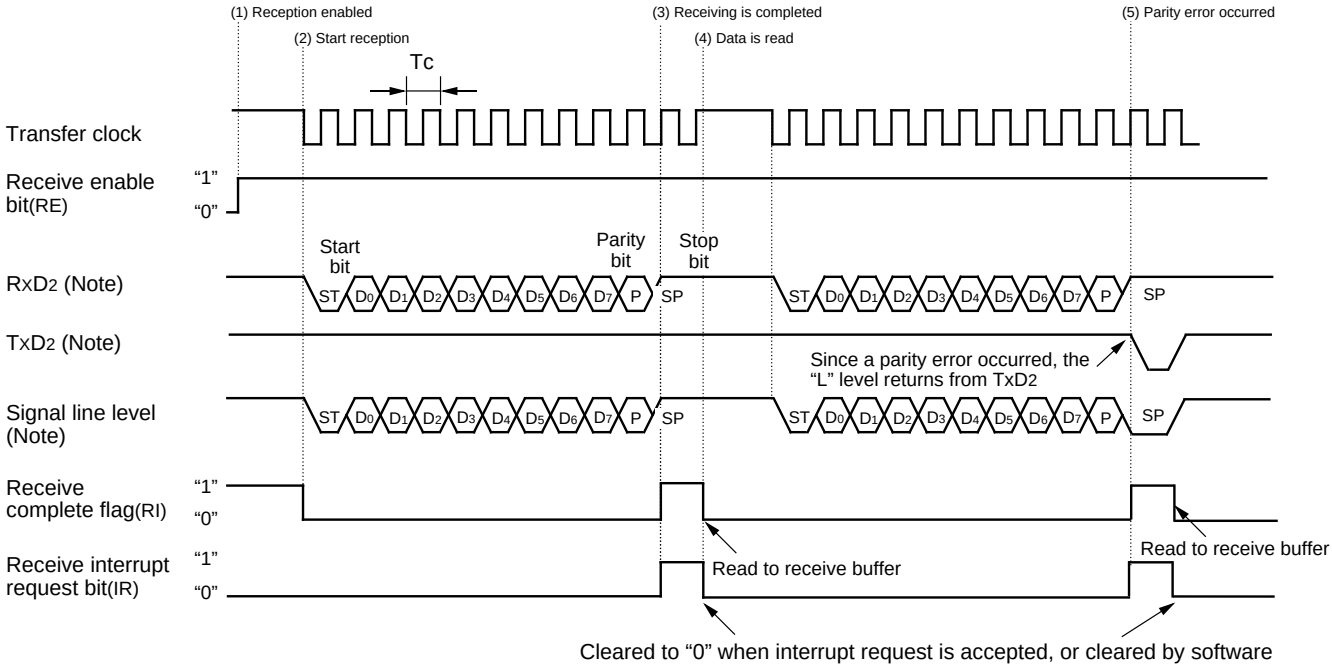
(5) When the parity error is occurred, TxD2 pin goes to “L” level.

Figure 1 shows the operation timing

Example of wiring



Example of operation



Shown in ( ) are bit symbols.

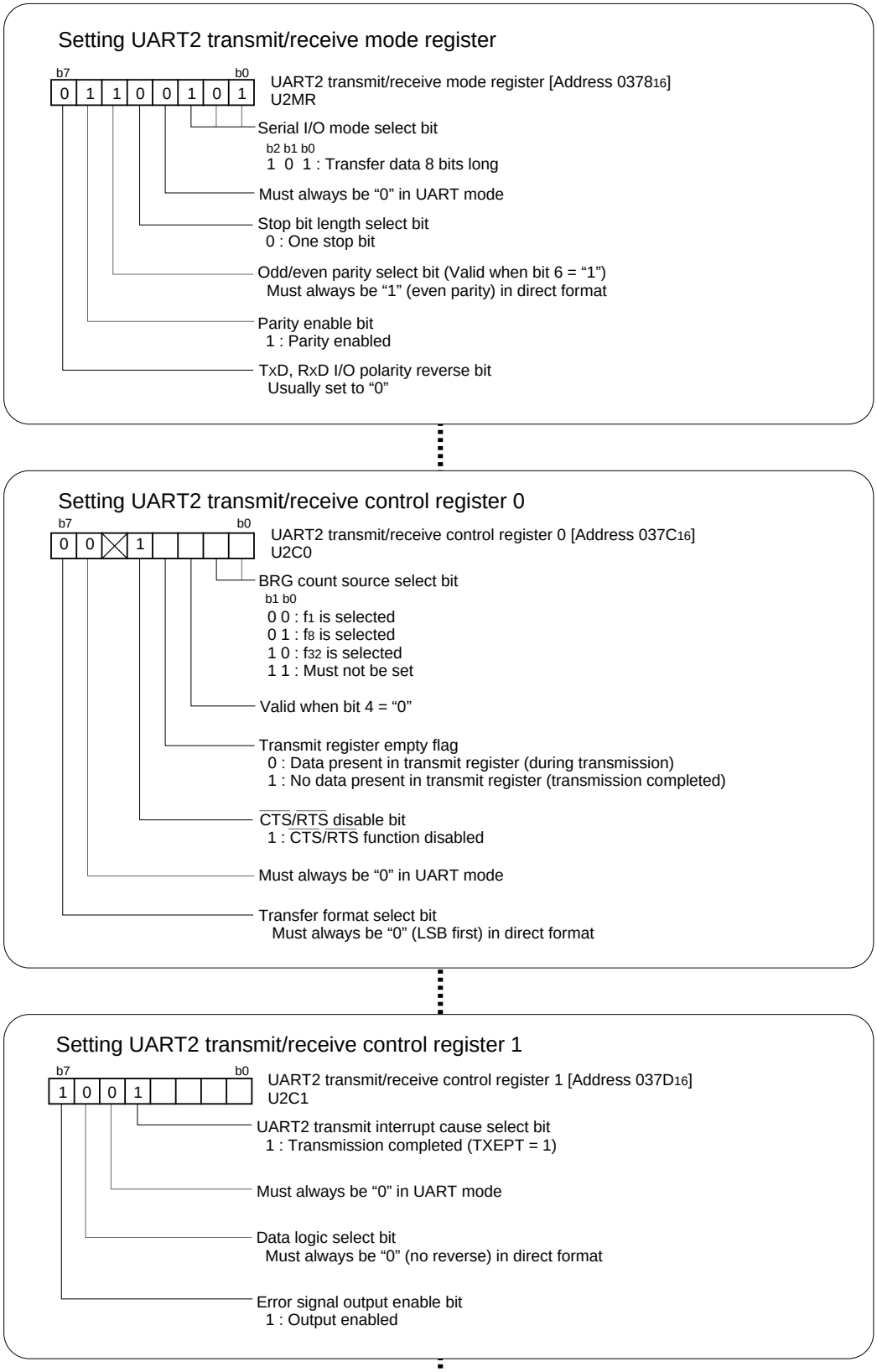
The above timing applies to the following settings :
- Parity is enabled.
- One stop bit.
- Transmit interrupt cause select bit = "1".

Tc = 16 (n + 1) / fi
fi : frequency of BRG2 count source (f_1, f_8, f_{32})
n : value set to BRG2

Note: TxD2 and RxD2 are connected in the manner of wired OR as shown in the connection diagram. So TxD2 and RxD2 ought to become the same signal from the logical standpoint, but the output signals turn complex, so they are shown separately. Also, the signal level resulting from connecting TxD2 and RxD2 is shown as a signal line level.

Figure 1. Operation timing of reception in UART mode (used for SIM interface)

3.0 Set-up procedure



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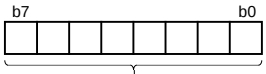
Setting UART2 bit rate generator

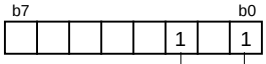


UART2 bit rate generator [Address 0379$_{16}$]
U2BRG

Can be set to 00$_{16}$ to FF$_{16}$ (Note)

Note: Write to UART2 bit rate generator when transmission/reception is halted.

Transmit enabled



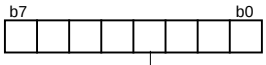
UART2 transmit/receive control register 1 [Address 037D$_{16}$]
U2C1

Transmit enable bit
1 : Transmission enabled

Receive enable bit
1 : Reception enabled

Start reception

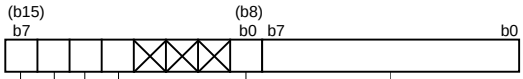
Checking completion of reception



UART2 transmit/receive control register 1 [Address 037D$_{16}$]
U2C1

Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register

Checking error



UART2 receive buffer register [Address 037F$_{16}$, 037E$_{16}$]
U2RB

Receive data

Overrun error flag
0 : No overrun error
1 : Overrun error found

Framing error flag
0 : No framing error
1 : Framing error found

Parity error flag
0 : No parity error
1 : Parity error found

Error sum flag
0 : No error
1 : Error found

Processing after reading out reception data

4.0 Programming Code

```
;******************************************************************************
;
;   M16C/62A Program Collection
;
;   FILE NAME : rjj05b0051_src.a30
;   CPU       : M16C/62A Group
;   FUNCTION  : Operation of Serial I/O
;               (reception used for SIM interface)
;   HISTORY   : 2003.05.16  Ver 1.00
;
;   Copyright(C)2003, Renesas Technology Corp.
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;   All rights reserved.
;
;******************************************************************************
;******************************************************************************
;       Include
;******************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr62a.inc      ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;******************************************************************************
;       Symbol definition
;******************************************************************************
ROM_TOP         .EQU    0F8000H     ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFDCH     ;Start address of fixed vector
;
;******************************************************************************
;       Program area
;******************************************************************************
;=============================================================================
;       Start up
;=============================================================================
        .SECTION    PROGRAM, CODE   ;Declares section name and section type
        .ORG        ROM_TOP         ;Declares start address
RESET:
        MOV.B    #03H, prcr         ;Removes protect
                                    ;Set processor mode registers 0 and 1
        MOV.B    #00000000B, pm0    ; Single-chip mode
        MOV.B    #00000000B, pm1    ; No expansion, No wait
                                    ;Set system clock control registers 0 and 1
        MOV.B    #00001000B, cm0    ; Xcin-Xcout High
        MOV.B    #00100000B, cm1    ; Xin-Xout High, Main clock is No divison
        MOV.B    #00H, prcr         ;Protects all registers
;
```

```
;=============================================================================
;       Serial I/O (reception used for SIM interface)
;=============================================================================
        MOV.B    #01100101B, u2mr  ;Setting UART2 transmit/receive mode register
;                 |||||+++---------;Serial I/O mode select bit (101:Transfer data 8 bits long)
;                 ||||+------------;Must always be "0" in UART mode
;                 |||+-------------;Stop bit length select bit (0:One stop bit)
;                 ||+--------------;Odd/even parity select bit (Valid when bit 6 = "1")
;                 ||                Must be "1"(even parity) in direct format
;                 |+---------------;Parity enable bit (1:Parity enabled)
;                 +----------------;TxD,RxD I/O polarity reverse bit (Usually set to "0")
        MOV.B    #00010000B, u2c0  ;Setting UART2 transmit/receive control register 0
;                 || |||++---------;BRG count source select bit (00:f1 is selected)
;                 || ||+-----------;CTS/RTS function select bit (Valid when bit 4="0")
;                 || |+------------;Transmit register empty flag
;                 || +-------------;CTS/RTS function disabled
;                 |+---------------;Must always be "0" in UART mode
;                 +----------------;Must be "0" (LSB first) in direct format
        MOV.B    #10010000B, u2c1  ;Setting UART2 transmit/receive control register 1
;                 |||+-------------;UART2 transmit interrupt cause select bit
;                 |||              ;(1:Transmission completed(TXEPT=1))
;                 ||+--------------;Must always be "0" in UART mode
;                 |+---------------;Data logic select bit
;                 |                 Must always be "0" (no reverse) in direct format
;                 +----------------;Error signal output enabled bit (1:Output enabled)
        MOV.B    #92, u2brg        ;Setting UART2 bit rate generator
        MOV.B    #10010101B, u2c1  ;Transmit enabled
;                      | +---------;Transmit enable bit (1:Transmission enabled)
;                      +-----------;Receive enable bit (1:Reception enabled)
;
;=============================================================================
;       Main program
;=============================================================================
WAIT_RECEIVE:
        BTST     ri_u2c1           ;Checking completion of reception
        JNC      WAIT_RECEIVE
;
CHK_ERR:
        ; Reading out error information and received data to R0 register
        ; (ex)
        MOV.W    u2rb, R0
        ; Check error (ex. Check error sum flag)
        BTST     15, R0
        JC       ERR_REC
;
        ; No error
        ; Processing after reading out reception data
        JMP      WAIT_RECEIVE
;=============================================================================
;       Error found
;=============================================================================
ERR_REC:
        NOP
        JMP      ERR_REC
;
```

```
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*******************************************************************************
;       Setting of fixed vector
;*******************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction interrupt vector
        .LWORD    dummy    ;Overflow (INT0 instruction) interrupt vector
        .LWORD    dummy    ;BRK instruction interrupt vector
        .LWORD    dummy    ;Address match interrupt vector
        .LWORD    dummy    ;Single-step interrupt vector
        .LWORD    dummy    ;Watchdog timer interrupt vector
        .LWORD    dummy    ;DBC interrupt vector
        .LWORD    dummy    ;NMI interrupt vector
        .LWORD    RESET    ;Sets reset vector
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

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Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/62A group Rev. C.1
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User's Manual

M16C/62A group Rev. 1.0
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