M16C/64C Group, M16C/65C Group

Providing a Timer Clock Independent of the CPU Clock

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Abstract

When using the M16C/64A or M16C/65 Group, switching the CPU clock from PLL clock to the main clock, or from the main clock to PLL clock, the clock source of peripheral function clock f1 changes. Therefore when f1 is used as the count source, the MCU cannot hold a fixed period.
The M16C/64C and M16C/65C Groups have the timer clock source select function which can provide the main clock as the timer clock source. With this function, the timer clock source is not changed when the CPU clock is switched. Therefore a fixed period is held.
This application note describes how to provide a timer clock independent of the CPU clock using the timer clock source select function in the M16C/65C.

Products

MCUs: M16C/64C Group, M16C/65C Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Transition between PLL operating mode and wait mode is repeated. When transitioning between PLL operating mode and wait mode, select the main clock as the timer clock source by the timer clock source select function, so the timer cycle remains unchanged. To exit wait mode, use timer A0 timer mode to generate interrupts in 100 ms periods. After exiting wait mode, enter PLL operating mode from high-speed or medium-speed mode, and invert output from a port every 10 times the timer A0 interrupt occurs (1 second). Enter high-speed or medium-speed mode from PLL operating mode, then enter wait mode from high-speed or medium-speed mode.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 shows dependence between the CPU clock and timer count source when using and not using the timer clock source select function.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer A (timer A0)	Generate interrupts every 100 ms, and exit wait mode.

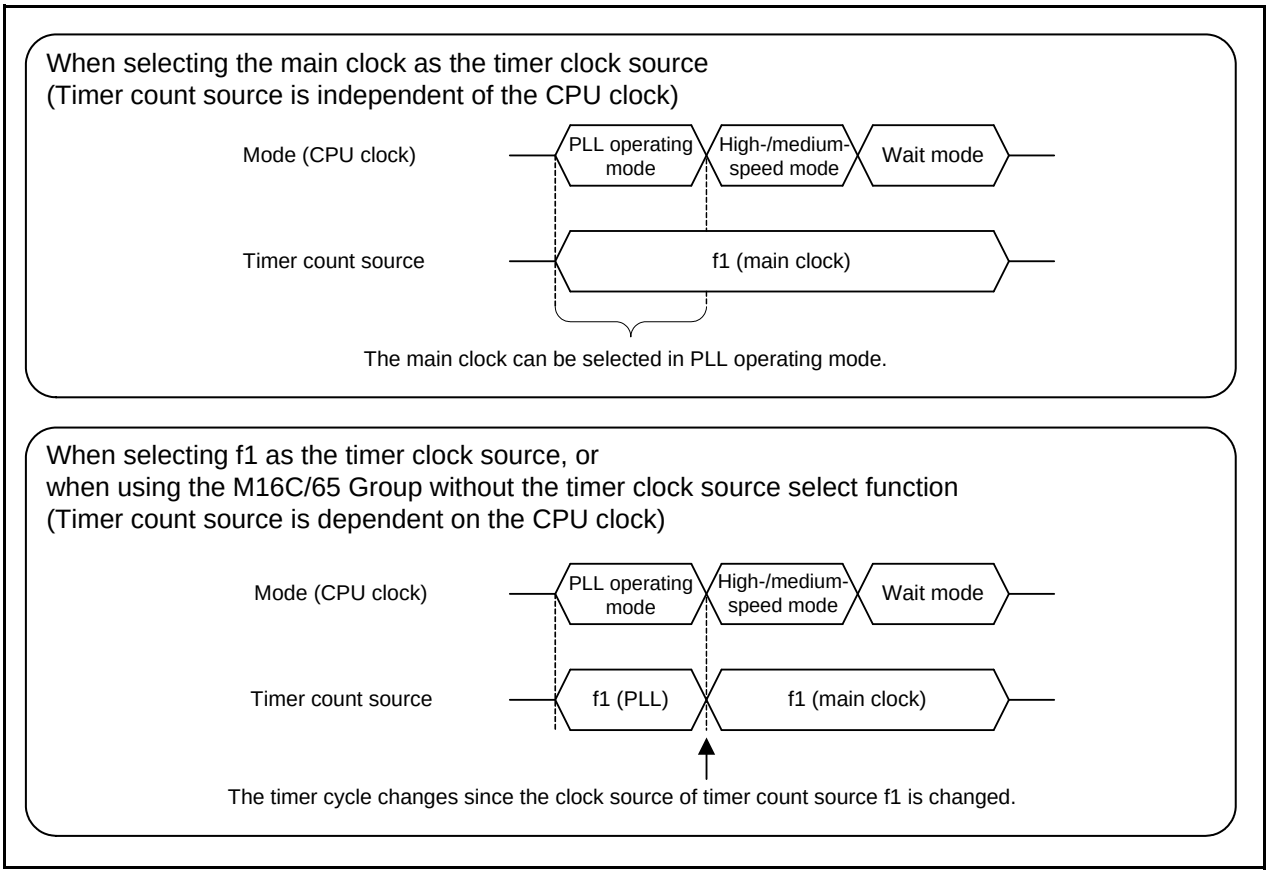

Figure 1.1 Dependence Between the CPU Clock and Timer Count Source

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	M16C/65C Group
Operating frequencies	• XIN clock: 6 MHz • CPU clock: 24 MHz (PLL clock: divided by 2, multiplied by 8)
Operating voltage	5 V (available between 2.7 to 5.5 V)
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09
C compiler	Renesas Electronics Corporation M16C Series/R8C Family Compiler V.5.45 Release 01
	Compile option -c -finfo -dir "$(CONFIGDIR)" The default setting is used in the integrated development environment.
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Peripheral Function

This chapter provides supplementary information on the timer clock source select function. Refer to the User's Manual: Hardware for basic information on this function.

3.1 Timer Clock Source Select Function

By adding the timer clock source select function to the M16C/64C and M16C/65C Groups the main clock can be provided as the timer clock source. Thus the timer clock source does not change when the CPU clock is switched. Therefore a fixed period is held.
Figure 3.1 shows Block Diagrams of the Timer Clock Source Select Function.

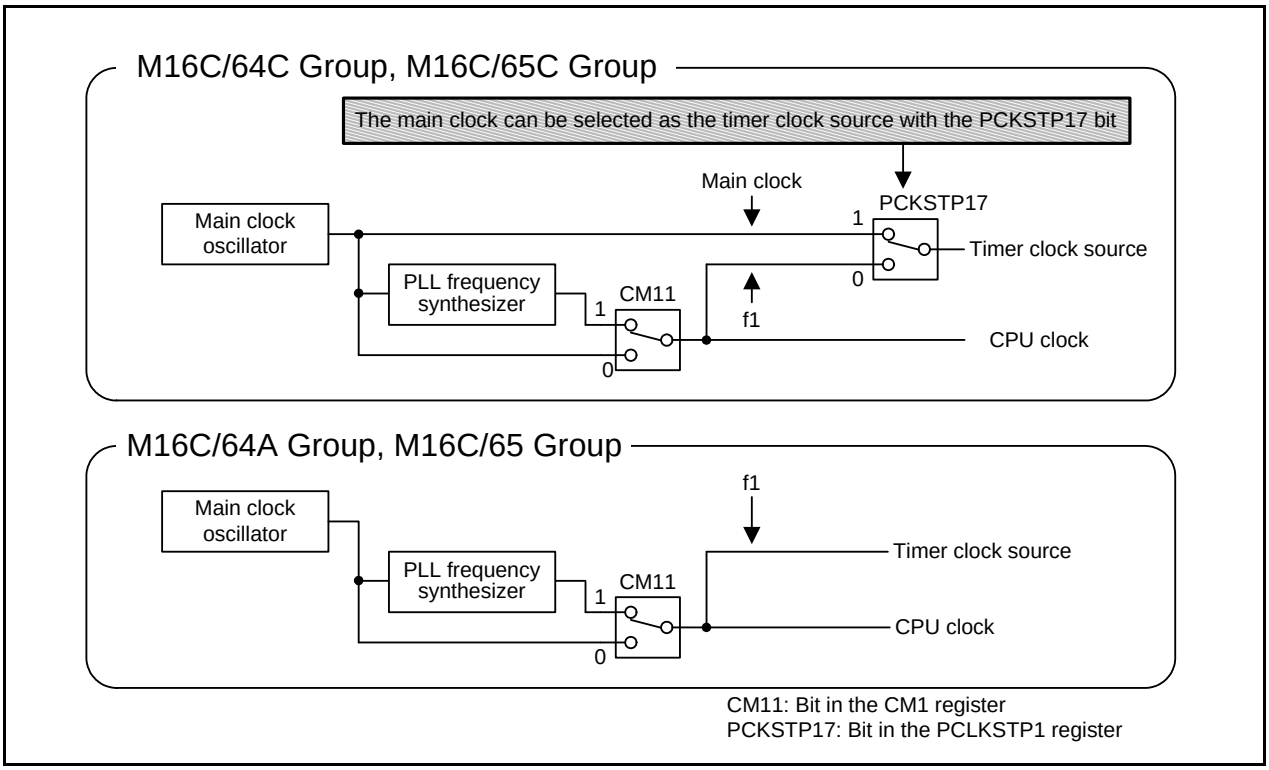

Figure 3.1 Block Diagrams of the Timer Clock Source Select Function

3.2 Notes on Using the Timer Clock Source Select Function

This section describes notes on using the timer clock source select function.

The function of the PCKSTP17 bit in the PCLKSTP1 register provides the main clock to timer A and timer B. Change the PCKSTP17 bit when the following conditions are both met:

- f1 and the main clock are both stably provided.
- All timers in timer A and timer B are stopped.

When using the main clock as the clock source of the timer A and timer B count sources, follow the notes below.

- Set the PCKSTP11 bit in the PCLKSTP1 register to 0 (f1 provide enabled).
- When the PCKSTP17 bit is set to 1, and timer A and timer B are still operating during wait mode, set the CM02 bit to 0 (peripheral function clock f1 does not stop in wait mode).

The main clock can be used as the count source for timer A and timer B when in PLL operating mode, high-speed mode, medium-speed mode, or wait mode. When in normal operating modes other than aforementioned modes, the main clock cannot be used as the count source for timer A and timer B. Figure 3.2 shows Mode Transition when Using the Timer Clock Source Select Function.

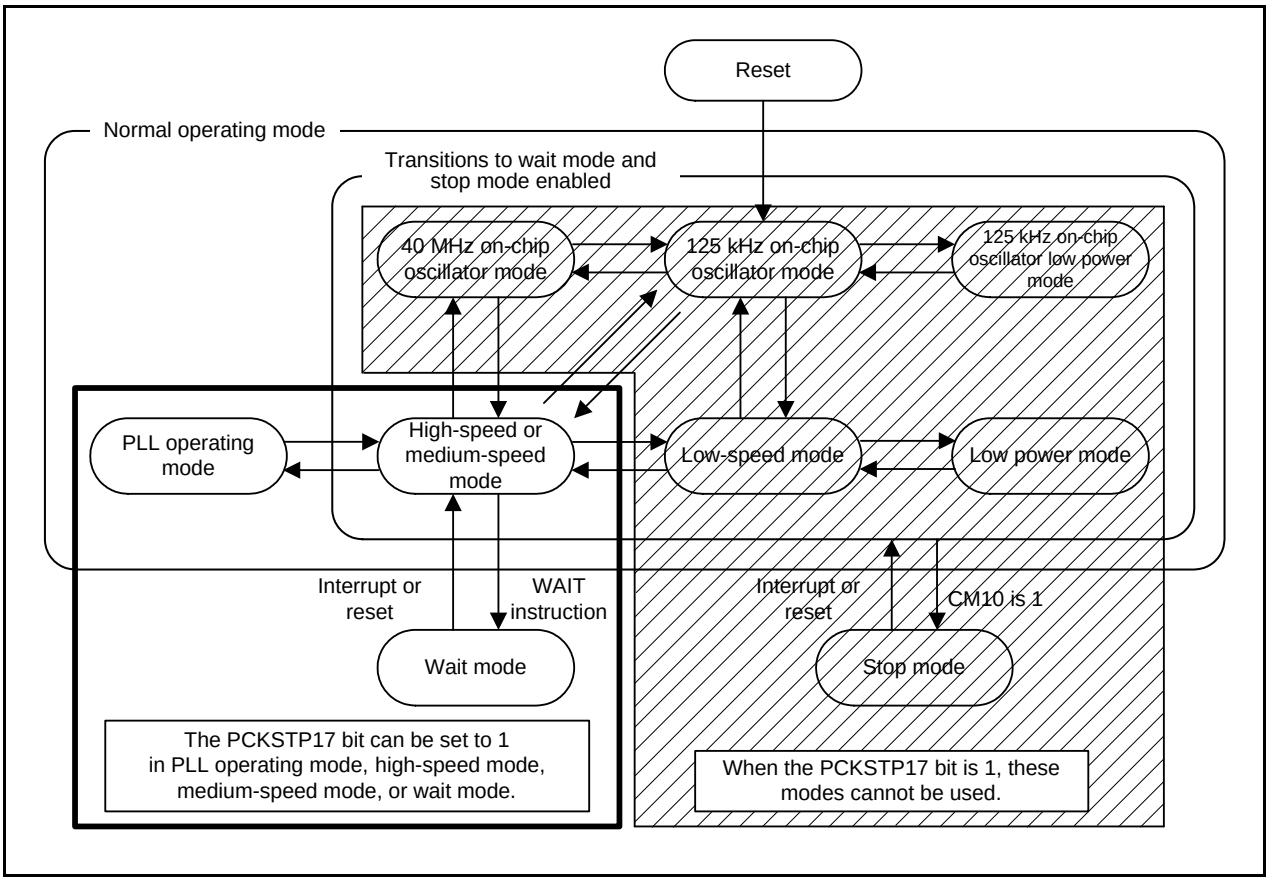

Figure 3.2 Mode Transition when Using the Timer Clock Source Select Function

4. Hardware

4.1 Pin Used

Table 4.1 lists the Pin Used and Its Function.

Table 4.1 Pin Used and Its Function

Pin Name	I/O	Function
P0_0	Output	Invert an output per second.

5. Software

5.1 Operation Overview

The sample code executes the steps 1 to 8 in order. Figure 5.1 shows a Sample Code Operation Example.

(1) Initialize the MCU.
(2) Initialize the peripheral functions (timer A0, ports).
  • Set the PCKSTP17 bit in the PCLKSTP1 register to 1 (main clock).
(3) Timer A0 starts counting.
(4) Execute the CPU clock medium-speed mode transition function.
  • Set the main clock divided by 16 as the CPU clock.
  • Set the PCKSTP1A bit in the PCLKSTP1 register to 1 (f1 provide disabled) to disable f1 provision to peripheral functions other than timer A and timer B.
(5) Execute the WAIT instruction to enter wait mode.
(6) Generate the timer A0 interrupt every 100 ms to exit wait mode.
(7) Execute the CPU clock PLL operating mode transition function.
  • Set the PLL clock with no division as the CPU clock.
  • Set the PCKSTP1A bit in the PCLKSTP1 register to 0 (f1 provide enabled) to enable f1 provision to peripheral functions other than timer A and timer B.
(8) Update the timer A0 interrupt counter.
(9) Check the value of the timer A0 interrupt counter, and invert a port output every second.

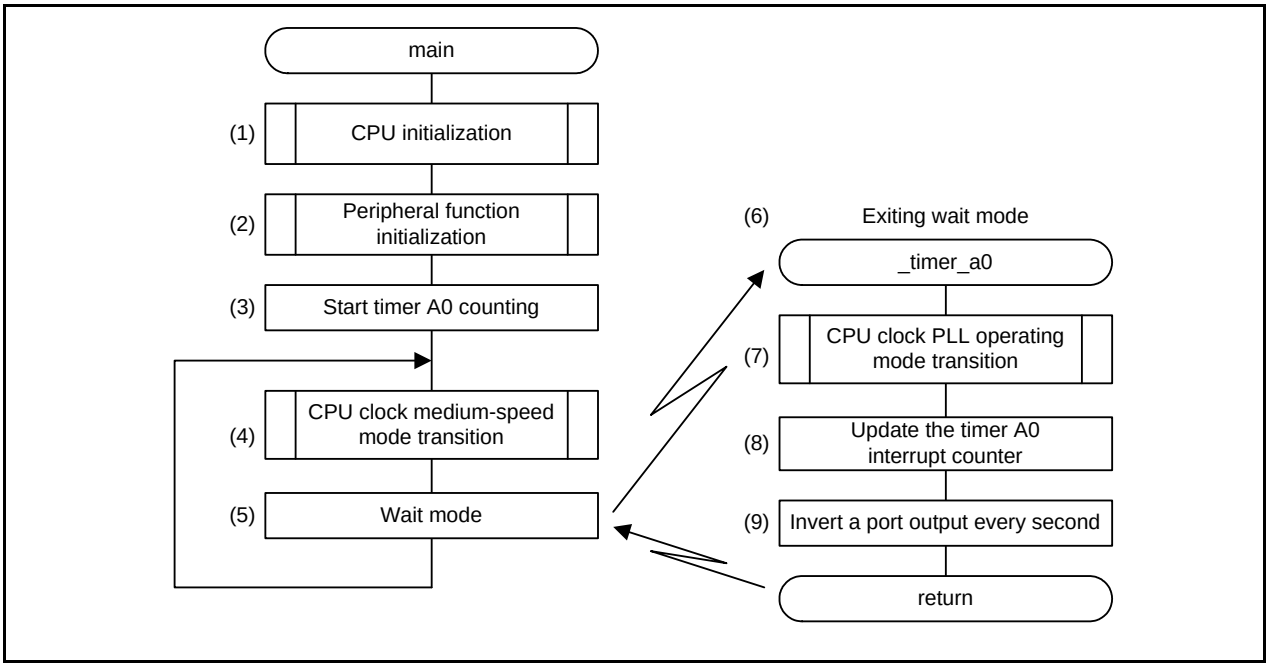

Figure 5.1 Sample Code Operation Example

5.2 Required Memory Size

Table 5.1 lists the Required Memory Size.

Table 5.1 Required Memory Size

Memory Used	Size	Remarks
ROM	270 bytes	In the r01an0711_src.c module
RAM	1 byte	In the r01an0711_src.c module
Maximum user stack usage	10 bytes	
Maximum interrupt stack usage	25 bytes	

The required memory size varies depending on the C compiler version and compiler options.

5.3 Constant

Table 5.2 lists the Constant Used in the Sample Code.

Table 5.2 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
TA_1S	10	Comparison value with the timer A0 interrupt counter.

5.4 Variable

Table 5.3 lists the Global Variable.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
unsigned char	cnt_ta0_int	Timer A0 interrupt counter (counts the number of interrupts every 100 ms)	main, _timer_a0

5.5 Functions

Table 5.4 lists the Functions.

Table 5.4 Functions

Function Name	Outline
mcu_init	CPU initialization
peripheral_init	Peripheral function initialization
cpu_slow	CPU clock medium-speed mode transition
cpu_fast	CPU clock PLL operating mode transition
_timer_a0	Timer A0 interrupt handling

5.6 Function Specifications

The following tables list the sample code function specifications.

mcu_init	
Outline	CPU initialization
Header	None
Declaration	void mcu_init(void)
Explanation	Set the PLL clock (divided by 2, and multiplied by 8) as the CPU clock.
Argument	None
Returned value	None
Remark	

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Explanation	Initialize ports used and initialize timer A0 used to exit wait mode. Set the main clock as the timer clock source.
Argument	None
Returned value	None
Remark	

cpu_slow	
Outline	CPU clock medium-speed mode transition
Header	None
Declaration	void cpu_slow(void)
Explanation	Set the main clock divided by 16 as the CPU clock. Disable f1 provision to peripheral functions other than timer A and timer B.
Argument	None
Returned value	None
Remark	

cpu_fast	
Outline	CPU clock PLL operating mode transition
Header	None
Declaration	void cpu_fast(void)
Explanation	Set the PLL clock with no division as the CPU clock. Enable f1 provision to peripheral functions other than timer A and timer B.
Argument	None
Returned value	None
Remark	

_timer_a0	
Outline	Timer A0 interrupt handling
Header	None
Declaration	void _timer_a0(void)
Explanation	Execute the CPU clock PLL operating mode transition function. Update the timer A0 interrupt counter. Invert the port P0_0 output every second.
Argument	None
Returned value	None
Remark	

5.7 Flowcharts

5.7.1 Main Processing

Figure 5.2 shows the Main Processing.

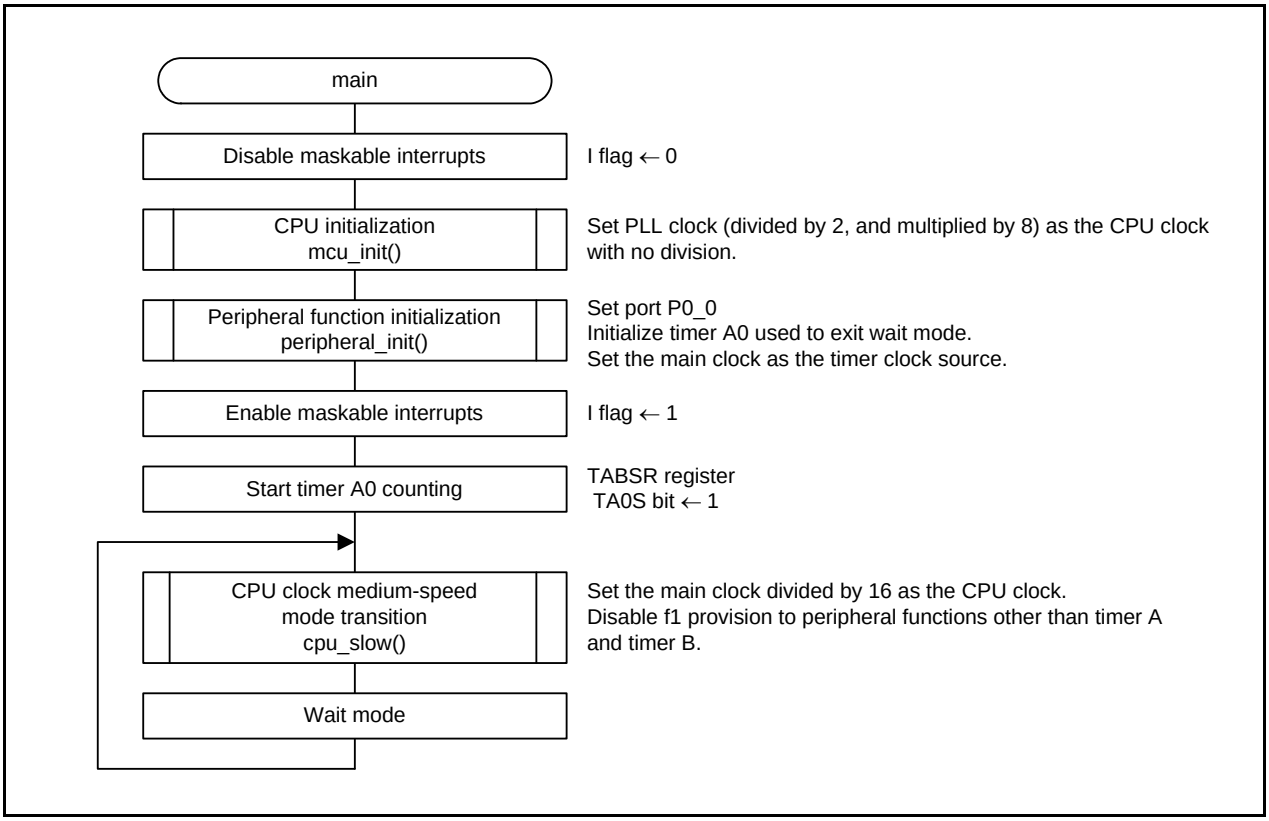

Figure 5.2 Main Processing

5.7.2 Peripheral Function Initialization

Figure 5.3 shows the Peripheral Function Initialization.

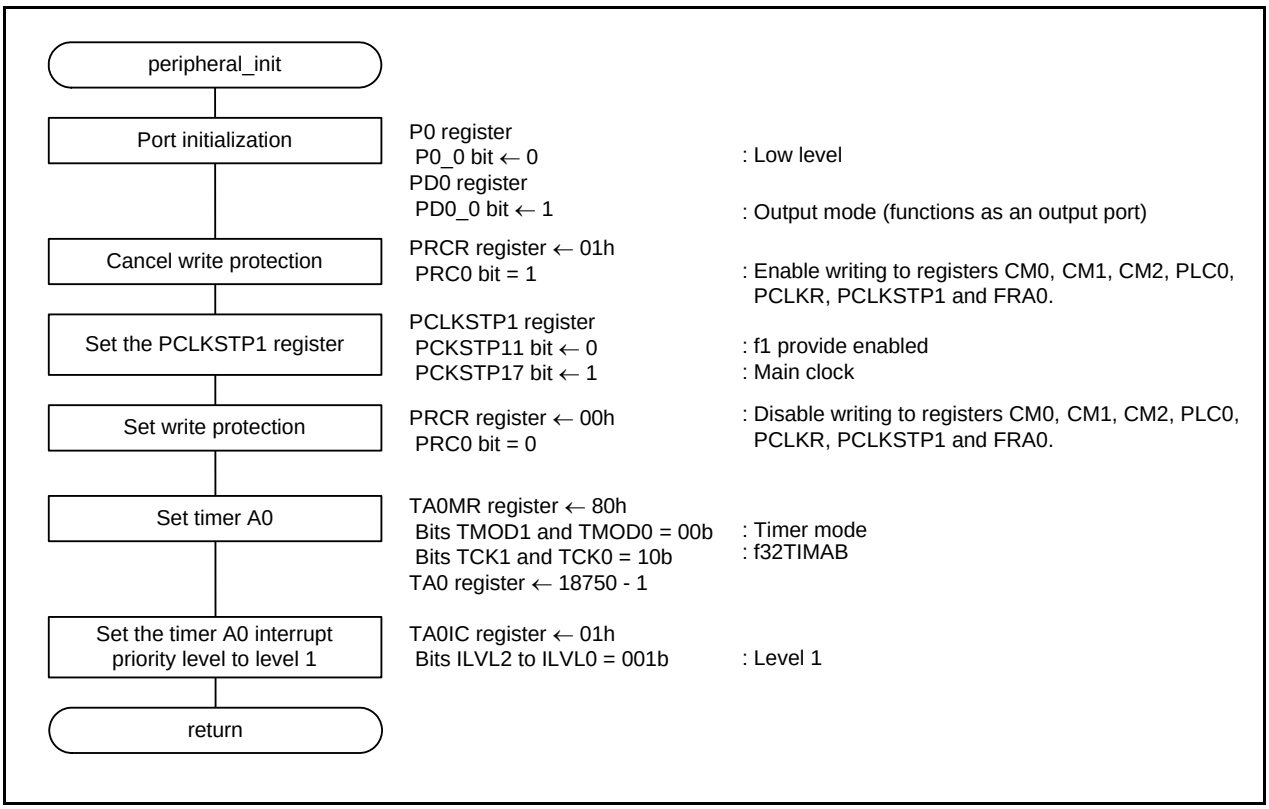

Figure 5.3 Peripheral Function Initialization

5.7.3 CPU Clock Medium-Speed Mode Transition

Figure 5.4 shows the CPU Clock Medium-Speed Mode Transition.

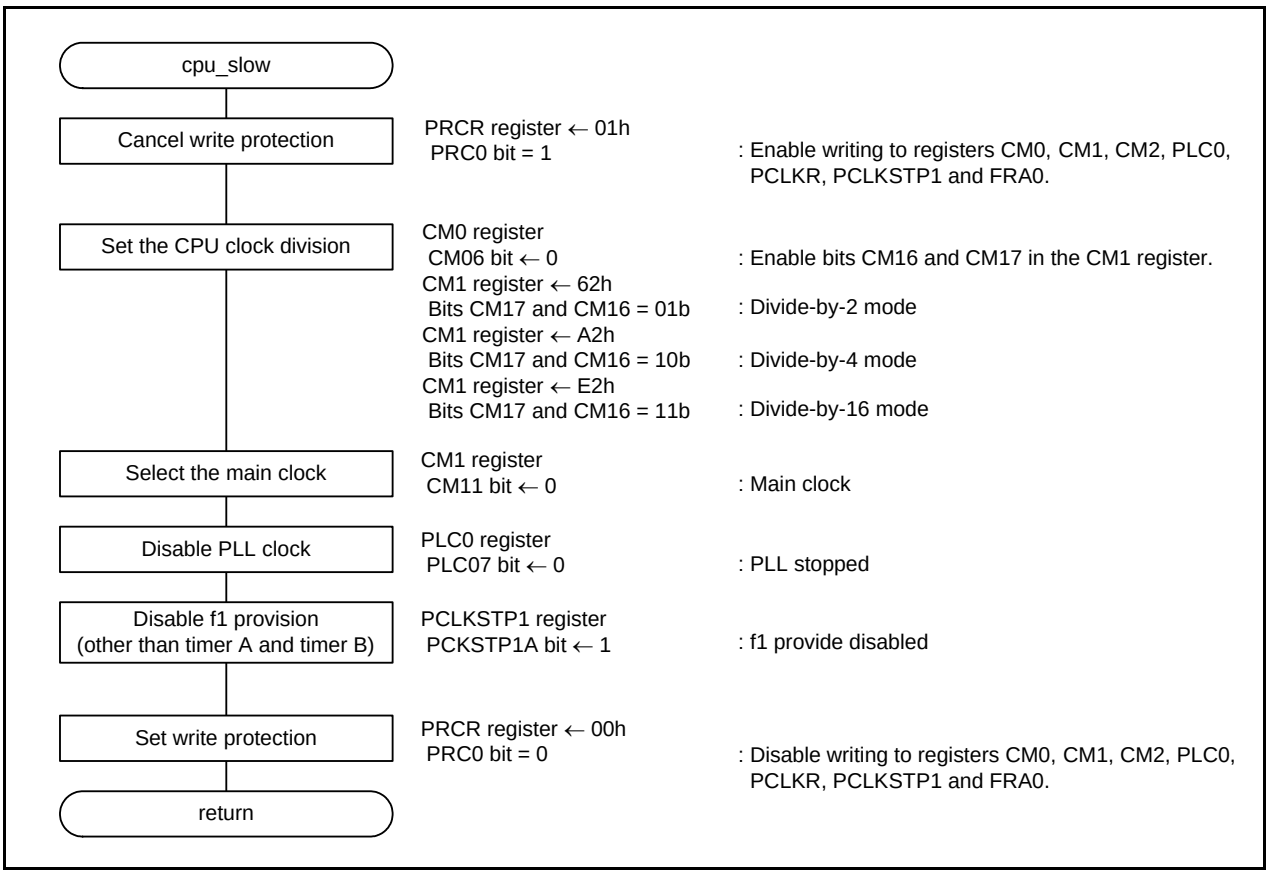

Figure 5.4 CPU Clock Medium-Speed Mode Transition

5.7.4 CPU Clock PLL Operating Mode Transition

Figure 5.5 shows the CPU Clock PLL Operating Mode Transition.

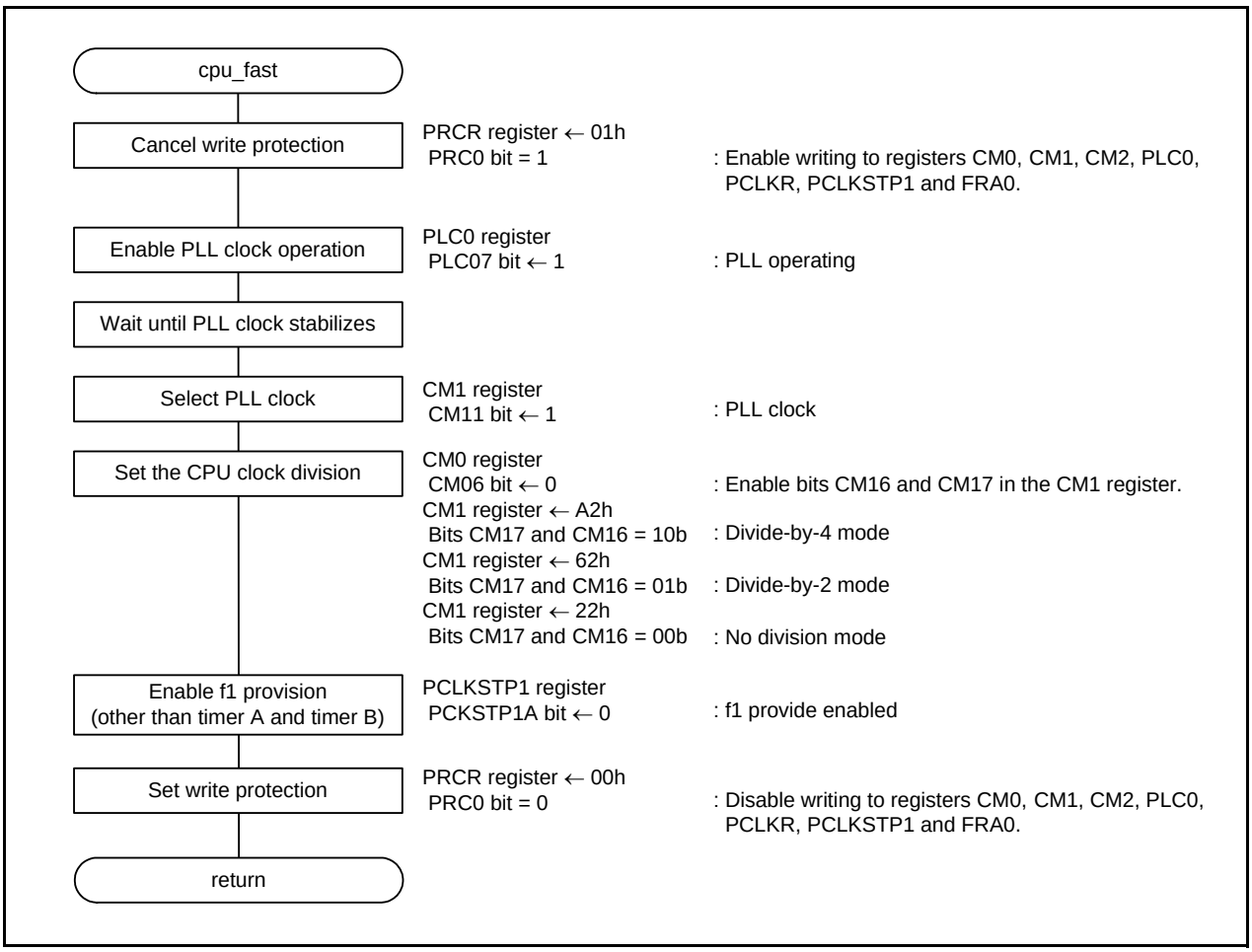

Figure 5.5 CPU Clock PLL Operating Mode Transition

5.7.5 Timer A0 Interrupt Handling

Figure 5.6 shows the Timer A0 Interrupt Handling.

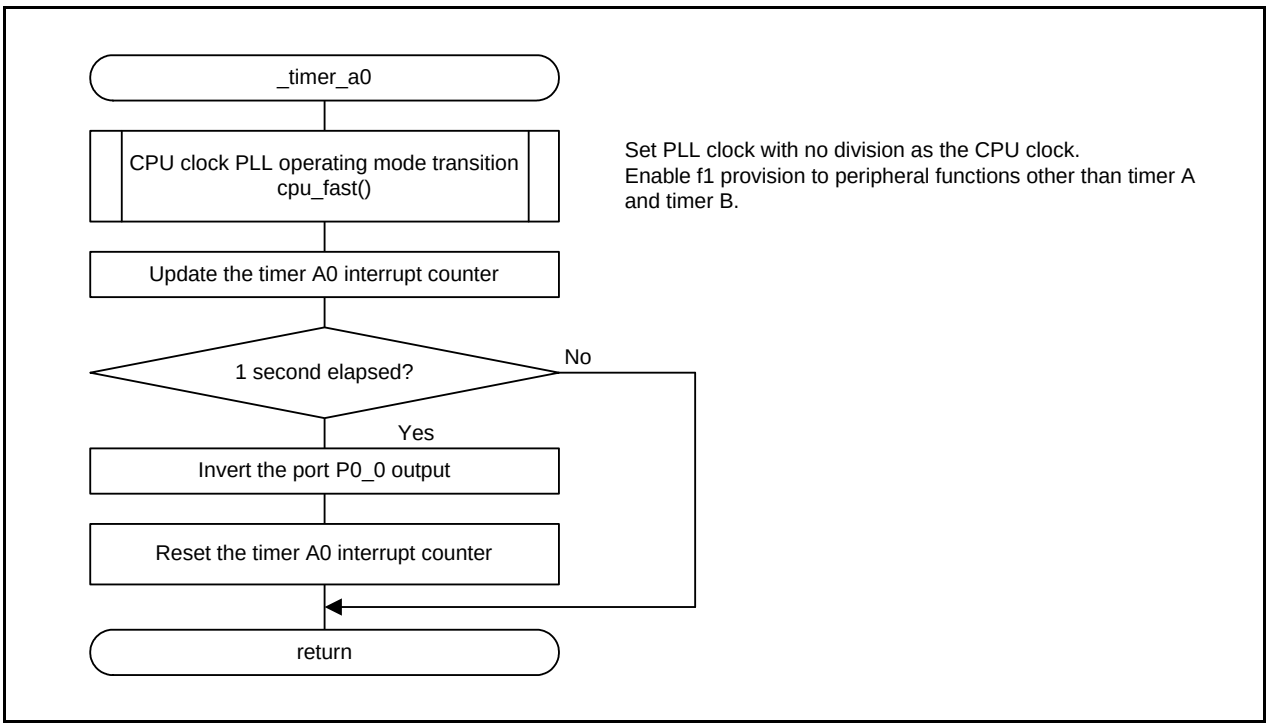

Figure 5.6 Timer A0 Interrupt Handling

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65C Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series/R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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Revision History	M16C/64C Group, M16C/65C Group Providing a Timer Clock Independent of the CPU Clock

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2011	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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