

## M16C/63, 64A, 65, 6C, 5LD, 56D, 5L, and 56 Groups

Timer B (Reading a Counter Value with Pulse Period Measurement Mode)

REJ05B1471-0100 Rev.1.00 Aug 31, 2010

### 1. Abstract

This application notes describes the setting method for reading a counter value with timer B (pulse period measurement mode) in the M16C/63, M16C/64A, M16C/65, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, and M16C/56 Groups.

### 2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

• MCUs: M16C/63 Group

M16C/64A Group

M16C/65 Group

M16C/6C Group

M16C/5LD Group

M16C/56D Group

M16C/5L Group

M16C/56 Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the user's manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

### 3. Pulse Period Measurement Mode

In pulse period measurement mode, the timer measures the pulse period of an external signal.

The count source starts counting at an active edge of the measured pulse, and the counter value is transferred to the register at the next active edge to continue counting.

Table 3.1 lists the Reading from Timer.

Table 3.1 Reading from Timer

Bits PPWFS12 to PPWFS10 in the PPWFS1 Register Bits PPWFS22 to PPWFS20 in the PPWFS2 Register	When 0	When 1
Timer Bi register (i = 0 to 5)	Measurement result	Counter value
Timer Bi-1 register	Undefined value	Measurement result

#### 3.1 Notes on Pulse Period Measurement Mode

When an active edge and overflow are generated simultaneously, input is not recognized at the active edge because an interrupt request is generated only once. Use this mode so overflow is not generated, or use pulse width measurement.

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, a timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If a count is started in this state, the MR3 bit may become 1 and a timer Bi interrupt request may be generated after the count starts before an active edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stopped), the same value is written to the counter.

## 4. Application Example

# 4.1 Application Example Settings

The following describes the application example uses timer B0 in the M16C/65 Group. When using an MCU other than the M16C/65 Group, refer to the user's manual for the particular MCU. Table 4.1 lists Application Example Settings.

Table 4.1 Application Example Settings

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Item	Setting	
Measurement modes	Pulse period measurement  ✓ (Measurement between a falling edge and the next falling edge of the measured pulse.)	
	Pulse period measurement (Measurement between a rising edge and the next rising edge of the measured pulse.)	
	Pulse width measurement (Measurement between a falling edge and the next falling edge of the measured pulse, and between a rising edge and the next rising edge of the measured pulse.)	
Pulse period/width measurement mode select	Measurement result is stored in the TBi register, and the TBi1 register is not used (i = 0 to 5).	
	The counter value is read in the TBi register, and the measurement result is stored in the TBi1 register.	

## 4.2 Application Example Operation

Sample operation of this application note is as follows.

- (1) When the TBiS bit in TABSR or TBSR register is set to 1, the counter starts (i = 0 to 5). While counting, ports P1 to P0 output the counter value.
- (2) When a measurement edge is input, the counter value is set to 0000h, and starts measurement. At this time, an undefined value is transferred to the reload register. A timer Bi interrupt is not requested.
- (3) When a measurement edge is input again, the counter value is transferred to the reload register, the counter becomes 0000h and starts measurement again.
- (4) The IR bit in the TBiIC register becomes 1 (interrupt requested). The MR3 bit in the TBiMR register is read in the interrupt processing.
  - (4-1) When the MR3 bit is 0 (no overflow), the measured value which has been stored in the TBi1 register is stored to RAM.
  - (4-2) When the MR3 bit is 1 (overflow), the related registers to timer Bi because sample program concludes the open-circuit or abnormal external circuit. Besides, P2\_0 is used as an error port and set to high.

Figure 4.1 shows the Timing of the Sample Program.

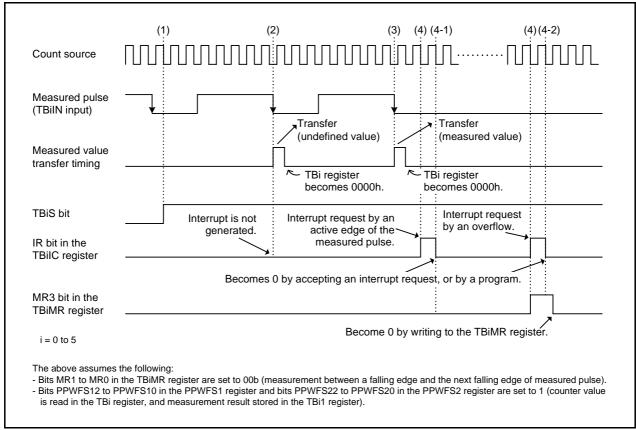


Figure 4.1 Timing of the Sample Program

### 4.3 Flowchart

## 4.3.1 Main Program

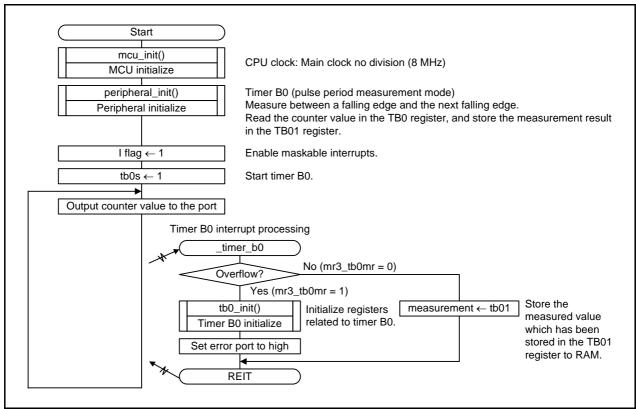


Figure 4.2 Main Program Flowchart

#### 4.3.2 Timer B0 Initialization

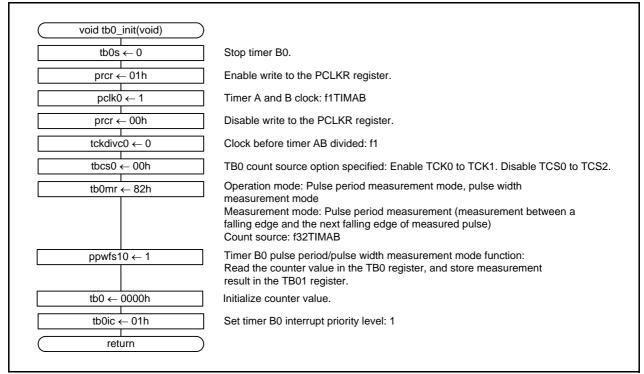


Figure 4.3 Timer B0 Initialization Flowchart

## 5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

#### 6. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.1.00 M16C/64A Group User's Manual: Hardware Rev.1.10 M16C/65 Group User's Manual: Hardware Rev.1.10 M16C/6C Group User's Manual: Hardware Rev.1.00 M16C/5LD, 56D Group User's Manual: Hardware Rev.1.10 M16C/5L, 56 Group User's Manual: Hardware Rev.1.00

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History	M16C/63, 64A, 65, 6C, 5LD, 56D, 5L, and 56 Groups Timer B (Reading a Counter Value with Pulse Period
	Measurement Mode)

Rev. Date	Data	Description		
	Date	Page	Summary	
1.00	Aug 31, 2010	_	First edition issued	

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

#### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

#### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

#### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

 The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

#### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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