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M16C/62P

I²C Master Interface Driver using DMA and ACK/NACK Interrupts

Introduction

This application note provides an example of how to use the M16C family I²C mode provided in the UART peripheral. A master implementation using the on chip DMA and ACK/NACK interrupts is shown interfacing to an external I²C EEPROM.

The hardware configuration consisted of a M30627FJPFP (M16C/62P with 512KFLASH/31KRAM/100pin) and a HN58X2404SI (RENESAS 4K I²C EEPROM with 512-word x 8-bit) connected via the M16C UART in I²C mode with external 1Kohm pull-up resistors on the SDA and SCL lines.

The source code has been tested with various M16C devices, UARTs, and compilers (both IAR and RENESAS NC30) with speeds up to 400Kb/s.

The program described in this example uses the I2C library to write and check-out correct writing/reading of a string of characters in the external EEPROM.

The string used is: “Thank you for using RENESAS M16C family I²C (this code uses ACK/NACK interrupt routines)”.

The number of message writes and errors (normally none) are monitored in 2 variables for reliability test purposes.

All tested conditions are validated only if no error was generated during the test. The source code and complete project files is available to download free of charge from our Website.

As M16C and M32C devices share most peripherals, it could be of interest to read following application note “Using Simple I2C Bus Mode on M32C/83.85” (www.renesas.com M16C application note REJ05B0145-0100Z).

Contents

Possible configurations.

The following table shows the possible options supported by current software version.

	M16C26	M16C26A	M16C28	M16C29	M16C6N4	M16C62P
UART0	Not applicable	Not applicable	Not applicable	Not applicable	**Tested**	**Tested**
UART1	Not applicable	Not applicable	Not applicable	Not applicable	*Not tested*	*Not tested*
UART2	**Tested**	*Not tested*	*Not tested*	*Not tested*	**Tested**	**Tested**
DMA1	**Tested**	*Not tested*	*Not tested*	*Not tested*	**Tested**	**Tested**

The options which have been tested were confirmed to work correctly with no errors detected during the test (the other ones should work as well but haven't been tested).

Usage.

1. Abstract of CPU.h

The "cpu.h" file allows choosing the configuration options; this file needs to be modified in order to select the correct configuration setting.

DMA1 used (or not), which UART is used (when this option is available for selected device), which device is used and which compiler (Renesas NC30 or IAR).

```
// -------------------------------------------------------------------------
// DMA use (comment this line if DMA1 is not used for transmission)
// -------------------------------------------------------------------------
#define DMA1_USED
// -------------------------------------------------------------------------
// UART selection (please uncomment one of here bellow only)
// -------------------------------------------------------------------------
//#define UART0
//#define UART1     // NOT TESTED ON THIS UART YET !!!!!!
#define UART2
// -------------------------------------------------------------------------
// CPU selection (please uncomment one of here bellow only)
// -------------------------------------------------------------------------
//#define M16C26
//#define M16C26A
//#define M16C28
#define M16C62P
//#define M16C6N4

//#define EVA_3DK62P
#ifdef  DMA1_USED
        #ifdef  UART0
        #define DMA1_ACK_TRIG_SOURCE   0x0B;   // Trig by UART0 ACK
        #endif
        #ifdef  UART1
          #define DMA1_ACK_TRIG_SOURCE 0x0F;   // Trig by UART1 ACK
        #endif
        #ifdef  UART2
        #define DMA1_ACK_TRIG_SOURCE   0x0D;   // Trig by UART2 ACK
  #endif
#endif
```

2. Detailed description.

The I²C protocol uses following main states for communication:

- START bit.
- Normal communication (8-bit synchronous).
- ACK or NACK bits
- STOP bit.

The M16C devices offer 2 options to implement the communication:

a) ACK/NACK interrupts (used in this example).

b) UART transmit/receive interrupts (used in M32C example mentioned above).

The first option (a) is more suitable in master mode as the master only needs to monitor the ACK/NACK signal from the slave. For slave mode the second option (b) is more appropriate as the slave needs to generate itself the ACK and NACK signals upon reception of data and or address.

Below figure shows the timing and process being used in this application note.

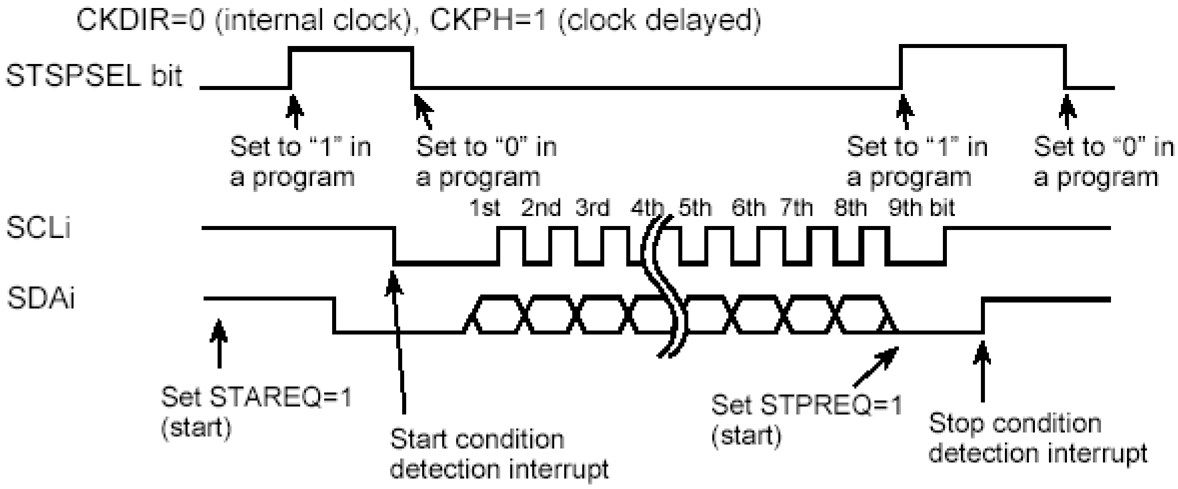


Figure 1

The register UiSMR4 allows automatic generating the START and STOP signals (as well as RESTART which is not used here). This register has only been introduced in the recent M16C devices (the ones mentioned in above tables) and offers the benefit of avoiding direct port toggling to generate these conditions.

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
U0SMR4 to U2SMR4	036Ch, 0370h, 0374h	00h

Bit	Bit Symbol	Bit Name	Function	RW
b0	STAREQ	Start Condition Generate Bit [1]	0 : Clear 1 : Start	RW
b1	RSTAREQ	Restart Condition Generate Bit [1]	0 : Clear 1 : Start	RW
b2	STPREQ	Stop Condition Generate Bit [1]	0 : Clear 1 : Start	RW
b3	STSPSEL	SCL,SDA Output Select Bit	0 : Start and stop conditions not output 1 : Start and stop conditions output	RW
b4	ACKD	ACK Data Bit	0 : ACK 1 : NACK	RW
b5	ACKC	ACK Data Output Enable Bit	0 : Serial I/O data output 1 : ACK data output	RW
b6	SCLHI	SCL Output Stop Enable Bit	0 : Disabled 1 : Enabled	RW
b7	SWC9	SCL Wait Bit 3	0 : SCL "L" hold disabled 1 : SCL "L" hold enabled	RW

3. Start condition generation

A high-to-low transition of the SDA with SCL high is generated in order to start read, write operation.

Bellow 2 lines will force the device to generate the START condition:

UiSMR4 = 0x71; // Start condition generate (STSPSEL=0/STAREQ=1)

UiSMR4 = 0x09; // STSP output enable (STSPSEL=1/STAREQ=1)

After UiSMR4 has been set as mentioned the device generates the START signal which automatically generates a START/STOP interrupt request.

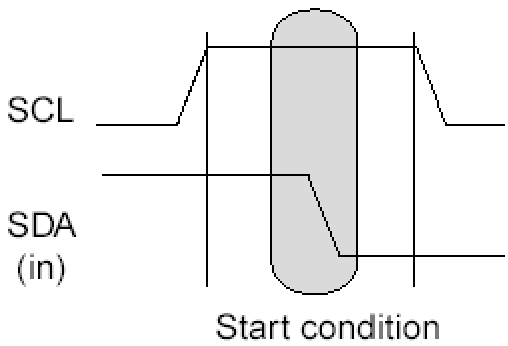


Figure 2

The first action to be done in the START interrupt routine section is to clear the START signal request by setting new value in UiSMR4 register:

UiSMR4 = 0x00; // clear : STSPSEL=0

4. Stop Condition generation

A low-to-high of the SDA with the SCL high is a stop condition. In the case of write operation, a stop condition terminates the write data input and places the device in an internally-timed write cycle to the memories.

Similarly to START condition, the STOP condition is initiated by configuring the UiSMR4 register:

UiSMR4 = 0x74;   // SCL=SDA="H"

UiSMR4 = 0x0C;   // Stop condition (STSPSEL=1/STPREQ=1)

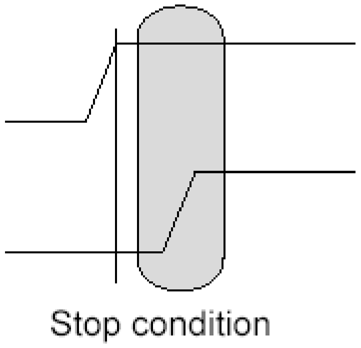


Figure 3

After UiSMR4 has been set as mentioned the device generates the STOP signal which automatically generates a START/STOP interrupt cause.

The first action to be done in the STOP interrupt routine section is to clear the STOP signal request by setting new value in UiSMR4 register:

UiSMR4 = 0x30;   // ACK data output "H"

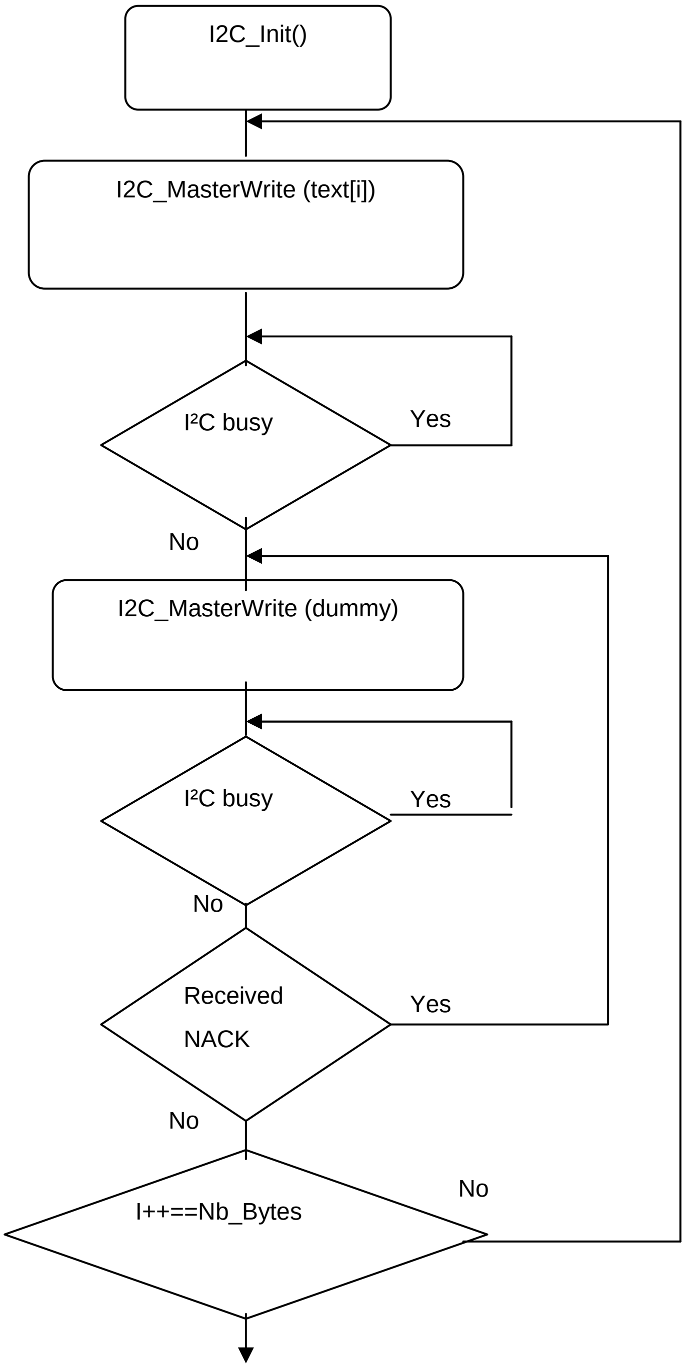
5. Interrupt causes

Below interrupt vectors are used in order to process data transmission and reception.

Interrupt function name	result
UARTi Bus Collision Detect	Start condition detection or stop condition detection
NACK interrupt (shared with Transmit Interrupt)	No acknowledgment detection (NACK) Rising edge of SCLi 9th bit
ACK interrupt (shared with Receive Interrupt)	Acknowledgment detection (ACK) Rising edge of SCLi 9th bit

Main program flowchart.

1. **Main routine (write portion)**

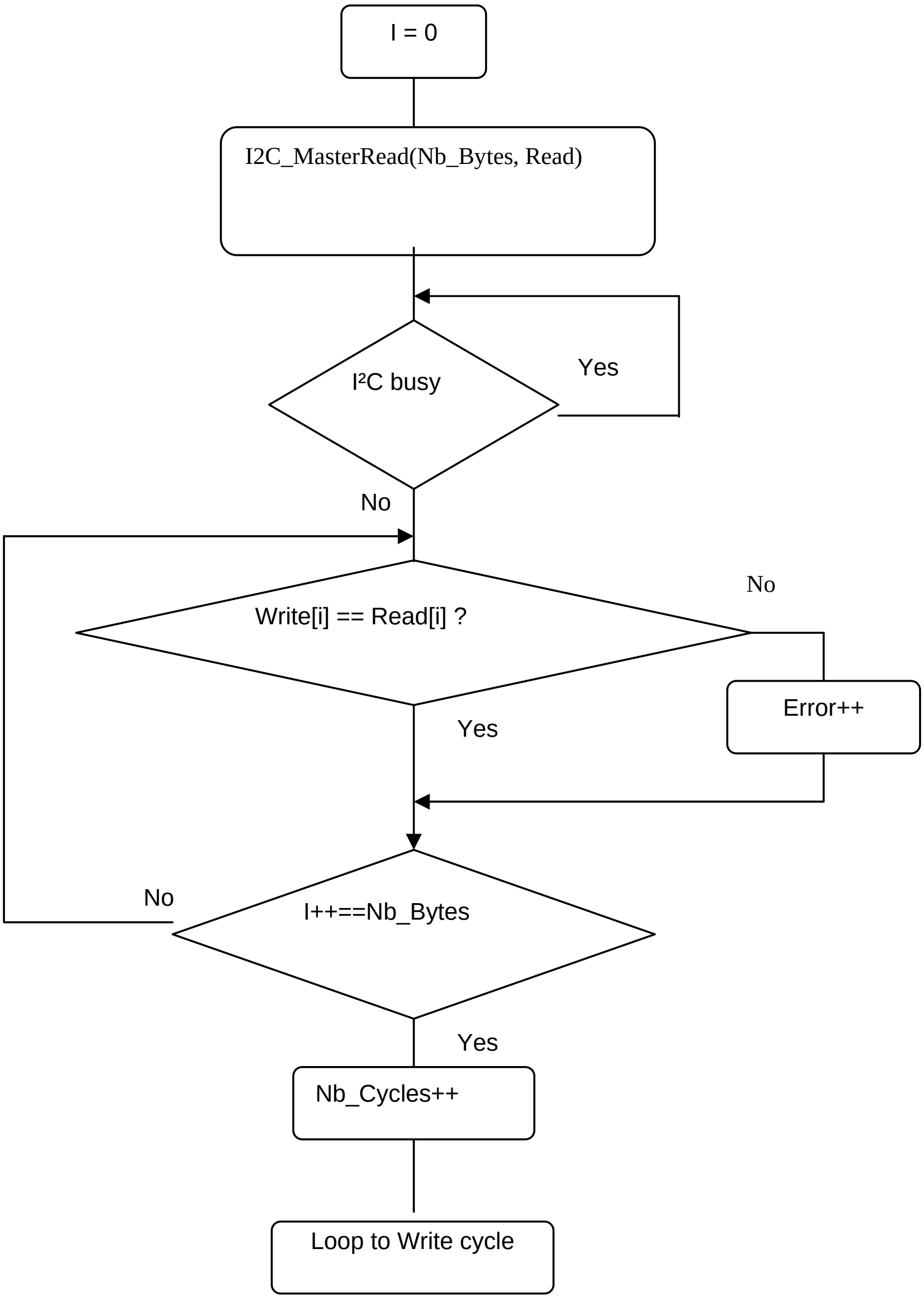


Write data to EEPROM

Test if EEPROM has finished writing

Loop until EEPROM is not busy

2. Main routine (verify portion)



Functions description.

Only 3 functions are currently accessible from application software, these are I2C_init, I2C_MasterWrite and I2C_MasterRead. The other functions described below shouldn't be called by the application software (most of them are interrupt functions). The pins used for I²C interface should be kept in input mode.

1. **void I2C_init (void)**

This function is to be called in the processor initialization section. It prepares the UART settings to work in I²C mode.

2. **I2C_MasterWrite(address, *ptrData, length)**

This function will start a write process to slave peripheral. Input parameters are device address, pointer to data to be written (ptrData) and number of bytes to be written (length). Inside the function a global bit variable "busy" (CurrentStatus.bit.busy) is used to monitor I²C bus status to avoid accessing the bus while a cycle is not completed. When a new cycle is started this boolean is set true, at the end of the cycle the driver code clears this Boolean to false to allow a new cycle to start (see below I2C_StartStopDetection function) .

If a new request comes while the "busy" bit is set, the driver returns an error and nothing is done.

If "busy" Boolean is false it is turned true and driver global variables are initialized with passed parameters (these will be shared and modified by interrupt functions).

3. **I2C_MasterRead(address, *ptrData, length)**

This function will start a read process from slave peripheral. Input parameters are device address, pointer to buffer where data is to be stored (ptrData) and number of bytes to be read (length). In the function a global bit variable "busy" (CurrentStatus.bit.busy) is used to monitor I²C bus status to avoid accessing the bus while a cycle is not completed. The function of the "busy" bit is same as in the I2C_Master function.

4. **_INTERRUPT void I2C_StartStopDetection(void)**

This function is called when a stop or start condition interrupt is generated. The BBS bit in the UiSMR sfr register indicates whether it is the start or stop condition ("1" indicates start and "0" indicates stop condition).

When start condition is the interrupt cause this routine will send the I²C slave address (including R/W bit) with 9^{th} bit set to 1 (to allow slave to generate ACK or NACK) and enable the NACK and ACK interrupts (or DMA instead of ACK interrupt in case it is used to automatically send the data).

When a stop condition is detected both NACK, ACK interrupts are disabled and "busy" bit is cleared to allow later access to the bus for other requests.

5. **_INTERRUPT void I2C_ACK(void)**

This function is called when ACK condition is detected. It is enabled in I²C read or I²C write modes if the DMA is not used or only in I²C read mode if DMA is used.

In I²C write mode this routine will write data buffer contents to UARTi transmit buffer with automatic increment of the data buffer index.

In I²C read mode it stores contents of UARTi receive buffer in the data buffer (with automatic increment of buffer index) and it will put 0x00FF in the UARTi transmit register to acknowledge received byte (9^{th} bit to 0 means ACK signal is sent). The last byte transmitted should be 0x01FF so that slave can put the ACK level (or NACK in case of problem) for acknowledgement of the transmission.

6. **_INTERRUPT void I2C_NACK(void)**

This function allows stopping the on-going I²C transmission by disabling ACK interrupt or DMA.

7. **_INTERRUPT void DMA_interrupt(void)**

Stops DMA function and enables ACK interrupt (to accept last byte).

Conclusion

M16C devices offer a powerful and easy way of handling I²C bus to slave devices without consuming CPU power doing port toggling. This application note is made available to help M16C developers speed up their development.

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