RX72T Group, RX62T/RX62G Group

Differences Between the RX72T Group and the RX62T Group

Summary

This application note is a reference document that lists differences in peripheral modules, I/O registers, and pin functions between the RX72T Group and the RX62T Group. This document also provides important information that needs to be taken into account when replacing the MCU. Unless otherwise indicated the maximum MCU specifications of RX72T Group products with 144 pins (with programmable gain amplifier (PGA) pseudo-differential input and USB pins) and RX62T Group products with 112 pins are described. Refer to the User's Manual: Hardware of each MCU for details of differences in electrical characteristics, usage notes, and setting procedures.

Target Devices

RX72T Group

RX62T Group

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1. Comparison of Built-In Functions of RX72T Group and RX62T Group

Table 1.1 is a comparative listing of the built-in functions of RX72T Group and RX62T Group. For details of each function, refer to section 2, Comparative Overview of Specifications, as well as the documents listed in section 5, Reference Documents.

Table 1.1 Comparison of Built-In Functions of RX72T Group and RX62T Group

Function	RX62T	RX72T
CPU	●	
Operating modes	●	
Address space	▲	
Resets	▲	
Option-setting memory (OFSM)	*1	○
Voltage detection circuit (LVD): RX62T, (LVDA): RX72T	▲	
Clock generation circuit	●	
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption	●	
Register write protection function	×	○
Exception handling	▲	
Interrupt controller (ICU): RX62T, (ICUC): RX72T	●	
Buses	●	
Memory-protection unit (MPU)	▲	
DMA controller (DMACAa)	×	○
Data transfer controller (DTC): RX62T, (DTCa): RX72T	●	
Event link controller (ELC)	×	○
I/O ports	●	
Multi-function pin controller (MPC)	*2	○
Multi-function timer pulse unit 3 (MTU3): RX62T, (MTU3d): RX72T	●	
Port output enable 3 (POE3): RX62T, (POE3B): RX72T	●	
General PWM timer (GPT/GPTa): RX62T, (GPTW): RX72T	● *3	
High resolution PWM waveform generation circuit (HRPWM)	*4	○
GPT port output enable (POEG)	×	○
8-bit timer (TMR)	×	○
Compare match timer (CMT)	●	
Watchdog timer (WDT): RX62T, (WDTA): RX72T	●/▲	
Independent watchdog timer (IWDT): RX62T, (IWDTa): RX72T	●	
USB 2.0 FS Host/Function module (USBb)	×	○
Serial communications interface (SCIb): RX62T, (SCIj, SCIi, SCIh): RX72T	●	
I²C bus interface (RIIC): RX62T, (RIICa): RX72T	●	
CAN module (CAN)	●	
Serial peripheral interface (RSPI): RX62T, (RSPIc): RX72T	●	
CRC calculator (CRC): RX62T, (CRCA): RX72T	●	
Arithmetic unit for trigonometric functions (TFU)	×	○
Trusted secure IP (TSIP-Lite)	×	○
LIN module (LIN)	○	*5
12-bit A/D converter (S12ADA): RX62T, (S12ADH): RX72T	●	
10-bit A/D converter (ADA)	○	×
12-bit D/A converter (R12DAb)	×	○
Temperature sensor (TEMPS)	×	○
Comparator C (CMPC)	*6	○
Data operation circuit (DOC)	×	○

Function	RX62T	RX72T
RAM	●/▲	
Flash memory	●/▲	
Packages	●/▲/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. Section 31, ROM (Flash Memory for Code Storage), in RX62T Group, RX62G Group User's Manual: Hardware contains a description of functions corresponding to the description of the option setting memory in the documentation of the RX72T Group. For details, refer to 4, Important Information when Migrating Between MCUs.
2. Section 15, I/O Ports, in RX62T Group, RX62G Group User's Manual: Hardware contains a description of functions corresponding to the description of the multi-function pin controller in the documentation of the RX72T Group. For details, refer to 4, Important Information when Migrating Between MCUs.
3. The GPTa is implemented on the RX62G Group only.
4. A description of the HRPWM function appears in the General PWM Timer (GPT) section of RX62T Group, RX62G Group User's Manual: Hardware.
5. The description of the SCIh in the documentation of the RX72T Group describes functions corresponding to those described in section 27, LIN Module (LIN), in RX62T Group, RX62G Group User's Manual: Hardware.
6. A description of the comparator function appears in the 12-Bit A/D Converter (S12ADB) section of RX62T Group, RX62G Group User's Manual: Hardware.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX62T	RX72T
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 200 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Single-precision floating point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX62T	RX72T
EXTB	—	—	Exception table register
ACC (RX62T) ACC0, ACC1 (RX72T)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Operating Modes

Table 2.3 is a comparative overview of operating modes, and Table 2.4 is a comparison of operating mode–related registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX62T	RX72T
Selection of operating modes by mode-setting pins on release from reset state	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	—	Boot mode (USB interface)
	—	Boot mode (FINE interface)
	—	User boot mode
Selection of operating modes by register settings	Single-chip mode	Single-chip mode
	—	User boot mode
	—	On-chip ROM disabled extended mode
	—	On-chip ROM enabled extended mode
Selection of endian order	MDE pin	MDE register

Table 2.4 Comparison of Operating Mode–Related Registers

Register	Bit	RX62T	RX72T
MDMONR	MD	—	MD pin status flag
	MD0	MD0 pin status flag	—
	MD1	MD1 pin status flag	—
	MDE	MDE pin status flag	—
MDSR	IROM	On-chip ROM startup status flag	—
	BOTS	Boot mode startup flag	—
	UBTS	—	User boot mode startup flag
SYSCR0	EXBE	—	External bus enable bit
SYSCR1	—	System control register 1	System control register 1
		Initial values after a reset are different.	
	ECCRAME	—	ECCRAM enable bit
VOLSR	—	—	Voltage level setting register

2.3 Address space

Figure 2.1 is a comparative memory map of single-chip mode on the RX62T: R5F562TAxxxx, Figure 2.2 is a comparative memory map of single-chip mode on the RX62T: R5F562T7xxxx, and Figure 2.3 is a comparative memory map of single-chip mode on the RX62T: R5F562T6xxxx.

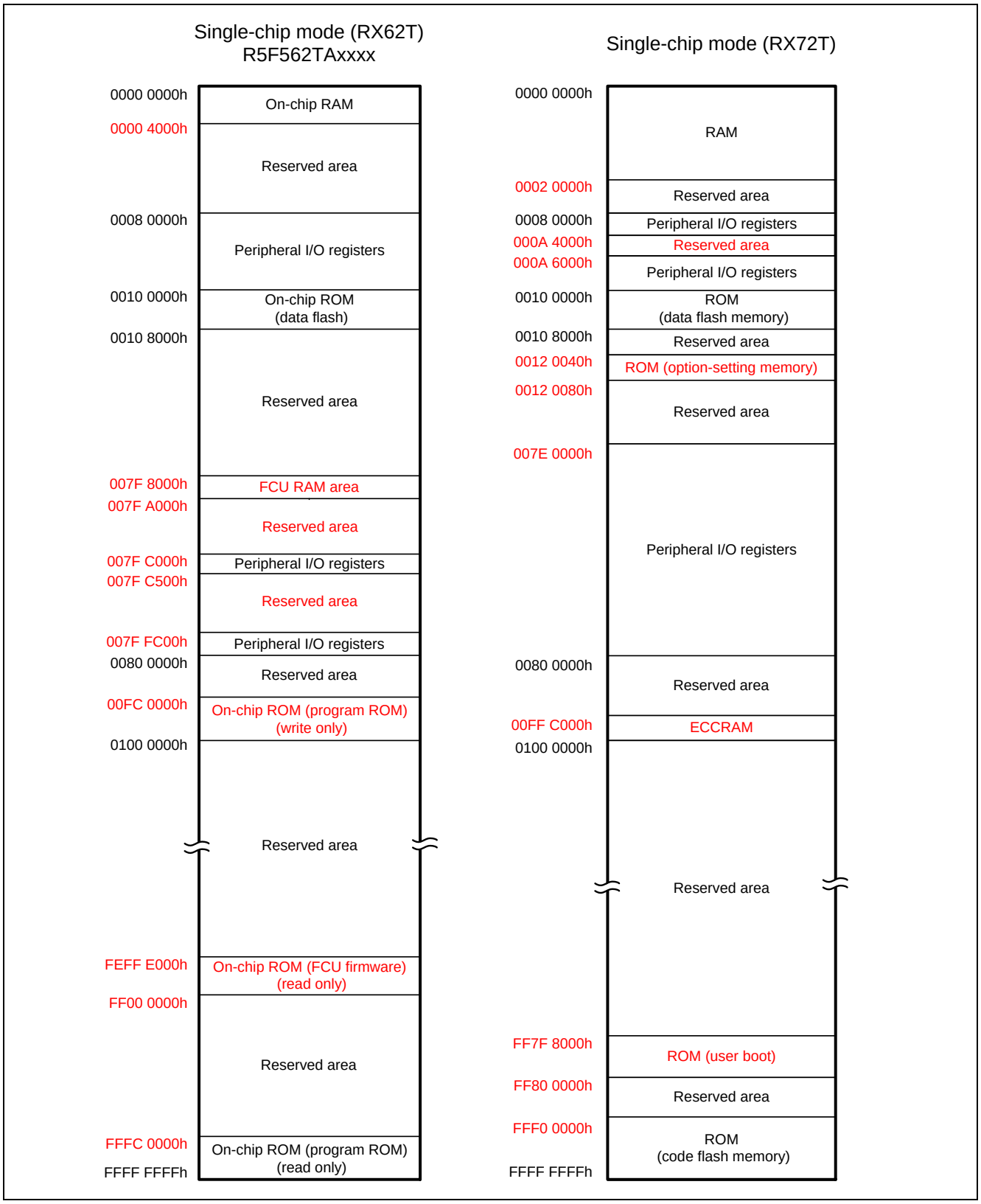


Figure 2.1 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562TAxxxx)

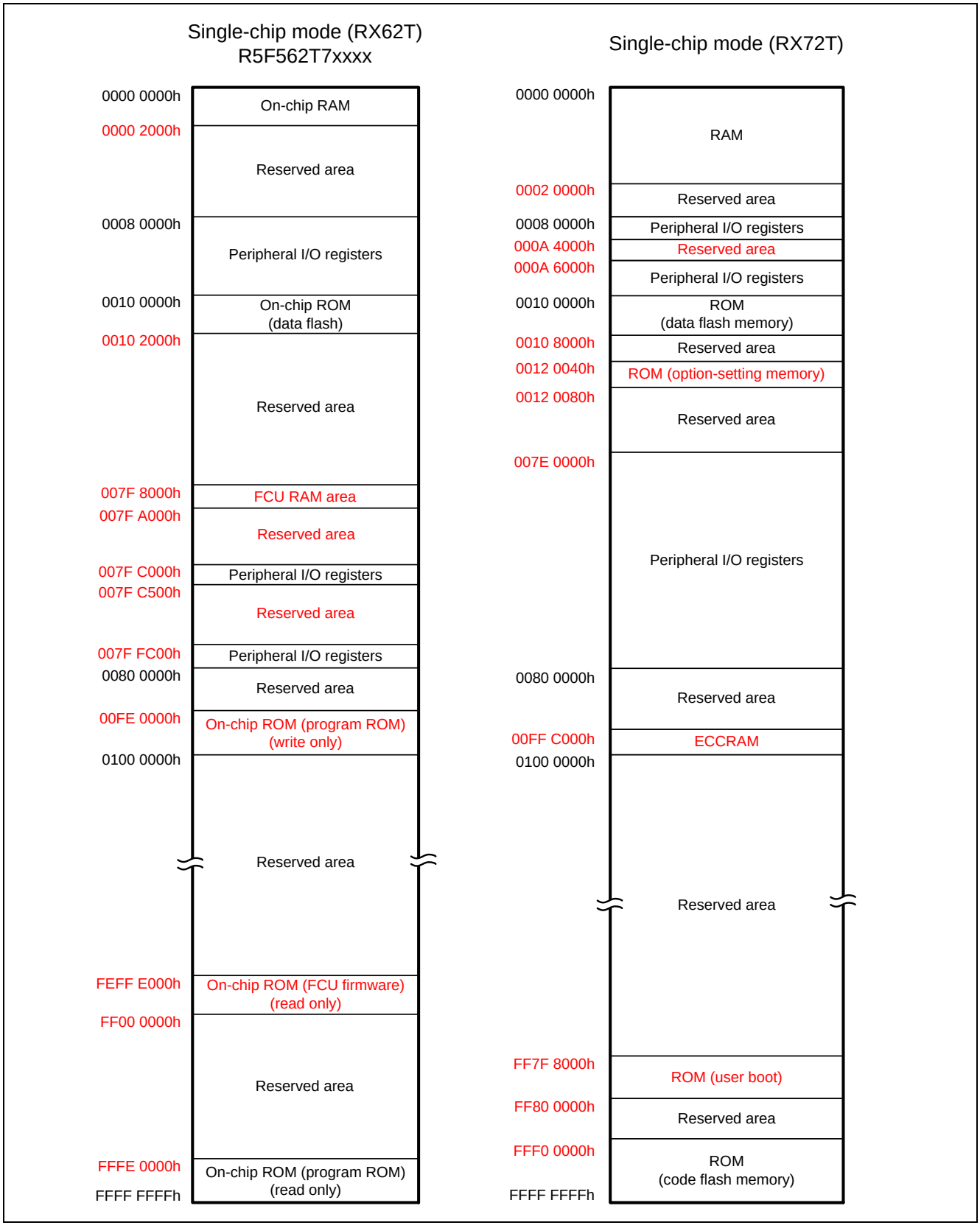


Figure 2.2 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562T7xxxx)

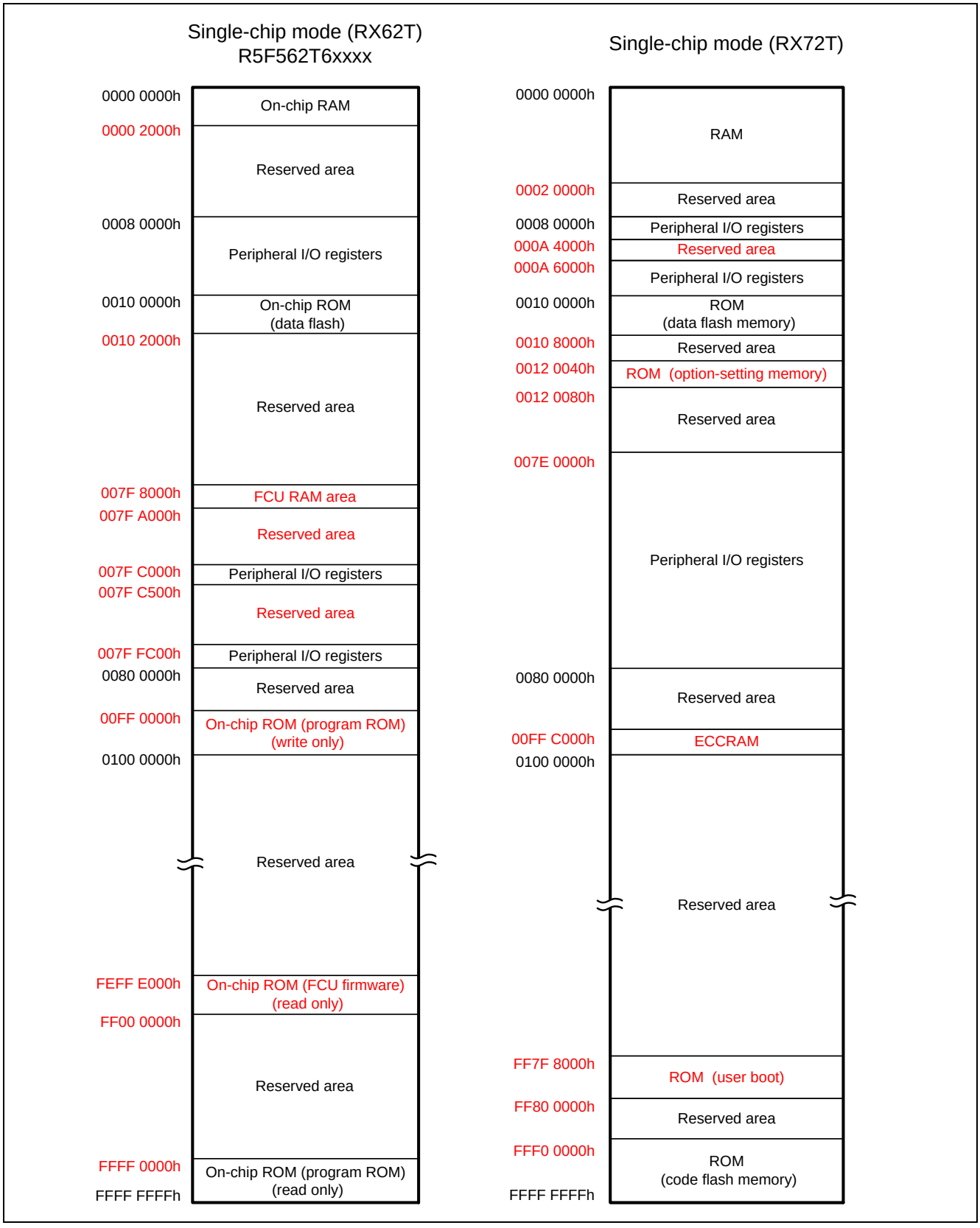


Figure 2.3 Comparative Memory Map of Single-Chip Mode (RX62T: R5F562T6xxxx)

2.4 Resets

Table 2.5 is a comparative overview of resets, and Table 2.6 is a comparison of reset-related registers.

Table 2.5 Comparative Overview of Resets

Item	RX62T	RX72T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises or falls (voltage detection: VPOR)	VCC rises (voltage detection: VPOR)
Voltage-monitoring reset 0	—	VCC falls (voltage detection: Vdet0)
Voltage-monitoring reset 1	VCC falls (voltage detection: Vdet1)	VCC falls (voltage detection: Vdet1)
Voltage-monitoring reset 2	VCC falls (voltage detection: Vdet2)	VCC falls (voltage detection: Vdet2)
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	The independent watchdog timer underflows.	The independent watchdog timer underflows or a refresh error occurs.
Watchdog timer reset	The watchdog timer overflows.	The watchdog timer underflows or a refresh error occurs.
Software reset	—	Register setting

Table 2.6 Comparison of Resets Registers

Register	Bit	RX62T	RX72T
RSTSR	—	Reset status register	—
RSTSR0	—	—	Reset status register 0
RSTSR1	—	—	Reset status register 1
RSTSR2	—	—	Reset status register 2
RSTCSR	—	Reset control/status register	—
IWDTSR	—	IWDT status register	—
SWRR	—	—	Software reset register

2.5 Voltage Detection Circuit

Table 2.7 is a comparative overview of voltage detection circuit, and Table 2.8 is a comparison of voltage detection circuit registers.

Table 2.7 Comparative Overview of Voltage Detection Circuit

Item		RX62T (LVD)		RX72T (LVDA)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detected event	Voltage drops past Vdet1.	Voltage drops past Vdet2.	Voltage drops past Vdet0.	Voltage rises or drops past Vdet1.	Voltage rises or drops past Vdet2.
	Detection voltage	One level only	One level only	Selectable between two different levels using OFS1.VDSEL [1:0] bits	Selectable between five different levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable between five different levels using LVDLVLR. LVD2LVL[3:0] bits
	Monitoring flag	No	No	No	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1.	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2.
		RSTSR.LVD1F flag: Vdet1 passage detection	RSTSR.LVD2F flag: Vdet2 passage detection	No	LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection
Processing upon voltage detection	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet1 > VCC; CPU restart after specified duration of VCC > Vdet1	Reset when Vdet2 > VCC; CPU restart after specified duration of Vdet2 > VCC	Reset when Vdet0 > VCC; CPU restart after specified duration of VCC > Vdet0	Reset when Vdet1 > VCC; CPU restart timing selectable: after specified duration of VCC > Vdet1 or after specified duration of Vdet1 > VCC	Reset when Vdet2 > VCC; CPU restart timing selectable: after specified duration of VCC > Vdet2 or after specified duration of Vdet2 > VCC

Item		RX62T (LVD)		RX72T (LVDA)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Processing upon voltage detection	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	No	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Non-maskable interrupt	Non-maskable interrupt		Non-maskable interrupt or maskable interrupt, selectable	Non-maskable interrupt or maskable interrupt, selectable
		Interrupt request when Vdet1 > VCC	Interrupt request when Vdet2 > VCC		Interrupt request both when Vdet1 > VCC and when VCC > Vdet1, or when one or the other occurs	Interrupt request both when Vdet2 > VCC and when VCC > Vdet2, or when one or the other occurs
Digital filter	Enabled/ disabled switching	No digital filter function	No digital filter function	No digital filter function	Yes	Yes
	Sampling time	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		No	No	No	Yes Output of event signal at detection of Vdet passage	Yes Output of event signal at detection of Vdet passage

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX62T (LVD)	RX72T (LVDA)
RSTSR	—	Reset status register	—
LVDKEYR	—	Key code register for low-voltage detection control register	—
LVDCR	—	Low-voltage detection control register	—
LVD1CR1	—	—	Voltage monitoring 1 circuit control register 1
LVD1SR	—	—	Voltage monitoring 1 circuit status register
LVD2CR1	—	—	Voltage monitoring 2 circuit control register 1
LVD2SR	—	—	Voltage monitoring 2 circuit status register
LVCMPCR	—	—	Voltage monitoring circuit control register
LVDLVLR	—	—	Voltage detection level select register
LVD1CR0	—	—	Voltage monitoring 1 circuit control register 0
LVD2CR0	—	—	Voltage monitoring 2 circuit control register 0

2.6 Clock Generation Circuit

Table 2.9 is a comparative overview of clock generation circuit, and Table 2.10 is a comparison of clock generation circuit registers.

Table 2.9 Comparative Overview of Clock Generation Circuit

Item	RX62T	RX72T
Use	• Generates the system clock (ICLK) supplied to the CPU, DTC, MTU3, GPT ROM, and RAM.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the RSPI, SCIi, MTU3 (internal peripheral buses), GPTW (internal peripheral buses), and HRPWM (internal peripheral buses).
	• Generates the peripheral module clock (PCLK) supplied to the peripheral modules.	• Generates the peripheral module clock (PCLKB) supplied to peripheral modules. • Generates the counter reference clock for the peripheral module supplied to the MTU3 and GPTW and the reference clock (PCLKC) for the HRPWM. • Generates the peripheral module clocks (for analog conversion) (PCLKD) supplied to S12AD. • Generates the flash-IF clock (FCLK) supplied to the flash interface. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the USB clock (UCLK) supplied to the USBb. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN.
	• Generates the on-chip oscillator clock (IWDTCLK) supplied to the IWDT.	• Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.

Item	RX62T	RX72T
Operating frequency	• ICLK: 8 to 100 MHz • PCLK: 8 to 50 MHz • IWDTCLK: 125 kHz (typ.) • Clock frequency setting limit: ICLK ≥ PCLK recommended	• ICLK: 200 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 200 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same as clocks from respective oscillators. • CANMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz • Clock frequency setting limit: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB
Main clock oscillator	• Resonator frequency: 8 MHz to 12.5 MHz • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock oscillator, the clock source is switched to the internal oscillator, and the MTU3 and GPT pins are driven high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop is detected on the main clock, the system clock source is switched to LOCO, and MTU3 and GPTW output can be forcedly driven high-impedance.
PLL frequency synthesizer	• Input clock source: Main clock • Input pulse frequency division ratio: 1 • Input frequency: 8 MHz to 12.5 MHz • Frequency multiplication ratio: 8 • Output clock frequency: 64 MHz to 100 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable among 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	—	• Selectable among 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 240 kHz

Item	RX62T	RX72T
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
Control of output on BCLK pin	—	• Selectable between BCLK clock output or high output • Selectable between BCLK or BCLK/2
Event link function (output)	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX62T	RX72T
SCKCR	—	System clock control register	System clock control register
		Initial values after a reset are different.	
	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
	PCK[3:0]	Peripheral module clock select bits	—
	PCKB[3:0]	—	Peripheral module clock B (PCLKB) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	BCK[3:0]	—	External bus clock (BCLK) select bits
	PSTOP1	—	BCLK pin output control bit
	ICK[3:0]	System clock select bits b27 b24 0 0 0 0: ×8 0 0 0 1: ×4 0 0 1 0: ×2 0 0 1 1: ×1 Settings other than the above are prohibited.	System clock (ICLK) select bits b27 b24 0 0 0 0: 1/1 0 0 0 1: 1/2 0 0 1 0: 1/4 0 0 1 1: 1/8 0 1 0 0: 1/16 0 1 0 1: 1/32 0 1 1 0: 1/64 Settings other than the above are prohibited.
	FCK[3:0]	—	FlashIF clock (FCLK) select bits
MEMWAIT	—	—	Memory wait cycle setting register
SCKCR2	—	—	System clock control register 2
SCKCR3	—	—	System clock control register 3
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2
BCKCR	—	—	External bus clock control register
MOSCCR	—	—	Main clock oscillator control register
LOCOCR	—	—	Low-speed on-chip oscillator control register
ILOCOCR	—	—	IWDT-dedicated on-chip oscillator control register
HOCOCR	—	—	High-speed on-chip oscillator control register
HOCOCR2	—	—	High-speed on-chip oscillator control register 2
OSCOVFSR	—	—	Oscillation stabilization flag register
OSTDCR	OSTDIE	—	Oscillation stop detection interrupt enable bit
	OSTDF	Oscillation stop detection flag	—
	KEY[7:0]	OSTDCR key code	—
OSTDSR	—	—	Oscillation stop detection status register
MOSCWTCR	—	—	Main clock oscillator wait control register

Register	Bit	RX62T	RX72T
MOFCR	—	—	Main clock oscillator function control register
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register

2.7 Low Power Consumption

Table 2.11 is a comparative overview of low power consumption, Table 2.12 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.13 is a comparison of low power consumption registers.

Table 2.11 Comparative Overview of Low Power Consumption

Item	RX62T	RX72T
Reduced power consumption by switching clocks	The frequency division ratio is settable independently for the system clock (ICLK) and peripheral module clocks (PCLK).	The frequency division ratio is settable independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	—	It is possible to select between BCLK output and high output.
Module stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	It is possible to transition to low power consumption modes that stop the CPU, peripheral modules, and oscillator.	It is possible to transition to low power consumption modes that stop the CPU, peripheral modules, and oscillator.
Low power consumption function	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode

Table 2.12 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX72T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	Operation	Operation possible
	PLL	Operation	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM, ECCRAM: RX72T	Operation (retained)	Operation possible (retained)
	Flash memory	Operation	Operation
	USB 2.0 Host/Function module (USBb)	—	Operation possible
	Watchdog timer (WDT: RX62T, WDTA: RX72T)	Operation	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX72T)	Operation	Operation possible
	Port output enable (POE3: RX62T, POE3B: RX72T)	Operation possible	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	—	Operation possible
	Voltage detection circuit	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	Operation	Operation possible
	PLL	Operation	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM, ECCRAM: RX72T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX72T
All-module clock stop mode	USB 2.0 Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDT: RX62T, WDTA: RX72T)	Operation	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX72T)	Operation	Operation possible
	Port output enable (POE3: RX62T, POE3B: RX72T)	Operation possible*1	Operation possible*1
	8-bit timer (unit 0, unit 1) (TMR)	—	Operation possible
	Voltage detection circuit	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	Stopped	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM, ECCRAM: RX72T	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	—	Stopped
	Watchdog timer (WDT: RX62T, WDTA: RX72T)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX72T)	Stopped (retained)	Operation possible
	Port output enable (POE3: RX62T, POE3B: RX72T)	Stopped (retained)	Stopped (retained)
	8-bit timer (unit 0, unit 1) (TMR)	—	Stopped (retained)
	Voltage detection circuit	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX62T	RX72T
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (reset processing)	Program execution state (reset processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	—	Stopped
	Low-speed on-chip oscillator	—	Stopped
	IWDT-dedicated on-chip oscillator	Stopped	Stopped (undefined)
	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	On-chip RAM (0000 0000h to 0000 3FFFh): RX62T RAM, ECCRAM: RX72T	Stopped (undefined)	Stopped (undefined)
	Flash memory	Stopped (retained)	Stopped (retained)
	USB 2.0 Host/Function module (USBb)	—	Stopped (undefined)
	Watchdog timer (WDT: RX62T, WDTA: RX72T)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT: RX62T, IWDTa: RX72T)	Stopped (undefined)	Stopped (undefined)
	Port output enable (POE3: RX62T, POE3B: RX72T)	Stopped (undefined)	Stopped (undefined)
	8-bit timer (unit 0, unit 1) (TMR)	—	Stopped (undefined)
	Voltage detection circuit	Operation	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

Notes: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

1. If POE interrupts are enabled and a POE interrupt source occurs while the chip is in all-module clock stop mode, return from all-module clock stop mode does not occur but the state of the interrupt source flag is retained. If a different source initiates return from all-module clock stop mode in this state, the POE interrupt is generated after the return.

Table 2.13 Comparison of Low Power Consumption Registers

Register	Bit	RX62T	RX72T
SBYCR	STS[4:0]	Standby timer select bits	—
	OPE	—	Output port enable bit
MSTPCRA	MSTPA2	—	8-bit timer 7/6 (unit 3) module stop bit
	MSTPA3	—	8-bit timer 5/4 (unit 2) module stop bit
	MSTPA4	—	8-bit timer 3/2 (unit 1) module stop bit
	MSTPA5	—	8-bit timer 1/0 (unit 0) module stop bit
	MSTPA7	General PWM timer module stop bit	General PWM timer/high resolution PWM/GPTW-dedicated port output enable module stop bit
	MSTPA19	—	12-bit D/A converter module stop bit
	MSTPA23	10-bit A/D converter module stop bit	12-bit A/D converter (unit 2) module stop bit
	MSTPA24	12-bit A/D converter control section module stop bit	Module stop A24 bit
	MSTPA27	—	Module stop A27 bit
	MSTPA28	Data transfer controller module stop bit	DMA controller/data transfer controller module stop bit
	MSTPA29	—	Module stop A29 bit
MSTPCRB	MSTPB4	—	Serial communication interface 12 module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB7	LIN module stop bit	—
	MSTPB9	—	Event link controller module stop bit
	MSTPB10	—	Comparator C module stop bit
	MSTPB19	—	Universal serial bus 2.0 FS interface module stop bit
	MSTPB25	—	Serial communication interface 6 module stop bit
	MSTPB26	—	Serial communication interface 5 module stop bit
	MSTPB29	Serial communication interface 2 module stop bit	—
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC6	—	ECCRAM module stop bit
	MSTPC19	—	CAC module stop bit
	MSTPC24	—	Serial communication interface 11 module stop bit
	MSTPC26	—	Serial communication interface 9 module stop bit
	MSTPC27	—	Serial communication interface 8 module stop bit
MSTPCRD	—	—	Module stop control register D
RSTCKCR	—	—	Sleep mode return clock source switching register

Register	Bit	RX62T	RX72T
DPSBYCR	—	Deep standby control register	Deep standby control register
		Initial values after a reset are different.	
DPSWCR	—	Deep standby wait control register	—
DPSIER	—	Deep standby interrupt enable register	—
DPSIER0	—	—	Deep standby interrupt enable register 0
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	Deep standby interrupt enable register 2
DPSIFR	—	Deep standby interrupt flag register	—
DPSIFR0	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	Deep standby interrupt flag register 2
DPSIEGR	—	Deep standby interrupt edge register	—
DPSIEGR0	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	Deep standby interrupt edge register 2
RSTSR	—	Reset status register	—

2.8 Exception Handling

Table 2.14 is a comparative listing of vectors, and Table 2.15 is a comparative listing of instructions for returning from exception handling routines.

Table 2.14 Comparison of Vectors

Item		RX62T	RX72T
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception (RX62T)/ single-precision floating-point exception (RX72T)		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.15 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX62T	RX72T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception (RX62T)/ single-precision floating-point exception (RX72T)		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.9 Interrupt controller

Table 2.16 is a comparative overview of interrupt controller, and Table 2.17 is a comparison of interrupt controller registers.

Table 2.16 Comparative Overview of Interrupt Controller

Item		RX62T (ICU)	RX72T (ICUC)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Number of sources: 101 • Interrupt detection: Edge detection/level detection The detection method is predetermined for each connected peripheral module source.	• Interrupts from peripheral modules • Number of sources: 256 • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupts: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1 interrupts: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	Interrupts from pins IRQ7 to IRQ0 • Number of sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or rising and falling edges	Interrupts by input signals on IRQi pins (i = 0 to 15) • Number of sources: 16 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• Interrupt generation by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	Specification of priority by means of register setting	The priority level is set by writing to interrupt source priority register r (IPRr) (r = 000 to 255).

Item		RX62T (ICU)	RX72T (ICUC)
Interrupts	Fast interrupt function	Faster CPU interrupt processing can be specified for a single interrupt source only.	The CPU's interrupt response time can be reduced. This setting can be used for one interrupt source only.
	DTC control	• An interrupt source can be used to start the DTC. • Number of DTC activating sources: 87 (78 peripheral function interrupts + 8 external pin interrupts + 1 software interrupt)	• An interrupt source can be used to start the DTC. • Number of DTC activating sources: 129 (111 peripheral function interrupts + 16 external pin interrupts + 2 software interrupts)
	DMAC control	—	An interrupt source can be used to start the DMAC.
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Voltage monitoring interrupt	Interrupt at detection of drop in power supply voltage	Interrupt from voltage detection circuit 1 (LVD1) or voltage detection circuit 2 (LVD2) at detection of power supply voltage rise or drop
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt occurs at detection of main clock oscillation having stopped.
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	—	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.
Return from low power consumption state	Sleep mode	Exit sleep mode by non-maskable interrupt, any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by non-maskable interrupt, interrupt IRQ7 to IRQ0, or WDT interrupt.	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral function interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, USB resume, IWDT, or TMR0 to TMR3).
	Software standby mode	Exit software standby mode by non-maskable interrupt or interrupt IRQ7 to IRQ0.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral function interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, or IWDT).

Item		RX62T (ICU)	RX72T (ICUC)
Return from low power consumption state	Deep software standby mode	Exit deep software standby mode by NMI pin interrupt, external interrupt, and any of certain external pin interrupts (voltage monitoring).	Exit deep software standby mode by NMI pin interrupt, any of certain external pin interrupts, or peripheral function interrupt (voltage monitoring 1 or voltage monitoring 2).

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX62T (ICU)	RX72T (ICUC)
IRn*1	—	Interrupt request register n (n = 016 to 254)	Interrupt request register n (n = 016 to 255)
IPRm*1	—	Interrupt source priority register m (m = 00h to 90h)	Interrupt source priority register m (m = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC activation enable register n (n = 027 to 254)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	—	DMAC trigger select register m (m = 0 to 7)
IRQCRn	—	IRQ control register n (n = 0 to 7)	IRQ control register n (n = 0 to 15)
IRQFLTE0	—	—	IRQ pin digital filter enable register 0
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	—	—	IRQ pin digital filter setting register 0
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	LVDST	Voltage-monitoring interrupt detection status flag	—
	OSTST	Oscillation stop detection interrupt status flag (b2)	Oscillation stop detection interrupt status flag (b1)
	WDTST	—	WDT underflow/refresh error status flag
	IWDTST	—	IWDT underflow/refresh error status flag
	LVD1ST	—	Voltage monitoring 1 interrupt status flag
	LVD2ST	—	Voltage monitoring 2 interrupt status flag
	RAMST	—	RAM error interrupt status flag

Register	Bit	RX62T (ICU)	RX72T (ICUC)
NMIER	LVDEN	Voltage-monitoring interrupt enable bit	—
	OSTEN	Oscillation stop detection interrupt enable bit (b2)	Oscillation stop detection interrupt enable bit (b1)
	WDTEN	—	WDT underflow/refresh error enable bit
	IWDTEN	—	IWDT underflow/refresh error enable bit
	LVD1EN	—	Voltage monitoring 1 interrupt enable bit
	LVD2EN	—	Voltage monitoring 2 interrupt enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	OSTCLR	OST clear bit (b2)	OST clear bit (b1)
	WDTCLR	—	WDT clear bit
	IWDTCLR	—	IWDT clear bit
	LVD1CLR	—	LVD1 clear bit
	LVD2CLR	—	LVD2 clear bit
NMIFLTE	—	—	NMI pin digital filter enable register
NMIFLTC	—	—	NMI pin digital filter setting register
GRPBE0, GRPBL0/ GRPBL1, GRPAL0	—	—	Group BE0, BL0/BL1, and AL0 interrupt request registers
GENBE0, GENBL0/ GENBL1, GENAL0	—	—	Group BE0, BL0/BL1, and AL0 interrupt request enable registers
GCRBE0	—	—	Group BE0 interrupt clear register
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 12h)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register write protect register

Note: 1. On the RX62T Group N = 255 correspond to a reserved area.

2.10 Buses

Table 2.18 is a comparative overview of bus, and Table 2.19 is a comparison of bus registers.

Table 2.18 Comparative Overview of Bus

Item		RX62T	RX72T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to on-chip RAM	Connected to RAM
	Memory bus 2	Connected to on-chip ROM	Connected to code flash memory
	Memory bus 3	—	Connected to ECCRAM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (bus error monitoring section, interrupts, etc.) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (WDT, CMT, CRC, SCI, etc.) • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	—	• Connected to peripheral modules (USBb and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU3 and GPT) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (MTU3, GPTW, HRPWM, RSPI, and SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX62T	RX72T
Internal peripheral buses	Internal peripheral bus 5	—	Reserved area
	Internal peripheral bus 6	• Connected to on-chip ROM (P/E) and data flash memory • Operates in synchronization with the peripheral-module clock (PCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	—	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)

Table 2.19 Comparison of Bus Registers

Register	Bit	RX62T	RX72T
CSnCR	—	—	CSn control register (n = 0 to 3)
CSnREC	—	—	CSn recovery cycle setting register (n = 0 to 3)
CSRECEN	—	—	CS recovery cycle insertion enable register
CSnMOD	—	—	CSn mode register (n = 0 to 3)
CSnWCR1	—	—	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	—	CSn wait control register 2 (n = 0 to 3)
BEREN	TOEN	—	Timeout detection enable bit
BERSR1	TO	—	Timeout bit
BUSPRI	—	—	Bus priority control register

2.11 Memory-Protection Unit

Table 2.20 is a comparison of memory-protection unit registers.

Table 2.20 Comparison of Memory-Protection Unit Registers

Register	Bit	RX62T (MPU)	RX72T (MPU)
MPESTS	IA (RX62T) IMPER (RX72T)	Instruction memory-protection error generated bit	Instruction memory-protection error generated bit
	DA (RX62T) DMPER (RX72T)	Data memory-protection error generation bit	Data memory-protection error generation bit

2.12 Data Transfer Controller

Table 2.21 is a comparative overview of data transfer controller.

Table 2.21 Comparative Overview of Data Transfer Controller

Item	RX62T (DTC)	RX72T (DTCa)
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum repeat size is 256. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 255 data units.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Number of transfer channels	Ability to transfer data on number of channels corresponding to number of interrupt sources (transfer from the ICU by DTC activation request)	Equal to number of all interrupt sources that can start a DTC transfer.
Chain transfer function	• Data can be transferred on multiple channels by a single activation source (chain transfer). • Either executed when counter = 0 or always executed can be selected for chain transfer.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Transfer space	• 16 MB in short-address mode (within 00000000h to 007FFFFFh or FF800000h to FFFFFFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 00000000h to 007FFFFFh or FF800000h to FFFFFFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Bit length of single data unit: 8, 16, or 32 bits • Number of data units in a single block: 1 to 255 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt sources	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.

Item	RX62T (DTC)	RX72T (DTCa)
Event link function	—	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Read skip	Transfer information read skipping can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back skipping is supported when the transfer source address or transfer destination address is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

2.13 I/O Ports

Table 2.22 and Table 2.23 are comparative overviews of I/O ports specifications for each package, Table 2.24 is a comparison of I/O port functions, and Table 2.25 is a comparison of I/O port registers.

Table 2.22 Comparative Overview of I/O Ports on 100-Pin Packages (RX72T: With PGA Pseudo-Differential Input)

Item	RX62T (100-Pin)	RX72T (100-Pin)	
		With PGA Pseudo-Differential Input and USB Pin	With PGA Pseudo-Differential Input and Without USB Pin
PORT0	—	P00, P01	P00, P01
PORT1	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24, P27
PORT3	P30 to P33	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P52 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB6	PB0 to PB7
PORTD	PD0 to PD7	PD2 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5
PORTH	—	PH0, PH4	PH0, PH4

Table 2.23 Comparative Overview of I/O Ports on 100-Pin Packages (RX72T: Without PGA Pseudo-Differential Input)

Item	RX62T (100-Pin)	RX72T (100-Pin) (Without PGA Pseudo-Differential Input and USB Pin)
PORT0	—	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24
PORT3	P30 to P33	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5

Table 2.24 Comparison of I/O Port Functions

Item	Port Symbol	RX62T	RX72T
Input pull-up	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
Open-drain output	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7
	PORTB	PB1, PB2	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
Driving ability switching	PORT0	—	P00, P01
	PORT1	—	P10 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P37
	PORT4	—	P43, P47
	PORT5	—	P50 to P55
	PORT6	—	P60 to P65
	PORT7	—	P70 to P76
	PORT8	—	P80 to P82
	PORT9	—	P90 to P96
	PORTA	—	PA0 to PA7

Item	Port Symbol	RX62T	RX72T
Driving ability switching	PORTB	—	PB0 to PB7
	PORTC	—	PC0 to PC6
	PORTD	—	PD0 to PD7
	PORTE	—	PE0, PE1, PE3 to PE6
	PORTF	—	PF0 to PF3
	PORTG	—	PG0 to PG2
	PORTH	—	PH1 to PH3, PH5 to PH7
	PORTK	—	PK0 to PK2
5 V tolerant	PORTB	—	PB1, PB2
	PORTC	—	PC0
	PORTD	—	PD2

Table 2.25 Comparison of I/O Ports Registers

Register	Bit	RX62T	RX72T
DDR (RX62T) PDR (RX72T)	B0 to B7	Pn0 to Pn7 I/O select bits (n = 1 to 3, 7 to 9, A, B, D, E, and G)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to H, and K)
DR (RX62T) PODR (RX72T)	B0 to B7	Pn0 to Pn7 output data store bits (n = 1 to 3, 7 to 9, A, B, D, E, and G)	Pm0 to 7 output data store bits (m = 0 to 9, A to H, and K)
PORT (RX62T) PIDR (RX72T)	B0 to B7	Pn0 to Pn7 bits (n = 1 to 9, A, B, D, E, and G)	Pm0 to 7 bits (m = 0 to 9, A to H, and K)
PMR	—	—	Port mode register
ICR	—	Input buffer control register	—
PF8IRQ	—	Port function register 8	—
PF9IRQ	—	Port function register 9	—
PFAADC	—	Port function register A	—
PFCMTU	—	Port function register C	—
PFDGPT	—	Port function register D	—
PFFSCI	—	Port function register F	—
PFGSPI	—	Port function register G	—
PFHSPI	—	Port function register H	—
PFJCAN	—	Port function register J	—
PFKLIN	—	Port function register K	—
PFMPOE	—	Port function register M	—
PFNPOE	—	Port function register N	—
ODR0	—	—	Open drain control register 0
ODR1	—	—	Open drain control register 1
PCR	—	—	Pull-up resistor control register
DSCR	—	—	Driving ability control register
DSCR2	—	—	Driving ability control register 2

2.14 Multi-Function Timer Pulse Unit 3

Table 2.26 is a comparative overview of multi-function timer pulse unit 3, and Table 2.27 is a comparison of multi-function timer pulse unit 3 registers, and Table 2.28 and Table 2.29 are comparative listings of TPSC bit settings.

Table 2.26 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX62T (MTU3)	RX72T (MTU3d)
Pulse input/output	Max. 24 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clock	Six to eight clocks for each channel (four clocks for channel 5)	11 clocks for each channel (14 clocks for MTU0 and MTU9, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))
Operating frequency	8 to 100 MHz	Up to 200 MHz
Available operations	[MTU0 to MTU4, MTU6, and MTU7] • Waveform output at compare match • Input capture function • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing at compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, and MTU9] • Waveform output at compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing at compare match or input capture • Simultaneous input and output to registers in synchronization with counter operations • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, and MTU7] Buffer operation available	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU9] Buffer operation available
	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU 4 and MTU6/MTU7, positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset PWM operation. • In complementary PWM mode, values can be transferred from buffer registers to temporary registers at timer-counter peaks or troughs or when the buffer registers (MTU4.TGRD and MTU7.TGRD) are written to. • Double-buffering is selectable in complementary PWM mode.	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU 4 and MTU6/MTU7, positive and negative signals in six phases (12 phases in total) can be output in complementary PWM and reset-synchronized PWM operation. • In complementary PWM mode, values can be transferred from buffer registers to temporary registers at timer-counter peaks or troughs or when the buffer registers (MTU4.TGRD and MTU7.TGRD) are written to. • Double-buffering is selectable in complementary PWM mode.

Item	RX62T (MTU3)	RX72T (MTU3d)
Available operations	[MTU1, MTU2] • Phase counting mode can be specified independently • Cascade connection operation available	[MTU1, MTU2] • Phase counting mode can be specified independently • 32-bit phase counting mode can be specified for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available
	[MTU3, MTU4] A mode for driving AC synchronous motors (brushless DC motors) through interlocking with MTU0 and using complementary PWM output and reset PWM output is available, allowing selection between two types of waveform output (chopping or level).	[MTU3, MTU4] A mode for driving AC synchronous motors (brushless DC motors) through interlocking with MTU0 and using complementary PWM output and reset-synchronized PWM output is available, allowing selection between two types of waveform output (chopping or level).
	[MTU5] Ability to operate as a dead-time compensation counter	[MTU5] Ability to operate as a dead-time compensation counter
	—	[MTU6, MTU7] A mode for driving AC synchronous motors (brushless DC motors) through interlocking with MTU9 and using complementary PWM output and reset-synchronized PWM output is available, allowing selection between two types of waveform output (chopping or level).
Interrupt skipping function	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped.	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped.
Interrupt sources	38 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	A/D converter start triggers can be generated.	A/D converter start triggers can be generated.
	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output.	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output.
Low power consumption function	Ability to specify transition to module stop state	Ability to specify transition to module stop state
Complementary PWM mode	Only when using the double buffer function, a value of (output PWM duty value − 1) is set in the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)).	Only when using the double buffer function, a value of (output PWM duty value) is set in the buffer registers (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)).

Table 2.27 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register		Bit	RX62T (MTU3)	RX72T (MTU3d)
TCR		TPSC[2:0] TPSC[1:0]	Time prescaler select bits Refer to Table 2.28 and Table 2.29 for details.	Time prescaler select bits Refer to Table 2.28 and Table 2.29 for details.
TCR2		—	—	Timer control register 2
TMDR1		MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough) x: Don’t care	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Phase counting mode 5 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough) x: Don’t care
TMDR3		—	—	Timer mode register 3
TSR	TSR	TGFA	Input capture/output compare flag A	—
		TGFB	Input capture/output compare flag B	—
		TGFC	Input capture/output compare flag C	—
		TGFD	Input capture/output compare flag D	—
		TCFV	Overflow flag	—
		TCFU	Underflow flag	—
		CMFW5	Compare match/input capture flag W5	—
		CMFV5	Compare match/input capture flag V5	—
		CMFU5	Compare match/input capture flag U5	—
	TSR2	TGFE	Compare match flag E	—
		TGFF	Compare match flag F	—
TCNTLW		—	—	Timer longword counter

Register	Bit	RX62T (MTU3)	RX72T (MTU3d)
TGRALW, TGRBLW	—	—	Timer longword general registers
TSTRA	CST9	—	Counter start 9 bit
TSYRA	SYNC9	—	Timer synchronous operation 9 bit
TCSYSTR	SCH9	—	Synchronous start 9 bit
TGCRB	—	—	Timer gate control register
NFCRn	—	—	Noise filter control register n (n = 0 to 4, 6, 7, 9, C)
NFCR5	—	—	Noise filter control register 5
TADSTRGR0	—	—	A/D conversion start request select register 0
TADSTRGR1	—	—	A/D conversion start request select register 1

Table 2.28 Comparison of TPSC Bit Settings (Other Than MTU5)

	RX62T (MTU3)		RX72T (MTU3d)		
Channel	TCR. TPSC [2:0]	Description	TCR2. TPSC2 [2:0]	TCR. TPSC [2:0]	Description
MTU0 (RX62T) MTU0, MTU9 (RX72T)	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	External clock: counts on MTCLKC pin input	0 0 0	1 1 0	External clock: counts on MTCLKC pin input
	1 1 1	External clock: counts on MTCLKD pin input	0 0 0	1 1 1	External clock: counts on MTCLKD pin input
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Internal clock: counts on PCLKC/256
			1 0 1	x x x	Internal clock: counts on PCLKC/1024
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	External clock: counts on MTIOC1A pin input

Channel	RX62T (MTU3)		RX72T (MTU3d)		
	TCR. TPSC [2:0]	Description	TCR2. TPSC2 [2:0]	TCR. TPSC [2:0]	Description
MTU1	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	Internal clock: counts on ICLK/256	0 0 0	1 1 0	Internal clock: counts on PCLKC/256
	1 1 1	Counts on MTU2.TCNT overflow/underflow	0 0 0	1 1 1	Counts on MTU2.TCNT overflow/underflow
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Internal clock: counts on PCLKC/1024
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited
MTU2	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	External clock: counts on MTCLKA pin input	0 0 0	1 0 0	External clock: counts on MTCLKA pin input
	1 0 1	External clock: counts on MTCLKB pin input	0 0 0	1 0 1	External clock: counts on MTCLKB pin input
	1 1 0	External clock: counts on MTCLKC pin input	0 0 0	1 1 0	External clock: counts on MTCLKC pin input

Channel	RX62T (MTU3)		RX72T (MTU3d)		
	TCR. TPSC [2:0]	Description	TCR2. TPSC2 [2:0]	TCR. TPSC [2:0]	Description
MTU2	1 1 1	Internal clock: counts on ICLK/1024	0 0 0	1 1 1	Internal clock: counts on PCLKC/1024
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Internal clock: counts on PCLKC/256
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited
MTU3 MTU4 MTU6 MTU7	0 0 0	Internal clock: counts on ICLK/1	0 0 0	0 0 0	Internal clock: counts on PCLKC/1
	0 0 1	Internal clock: counts on ICLK/4	0 0 0	0 0 1	Internal clock: counts on PCLKC/4
	0 1 0	Internal clock: counts on ICLK/16	0 0 0	0 1 0	Internal clock: counts on PCLKC/16
	0 1 1	Internal clock: counts on ICLK/64	0 0 0	0 1 1	Internal clock: counts on PCLKC/64
	1 0 0	Internal clock: counts on ICLK/256	0 0 0	1 0 0	Internal clock: counts on PCLKC/256
	1 0 1	Internal clock: counts on ICLK/1024	0 0 0	1 0 1	Internal clock: counts on PCLKC/1024
	1 1 0	External clock: counts on MTCLKA pin input*1	0 0 0	1 1 0	External clock: counts on MTCLKA pin input
	1 1 1	External clock: counts on MTCLKB pin input*1	0 0 0	1 1 1	External clock: counts on MTCLKB pin input
			0 0 1	x x x	Internal clock: counts on PCLKC/2
			0 1 0	x x x	Internal clock: counts on PCLKC/8
			0 1 1	x x x	Internal clock: counts on PCLKC/32
			1 0 0	x x x	Setting prohibited
			1 0 1	x x x	Setting prohibited
			1 1 0	x x x	Setting prohibited
			1 1 1	x x x	Setting prohibited

x: Don't care

Note: 1. This setting is not available on MTU6 or MTU7.

Table 2.29 Comparison of TPSC Bit Settings (MTU5)

	RX62T (MTU3)		RX72T (MTU3d)		
Channel	TCR. TPSC [1:0]	Description	TCR2. TPSC2 [2:0]	TCR. TPSC [1:0]	Description
MTU5	0 0	Internal clock: counts on ICLK/1	0 0 0	0 0	Internal clock: counts on PCLKC/1
	0 1	Internal clock: counts on ICLK/4	0 0 0	0 1	Internal clock: counts on PCLKC/4
	1 0	Internal clock: counts on ICLK/16	0 0 0	1 0	Internal clock: counts on PCLKC/16
	1 1	Internal clock: counts on ICLK/64	0 0 0	1 1	Internal clock: counts on PCLKC/64
			0 0 1	x x	Internal clock: counts on PCLKC/2
			0 1 0	x x	Internal clock: counts on PCLKC/8
			0 1 1	x x	Internal clock: counts on PCLKC/32
			1 0 0	x x	Internal clock: counts on PCLKC/256
			1 0 1	x x	Internal clock: counts on PCLKC/1024
			1 1 0	x x	Setting prohibited
			1 1 1	x x	External clock: counts on MTIOC1A pin input

x: Don’t care

2.15 Port Output Enable 3

Table 2.30 is a comparative overview of port output enable 3, and Table 2.31 is a comparison of port output enable 3 registers.

Table 2.30 Comparative Overview of Port Output Enable 3

Item	RX62T (POE3)	RX72T (POE3B)
Functions	• Input pins POE0#, POE4#, POE8#, POE10#, and POE11# can each be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low sampling.	• The POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins can each be set to falling-edge or low-level detection. When low-level detection is specified, a sampling clock can be selected among PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the number of samples can be selected among four, eight, or 16.
	• MTU complementary PWM output pins, MTU0, and GPT pins can be placed in the high-impedance state by POE0#, POE4#, POE8#, POE10#, or POE11# pin falling-edge or low sampling.	• Output on all control target pins can be disabled at detection of falling-edge or low-level input on the POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, and POE14# pins.
	• MTU complementary PWM output pins, MTU0, and GPT pins can be placed in the high-impedance state when the oscillation stop detection circuit in the clock pulse generator detects stopped oscillation.	• Output on all control target pins can be disabled when oscillation stop is detected by the oscillation stop detection function of the clock generator.
	• MTU complementary PWM output pins or GPT large-current output pins can be placed in the high-impedance state when the output levels of MTU complementary PWM output pins or GPT large-current output pins are compared and simultaneous active-level output continues for one cycle or more.	• MTU complementary PWM output pins can be disabled when output levels of MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • The GPTW output pins can be disabled when output levels of GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 to GPTW9 pins) are compared and simultaneous active-level output continues for one cycle or more.
	• MTU complementary PWM output pins, MTU0, and GPT pins can be placed in the high-impedance state in response to comparator detection by the 12-bit A/D converter (S12ADA).	• Output on all control target pins can be disabled in response to comparator C (CMPC) output detection.
	• MTU complementary PWM output pins, MTU0, and GPT pins can be placed in the high-impedance state by modifying the settings of the POE3 registers.	• Output on all control target pins can be disabled by modifying the settings of the POE registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated by input-level sampling or output-level comparison results.
Pin status while output is disabled	High-impedance	• High-impedance • General I/O port

Item	RX62T (POE3)	RX72T (POE3B)
Output disable control target pins	• MTU output pins — MTU0 pin (MTIOC0A-A, MTIOC0A-B, MTIOC0B-A, MTIOC0B-B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins — GPT0 pin (GTIOC0A-A, GTIOC0B-A, GTIOC0A-B, GTIOC0B-B) — GPT1 pin (GTIOC1A-A, GTIOC1B-A, GTIOC1A-B, GTIOC1B-B) — GPT2 pin (GTIOC2A-A, GTIOC2B-A, GTIOC2A-B, GTIOC2B-B) — GPT3 pin (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pin (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pin (GTIOC0A, GTIOC0B) — GPTW1 pin (GTIOC1A, GTIOC1B) — GPTW2 pin (GTIOC2A, GTIOC2B) — GPTW3 pin (GTIOC3A, GTIOC3B) — GPTW4 pin (GTIOC4A, GTIOC4B) — GPTW5 pin (GTIOC5A, GTIOC5B) — GPTW6 pin (GTIOC6A, GTIOC6B) — GPTW7 pin (GTIOC7A, GTIOC7B) — GPTW8 pin (GTIOC8A, GTIOC8B) — GPTW9 pin (GTIOC9A, GTIOC9B)

Item	RX62T (POE3)	RX72T (POE3B)
Conditions for generating output disable request	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11#. • Short circuit of output pins: Output of one of the combinations listed below A match (short circuit) of signal levels lasting one or more cycles on a combination of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A-A and GTIOC0B-A — GTIOC1A-A and GTIOC1B-A — GTIOC2A-A and GTIOC2B-A • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator • Detection of output from 12-bit A/D converter (S12ADA)	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, or POE14# • Short circuit of output pins: Output of one of the combinations listed below A match (short circuit) of signal levels lasting one or more cycles on a combination of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B — GTIOC8A and GTIOC8B — GTIOC9A and GTIOC9B • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output

Table 2.31 Comparison of Port Output Enable 3 Registers

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR1	POE0M[1:0] (RX62T) POE0M[3:0] (RX72T)	POE0 mode select bits (b1, b0) b1 b0 0 0: Accepts a request at the falling edge of the POE0# input. 0 1: Accepts a request when the POE0# input has been sampled at low level 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the POE0# input has been sampled at low level 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the POE0# input has been sampled at low level 16 times at PCLK/128 clock pulses and all are low level.	POE0 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request at the falling edge of the POE0# pin input. 0 0 0 1: Samples the level of the POE0# pin input at PCLK/8, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 0: Samples the level of the POE0# pin input at PCLK/16, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 1: Samples the level of the POE0# pin input at PCLK/128, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 0: Samples the level of the POE0# pin input at PCLK, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 1: Samples the level of the POE0# pin input at PCLK/2, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 1 0: Samples the level of the POE0# pin input at PCLK/4, and accepts a request when consecutive low-level results are detected the specified number of times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	POE0 sampling count select bits

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR1	POE0F	POE0 flag [Setting condition] When the input set by the POE0M[1:0] bits occurs on the POE0# pin [Clearing condition] When 0 is written to the POE0F flag after reading it as 1	POE0 flag [Setting condition] When the input set by the POE0M[3:0] and POE0M2[3:0] bits occurs on the POE0# pin [Clearing condition] When 0 is written to the POE0F flag after reading it as 1 When low-level sampling is specified by the POE0M[3:0] bits, a high level signal needs to be input on the POE0# pin to write 0 to this flag.
ICSR2	POE4M[1:0] (RX62T) POE4M[3:0] (RX72T)	POE4 mode select bits (b1, b0) b1 b0 0 0: Accepts a request at the falling edge of the POE4# input. 0 1: Accepts a request when the POE4# input has been sampled at low level 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the POE4# input has been sampled at low level 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the POE4# input has been sampled at low level 16 times at PCLK/128 clock pulses and all are low level.	POE4 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request at the falling edge of the POE4# pin input. 0 0 0 1: Samples the level of the POE4# pin input at PCLK/8, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 0: Samples the level of the POE4# pin input at PCLK/16, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 1: Samples the level of the POE4# pin input at PCLK/128, and accepts a request when consecutive low-level results are detected the specified number of times.

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR2	POE4M[1:0] (RX62T) POE4M[3:0] (RX72T)		0 1 0 0: Samples the level of the POE4# pin input at PCLK, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 1: Samples the level of the POE4# pin input at PCLK/2, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 1 0: Samples the level of the POE4# pin input at PCLK/4, and accepts a request when consecutive low-level results are detected the specified number of times. Settings other than the above are prohibited.
	POE4M2[3:0]	—	POE4 sampling count select bits
	POE4F	POE4 flag [Setting condition] When the input set by the POE4M[1:0] bits occurs on the POE4# pin [Clearing condition] When 0 is written to the POE4F flag after reading it as 1	POE4 flag [Setting condition] When the input set by the POE4M[3:0] and POE4M2[3:0] bits occurs on the POE4# pin [Clearing condition] When 0 is written to the POE4F flag after reading it as 1 When low-level sampling is specified by the POE4M[3:0] bits, a high level signal needs to be input on the POE4# pin to write 0 to this flag.
ICSR3	POE8M[1:0] (RX62T) POE8M[3:0] (RX72T)	POE8 mode select bits (b1, b0) b1 b0 0 0: Accepts a request at the falling edge of the POE8# input. 0 1: Accepts a request when the POE8# input has been sampled at low level 16 times at PCLK/8 clock pulses and all are low level.	POE8 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request at the falling edge of the POE8# pin input. 0 0 0 1: Samples the level of the POE8# pin input at PCLK/8, and accepts a request when consecutive low-level results are detected the specified number of times.

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR3	POE8M[1:0] (RX62T) POE8M[3:0] (RX72T)	1 0: Accepts a request when the POE8# input has been sampled at low level 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the POE8# input has been sampled at low level 16 times at PCLK/128 clock pulses and all are low level.	0 0 1 0: Samples the level of the POE8# pin input at PCLK/16, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 1: Samples the level of the POE8# pin input at PCLK/128, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 0: Samples the level of the POE8# pin input at PCLK, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 1: Samples the level of the POE8# pin input at PCLK/2, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 1 0: Samples the level of the POE8# pin input at PCLK/4, and accepts a request when consecutive low-level results are detected the specified number of times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	POE8 sampling count select bits
	POE8F	POE8 flag [Setting condition] When the input set by the POE8M[1:0] bits occurs on the POE8# pin [Clearing condition] When 0 is written to the POE8F flag after reading it as 1	POE8 flag [Setting condition] When the input set by the POE8M[3:0] and POE8M2[3:0] bits occurs on the POE8# pin [Clearing condition] When 0 is written to the POE8F flag after reading it as 1 When low-level sampling is specified by the POE8M[3:0] bits, a high level signal needs to be input on the POE8# pin to write 0 to this flag.

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR4	POE10M[1:0] (RX62T) POE10M[3:0] (RX72T)	POE10 mode select bits (b1, b0) b1 b0 0 0: Accepts a request at the falling edge of the POE10# input. 0 1: Accepts a request when the POE10# input has been sampled at low level 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the POE10# input has been sampled at low level 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the POE10# input has been sampled at low level 16 times at PCLK/128 clock pulses and all are low level.	POE10 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request at the falling edge of the POE10# pin input. 0 0 0 1: Samples the level of the POE10# pin input at PCLK/8, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 0: Samples the level of the POE10# pin input at PCLK/16, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 1: Samples the level of the POE10# pin input at PCLK/128, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 0: Samples the level of the POE10# pin input at PCLK, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 1: Samples the level of the POE10# pin input at PCLK/2, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 1 0: Samples the level of the POE10# pin input at PCLK/4, and accepts a request when consecutive low-level results are detected the specified number of times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	POE10 sampling count select bits

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR4	POE10F	POE10 flag [Setting condition] When the input set by the POE10M[1:0] bits occurs on the POE10# pin [Clearing condition] When 0 is written to the POE10F flag after reading it as 1	POE10 flag [Setting condition] When the input set by the POE10M[3:0] and POE10M2[3:0] bits occurs on the POE10# pin [Clearing condition] When 0 is written to the POE10F flag after reading it as 1 When low-level sampling is specified by the POE10M[3:0] bits, a high level signal needs to be input on the POE10# pin to write 0 to this flag.
ICSR5	POE11M[1:0] (RX62T) POE11M[3:0] (RX72T)	POE11 mode select bits (b1, b0) b1 b0 0 0: Accepts a request at the falling edge of the POE11# input. 0 1: Accepts a request when the POE11# input has been sampled at low level 16 times at PCLK/8 clock pulses and all are low level. 1 0: Accepts a request when the POE11# input has been sampled at low level 16 times at PCLK/16 clock pulses and all are low level. 1 1: Accepts a request when the POE11# input has been sampled at low level 16 times at PCLK/128 clock pulses and all are low level.	POE11 mode select bits (b3 to b0) b3 b0 0 0 0 0: Accepts a request at the falling edge of the POE11# pin input. 0 0 0 1: Samples the level of the POE11# pin input at PCLK/8, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 0: Samples the level of the POE11# pin input at PCLK/16, and accepts a request when consecutive low-level results are detected the specified number of times. 0 0 1 1: Samples the level of the POE11# pin input at PCLK/128, and accepts a request when consecutive low-level results are detected the specified number of times.

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ICSR5	POE11M[1:0] (RX62T) POE11M[3:0] (RX72T)		0 1 0 0: Samples the level of the POE11# pin input at PCLK, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 0 1: Samples the level of the POE11# pin input at PCLK/2, and accepts a request when consecutive low-level results are detected the specified number of times. 0 1 1 0: Samples the level of the POE11# pin input at PCLK/4, and accepts a request when consecutive low-level results are detected the specified number of times. Settings other than the above are prohibited.
	POE11M2[3:0]	—	POE11 sampling count select bits
	POE11F	POE11 flag [Setting condition] When the input set by the POE11M[1:0] bits occurs on the POE11# pin [Clearing condition] When 0 is written to the POE11F flag after reading it as 1	POE11 flag [Setting condition] When the input set by the POE11M[3:0] and POE11M2[3:0] bits occurs on the POE11# pin [Clearing condition] When 0 is written to the POE11F flag after reading it as 1 When low-level sampling is specified by the POE11M[3:0] bits, a high level signal needs to be input on the POE11# pin to write 0 to this flag.
ICSR6	—	—	Input level control/status register 6
ICSR7	—	—	Input level control/status register 7
ICSR8	—	—	Input level control/status register 8
ICSR9	—	—	Input level control/status register 9
ICSR10	—	—	Input level control/status register 10

Register	Bit	RX62T (POE3)	RX72T (POE3B)
OCSR1	OSF1	Output short flag 1 This flag indicates that one or more of the three pairs of two-phase outputs among MTU complementary PWM output pins (pins MTU3 and MTU4) or GPT large-current output pins (GPT0 to GPT2) to be compared has simultaneously been at active level. [Setting condition] When any one of the three pairs of two-phase outputs has simultaneously been at active level [Clearing condition] When 0 is written to the OSF1 flag after reading it as 1	Output short flag 1 This flag indicates that one or more of the three pairs of two-phase outputs among MTU complementary PWM output pins (pins MTU3 and MTU4) has simultaneously been at active level. However, if output disabling control for the corresponding pins is not enabled, this flag is not set to 1. [Setting condition] • When pins MTIOC3B and MTIOC3D simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU3BDZE bit, or at least one of bits PMMCR1.MTU3BME and PMMCR1.MTU3DME, is 1. • When pins MTIOC4A and MTIOC4C simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4ACZE bit, or at least one of bits PMMCR1.MTU4AME and PMMCR1.MTU4CME, is 1. • When pins MTIOC4B and MTIOC4D simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU4BDZE bit, or at least one of bits PMMCR1.MTU4BME and PMMCR1.MTU4DME, is 1. [Clearing condition] When 0 is written to the OSF1 flag after reading it as 1 To write 0 to this flag, the output on the MTU complementary PWM output pins must be at the inactive level.

Register	Bit	RX62T (POE3)	RX72T (POE3B)
OCSR2	OSF2	Output short flag 2 This flag indicates that one or more of the three pairs of two-phase outputs among MTU complementary PWM output pins (pins MTU6 and MTU7) has simultaneously been at active level. [Setting condition] When any one of the three pairs of two-phase outputs has simultaneously been at active level [Clearing condition] When 0 is written to the OSF2 flag after reading it as 1	Output short flag 2 This flag indicates that one or more of the three pairs of two-phase outputs among MTU complementary PWM output pins (pins MTU6 and MTU7) has simultaneously been at active level. However, if output disabling control for the corresponding pins is not enabled, this flag is not set to 1. [Setting condition] • When pins MTIOC6B and MTIOC6D simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU6BDZE bit, or at least one of bits PMMCR1.MTU6BME and PMMCR1.MTU6DME, is 1. • When pins MTIOC7A and MTIOC7C simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU7ACZE bit, or at least one of bits PMMCR1.MTU7AME and PMMCR1.MTU7CME, is 1. • When pins MTIOC7B and MTIOC7D simultaneously go to the active level for at least one cycle of PCLK while the value of the POECR2.MTU7BDZE bit, or at least one of bits PMMCR1.MTU7BME and PMMCR1.MTU7DME, is 1. [Clearing condition] When 0 is written to the OSF2 flag after reading it as 1 To write 0 to this flag, the output on the MTU complementary PWM output pins must be at the inactive level.
OCSR3	—	—	Output level control/status register 3
OCSR4	—	—	Output level control/status register 4
OCSR5	—	—	Output level control/status register 5

Register	Bit	RX62T (POE3)	RX72T (POE3B)
ALR1	OLSG0A	MTIOC3B/GTIOC0A-A active level setting bit	MTIOC3B pin active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B-A active level setting bit	MTIOC3D pin active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A-A active level setting bit	MTIOC4A pin active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B-A active level setting bit	MTIOC4C pin active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A-A active level setting bit	MTIOC4B pin active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B-A active level setting bit	MTIOC4D pin active level setting bit
ALR2	—	—	Active level register 2
ALR3	—	—	Active level register 3
ALR4	—	—	Active level register 4
ALR5	—	—	Active level register 5
SPOER	MTUCH34HIZ*1	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin output disable bit
	GPT01HIZ	GPT0 and GPT1 output high-impedance enable bit	GPTW0 and GPTW1 pin output disable bit
	GPT23HIZ	GPT2 and GPT3 output high-impedance enable bit	GPTW2 and GPTW3 pin output disable bit
	MTUCH9HIZ	—	MTU9 pin output disable bit
	GPT02HIZ	—	GPTW0 to GPTW2 pin output disable bit
	GPT46HIZ	—	GPTW4 to GPTW6 pin output disable bit
	GPT79HIZ	—	GPTW7 to GPTW9 pin output disable bit
POECR2	MTU4BDZE*1	MTU CH4BD high-impedance enable bit	MTIOC4B/MTIOC4D pin high-impedance enable bit
	MTU4ACZE*1	MTU CH4AC high-impedance enable bit	MTIOC4A/MTIOC4C pin high-impedance enable bit
	MTU3BDZE*1	MTU CH3BD high-impedance enable bit	MTIOC3B/MTIOC3D pin high-impedance enable bit
POECR3	—	Port output enable control register 3	Port output enable control register 3
		Initial values after a reset are different.	
	GPT2ABZE	GPT CH2AB high-impedance enable bit (b8)	GTIOC2A/GTIOC2B pin high-impedance enable bit (b2)
	GPT3ABZE	GPT CH3AB high-impedance enable bit (b9)	GTIOC3A/GTIOC3B pin high-impedance enable bit (b3)
	GPT4ABZE to GPT9ABZE	—	GTIOC4A/GTIOC4B to GTIOC9A/GTIOC9B pin high-impedance enable bit

Register	Bit	RX62T (POE3)	RX72T (POE3B)
POECR4	CMADDMT34ZE*1	MTUCH34 high-impedance CFLAG add bit	MTU3 and MTU4 output disabling condition CFLAG add bit
	IC1ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE0F add bit
	IC2ADDMT34ZE*1	MTUCH34 high-impedance POE4F add bit	MTU3 and MTU4 output disabling condition POE4F add bit
	IC3ADDMT34ZE*1	MTUCH34 high-impedance POE8F add bit	MTU3 and MTU4 output disabling condition POE8F add bit
	IC4ADDMT34ZE*1	MTUCH34 high-impedance POE10F add bit	MTU3 and MTU4 output disabling condition POE10F add bit
	IC5ADDMT34ZE*1	MTUCH34 high-impedance POE11F add bit	MTU3 and MTU4 output disabling condition POE11F add bit
	IC6ADDMT34ZE*1	—	MTU3 and MTU4 output disabling condition POE12F add bit
	IC8ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE9F add bit
	IC9ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE13F add bit
	IC10ADDMT34ZE	—	MTU3 and MTU4 output disabling condition POE14F add bit
	CMADDMT67ZE	MTUCH67 high-impedance CFLAG add bit	—
	IC1ADDMT67ZE	MTUCH67 high-impedance POE0F add bit	—
	IC3ADDMT67ZE	MTUCH67 high-impedance POE8F add bit	—
	IC4ADDMT67ZE	MTUCH67 high-impedance POE10F add bit	—
	IC5ADDMT67ZE	MTUCH67 high-impedance POE11F add bit	—
POECR4B	—	—	Port output enable control register 4B
POECR5	IC3ADDMT0ZE	—	MTU0 output disabling condition POE8F add bit
	IC6ADDMT0ZE	—	MTU0 output disabling condition POE12F add bit
	IC8ADDMT0ZE	—	MTU0 output disabling condition POE9F add bit
	IC9ADDMT0ZE	—	MTU0 output disabling condition POE13F add bit
	IC10ADDMT0ZE	—	MTU0 output disabling condition POE14F add bit
POECR6	IC4ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE10F add bit
	IC6ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE12F add bit
	IC8ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE9F add bit
	IC9ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE13F add bit

Register	Bit	RX62T (POE3)	RX72T (POE3B)
POECR6	IC10ADDGPT01ZE	—	GPTW0 and GPTW1 output disabling condition POE14F add bit
	CMADDGPT23ZE	GPTCH23 high-impedance CFLAG add bit	—
	IC1ADDGPT23ZE	GPTCH23 high-impedance POE0F add bit	—
	IC2ADDGPT23ZE	GPTCH23 high-impedance POE4F add bit	—
	IC3ADDGPT23ZE	GPTCH23 high-impedance POE8F add bit	—
	IC4ADDGPT23ZE	GPTCH23 high-impedance POE10F add bit	—
POECR6B	—	—	Port output enable control register 6B
POECR7	—	—	Port output enable control register 7
POECR8	—	—	Port output enable control register 8
POECR9	—	—	Port output enable control register 9
POECR10	—	—	Port output enable control register 10
POECR11	—	—	Port output enable control register 11
PMMCR0	—	—	Port mode mask control register 0
PMMCR1	—	—	Port mode mask control register 1
PMMCR2	—	—	Port mode mask control register 2
PMMCR3	—	—	Port mode mask control register 3
POECMPFR	—	—	Port output enable comparator output detection flag register
POECMPSEL	—	—	Port output enable comparator request select register
POECMPEXm		—	Port output enable comparator request extended selection register m (m = 0 to 8)
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2
M6SELR	—	—	MTU6 pin select register
M7SELR1	—	—	MTU7 pin select register 1
M7SELR2	—	—	MTU7 pin select register 2
M9SELR1	—	—	MTU9 pin select register 1
M9SELR2	—	—	MTU9 pin select register 2
G0SELR	—	—	GPTW0 pin select register
G1SELR	—	—	GPTW1 pin select register
G2SELR	—	—	GPTW2 pin select register
G3SELR	—	—	GPTW3 pin select register
G4SELR	—	—	GPTW4 pin select register
G5SELR	—	—	GPTW5 pin select register

Register	Bit	RX62T (POE3)	RX72T (POE3B)
G6SELR	—	—	GPTW6 pin select register
G7SELR	—	—	GPTW7 pin select register
G8SELR	—	—	GPTW8 pin select register
G9SELR	—	—	GPTW9 pin select register

Note: 1. The GPT and MTU pins are controlled by this register on the RX62T, but the GPT and MTU pins are controlled by separate registers on the RX72T.

2.16 General PWM Timer

Table 2.32 is a comparative overview of general PWM timers, Table 2.33 is a comparison of general PWM timer registers, and Table 2.34 is a comparative listing of GTIOA and GTIOB bit settings.

The GPTa is implemented on the RX62G Group only.

Table 2.32 Comparative Overview of General PWM Timer

Item	RX62T (GPT/GPTa)	RX72T (GPTW)
Functions	• 16 bits × 4 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter • Independently selectable clock source for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For each pair of output compare/input capture registers for each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use. • During output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Ability to synchronize operation with any of several counters • Synchronized operation modes (synchronized, or displaced by desired times for phase shifting) • Generation of dead time during PWM operation • Count start, count stop, or counter clearing by an external trigger • Output disable control by dead time error, detection of short-circuited output, or comparator-detection • A/D converter start trigger generation function	• 32 bits × 10 channels • Up-count or down-count operation (saw waves) or up/down-count operation (triangle waves) for each counter • Independently selectable clock source for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For each pair of output compare/input capture registers for each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use. • During output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Simultaneous start, stop, and clearing of desired channel counters • Synchronized operation modes (synchronized, or displaced by desired times for phase shifting) • Generation of dead time during PWM operation • Count start, count stop, counter clearing, up-counting, down-counting, or input capture by up to eight ELC events based on the ELC settings • Count start, count stop, counter clearing, up-counting, down-counting, or input capture at detection of two input signal conditions • Count start, count stop, counter clearing, up-counting, down-counting, or input capture by up to four external triggers • Function to control output negation by output disable requests from the POEG • A/D converter start trigger generation function

Item	RX62T (GPT/GPTa)	RX72T (GPTW)
Functions		• Event signals for compare match A to F and for overflow/underflow can be output to the ELC. • Ability to select noise filter function by input capture input • Bus clock: PCLKA, GPTW count reference clock: PCLKC, frequency ratio between PCLKA and PCLKC = 1:N (N = 1/2)
	• Ability to generate three-phase PWM waveforms incorporating dead time using combination of three counters • Ability to start, clear, and stop counters in response to external or internal triggers • Internal trigger sources: Comparator detection, software, and compare match • Ability to use the frequency-divided system clock (ICLK) as a counter clock for measuring the timing of the edges of signals produced by frequency-dividing the IWDT-dedicated low-speed on-chip oscillator clock (to detect abnormal oscillation)	• Ability to generate three-phase PWM waveforms incorporating dead time using combination of three counters • Ability to start, clear, and stop counters in response to external or internal triggers • Internal trigger sources: Software and compare match • Ability to monitor for frequency errors clock output from the main clock oscillator, low- and high-speed on-chip oscillators, PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB (Refer to the Clock Frequency Accuracy Measurement Circuit (CAC) chapter in RX72T Group User's Manual: Hardware.)
	• Ability to control rise and fall timing of two PWM output pins with an accuracy of up to 1/32 times the period of the system clock (ICLK) (PWM delay generation function) (RX62G Group only)	• Ability to adjust rise/fall timing of PWM waveforms with resolution of PCLKC cycle × 1/32 for complementary PWM output pins on up to four channels (Refer to the High Resolution PWM Waveform Generation Circuit (HRPWM) chapter in RX72T Group User's Manual: Hardware.)

Table 2.33 Comparison of General PWM Timer Registers

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTSTR	CST0 (RX62T) CSTRT0 (RX72T)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX62T) CSTRT1 (RX72T)	GPT1.GTCNT count start bit	Channel 1 count start bit
	CST2 (RX62T) CSTRT2 (RX72T)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX62T) CSTRT3 (RX72T)	GPT3.GTCNT count start bit	Channel 3 count start bit
	CSTRT4 to CSTRT9	—	Channel 4 to channel 9 count start bits
GTHSCR	—	General PWM timer hardware source start control register	—
GTHCCR	—	General PWM timer hardware source clear control register	—
GTHSSR	—	General PWM timer hardware start source select register	—
GTHPSR	—	General PWM timer hardware stop/clear source select register	—
GTWP	WP0 to WP3 (RX62T) WP (RX72T)	GPT0 to GPT3 register write enable bits	Register write disabled bits
	STRWP	—	GTSTR.CSTRT bit write disabled bit
	STPWP	—	GTSTP.CSTOP bit write disabled bit
	CLRWP	—	GTCLR.CCLR bit write disabled bit
	CMNWP	—	Common register write disabled bit
	PRKEY[7:0]	—	GTWP key code bits
GTSYNC	—	General PWM timer sync register	—
GTETINT	—	General PWM timer external trigger input interrupt register	—
GTBDR	—	General PWM timer buffer operation disable register	—
GTSWP	—	General PWM timer start write-protection register	—
LCCR	—	LOCO count control register	—
LCST	—	LOCO count status register	—
LCNT	—	LOCO count value register	—
LCNTA	—	LOCO count result average register	—
LCNTn	—	LOCO count result register n (n = 0 to 15)	—
LCNTDU, LCNTDL	—	LOCO count upper/lower permissible deviation register	—

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTIOR	GTIOA[5:0] (RX62T) GTIOA[4:0] (RX72T)	GTIOCnA pin function select bits (b5 to b0) Refer to Table 2.34 for details.	GTIOCnA pin function select bits (b4 to b0) Refer to Table 2.34 for details.
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX62T) GTIOB[4:0] (RX72T)	GTIOCnB pin function select bits (b13 to b8) Refer to Table 2.34 for details.	GTIOCnB pin function select bits (b20 to b16) Refer to Table 2.34 for details.
	OBDFLT	Output value at GTIOCnB pin count stop bit (b14)	Output value at GTIOCnB pin count stop bit (b22)
	OBHLD	Output retain at GTIOCnB pin count start/stop bit (b15)	Output retain at GTIOCnB pin count start/stop bit (b23)
	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value setting bits
	NFBEN	—	GTIOCnB pin input noise filter enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	EINT	Dead time error interrupt enable bit	—
	ADTRAUEN	GTADTRA compare match (up-counting) A/D converter start request enable bit (b12)	GTADTRA register compare match (up-counting) A/D converter start request enable bit (b16)
	ADTRADEN	GTADTRA compare match (down-counting) A/D converter start request enable bit (b13)	GTADTRA register compare match (down-counting) A/D converter start request enable bit (b17)
	ADTRBUEN	GTADTRB compare match (up-counting) A/D converter start request enable bit (b14)	GTADTRB register compare match (up-counting) A/D converter start request enable bit (b18)
	ADTRBDEN	GTADTRB compare match (down-counting) A/D converter start request enable bit (b15)	GTADTRB register compare match (down-counting) A/D converter start request enable bit (b19)
	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit
	GRPABL	—	Simultaneous low output stop detection enable bit

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTCR	CST	—	Count start bit
	ICDS	—	Input capture operation select at count stop bit
	MD[2:0]	Mode select bits (b2 to b0)	Mode select bits (b18 to b16)
	TPCS[1:0] (RX62T) TPCS[3:0] (RX72T)	Timer prescaler select bits (b9 and b8) b9 b8 0 0: ICLK (system clock) 0 1: ICLK/2 (system clock/2) 1 0: ICLK/4 (system clock/4) 1 1: ICLK/8 (system clock/8)	Timer prescaler select bits (b26 to b23) b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: Setting prohibited. 1 0 0 0: PCLKC/256 1 0 0 1: Setting prohibited. 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited. 1 1 0 0: GTETRGA (via the POEG) 1 1 0 1: GTETRGB (via the POEG) 1 1 1 0: GTETRGC (via the POEG) 1 1 1 1: GTETRGD (via the POEG)
	CCLR[1:0]	Counter clear source select bits	—
GTBER	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR register buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB registers buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD registers buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	CCRA[1:0]	GTCCRA buffer operation bits (b1 and b0)	GTCCRA register buffer operation bits (b17 and 16)
	CCRB[1:0]	GTCCRB buffer operation bits (b3 and b2)	GTCCRB register buffer operation bits (b19 and 18)
	PR[1:0]	GTPR buffer operation bits (b5 and b4)	GTPR register buffer operation bits (b21 and b20)
	CCRSWT	GTCCRA and GTCCRB forcible buffer operation bit (b6)	GTCCRA/GTCCRB registers forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA buffer transfer timing select bits (b9 and b8)	GTADTRA register buffer transfer timing select bits (b25 and b24)

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTBER	ADTDA	GTADTRA double buffer operation bit (b10)	GTADTRA register double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB buffer transfer timing select bits (b13 and b12)	GTADTRB register buffer transfer timing select bits (b29 and b28)
	ADTDB	GTADTRB double buffer operation bit (b14)	GTADTRB register double buffer operation bit (b30)
GTUDC	—	General PWM timer count direction register	—
GTITC	IVTC[1:0]	GTCIV interrupt skipping function select bits	GTCIV/GTCIU interrupt skipping function select bits
	IVTT[2:0]	GTCIV interrupt skipping count select bits	GTCIV/GTCIU interrupt skipping count select bits
GTST	TCFA	Compare match/input capture flag A	—
	TCFB	Compare match/input capture flag B	—
	TCFC to TCFF	Compare match flag C to F	—
	TCFPO	Overflow flag	—
	TCFPU	Underflow flag	—
	ITCNT[2:0]	GTCIV interrupt skipping count counter bits	GTCIV/GTCIU interrupt skipping count counter bits
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D converter start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D converter start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D converter start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D converter start request flag
	ODF	—	Output stop request flag
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
GTCNT	—	General PWM timer counter The GTCNT counter is a 16-bit readable/writable counter. Access in 8-bit units to the GTCNT counter is prohibited; it must be accessed in 16-bit units.	General PWM timer counter The GTCNT register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTCNT register is prohibited; it must be accessed in 32-bit units.

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTCCRm	—	General PWM timer compare capture register m (m = A to F) GTCCRm register is a 16-bit readable/writable register.	General PWM timer compare capture register m (m = A to F) GTCCRm register is a 32-bit readable/writable register. Access in 8-bit or 16-bit units to the GTCCRm register is prohibited; it must be accessed in 32-bit units.
GTPR	—	General PWM timer period setting register GTPR register is a 16-bit readable/writable register.	General PWM timer period setting register GTPR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPR register is prohibited; it must be accessed in 32-bit units.
GTPBR	—	General PWM timer period setting buffer register GTPBR register is a 16-bit readable/writable register.	General PWM timer period setting buffer register GTPBR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPBR register is prohibited; it must be accessed in 32-bit units.
GTPDBR	—	General PWM timer period setting double-buffer register GTPDBR register is a 16-bit readable/writable register.	General PWM timer period setting double-buffer register GTPDBR register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTPDBR register is prohibited; it must be accessed in 32-bit units.
GTADTRm	—	A/D converter start request timing register m (m = A or B) GTADTRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing register m (m = A or B) GTADTRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTRm register is prohibited; it must be accessed in 32-bit units.
GTADTBRm	—	A/D converter start request timing buffer register m (m = A or B) GTADTBRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTBRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing buffer register m (m = A or B) GTADTBRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTBRm register is prohibited; it must be accessed in 32-bit units.

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTADTDBRm	—	A/D converter start request timing double-buffer register m (m = A or B) GTADTDBRm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTADTDBRm register is prohibited; it must be accessed in 16-bit units.	A/D converter start request timing double-buffer register m (m = A or B) GTADTDBRm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTADTDBRm register is prohibited; it must be accessed in 32-bit units.
GTONCR	—	General PWM timer output negate control register	—
GTDVm	—	General PWM timer dead time value register m (m = U or D) GTDVm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTDVm register is prohibited; it must be accessed in 16-bit units.	General PWM timer dead time value register m (m = U or D) GTDVm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTDVm register is prohibited; it must be accessed in 32-bit units.
GTDBm	—	General PWM timer dead time value buffer register m (m = U or D) GTDBm register is a 16-bit readable/writable register. Access in 8-bit unit to the GTDBm register is prohibited; it must be accessed in 16-bit units.	General PWM timer dead time value buffer register m (m = U or D) GTDBm register is a 32-bit readable/writable counter. Access in 8-bit or 16-bit units to the GTDBm register is prohibited; it must be accessed in 32-bit units.
GTDLYCR	—	PWM output delay control register	—
GTDLYRA	—	GTIOCA rising output delay register	—
GTDLYFA	—	GTIOCA falling output delay register	—
GTDLYRB	—	GTIOCB rising output delay register	—
GTDLYFB	—	GTIOCB falling output delay register	—
GTSTP	—	—	General PWM timer software stop register
GTCLR	—	—	General PWM timer software clear register
GTSSR	—	—	General PWM timer start source select register
GTPSR	—	—	General PWM timer stop source select register
GTCSR	—	—	General PWM timer clear source select register
GTUPSR	—	—	General PWM timer count-up source select register

Register	Bit	RX62T (GPT/GPTa)	RX72T (GPTW)
GTDNSR	—	—	General PWM timer count-down source select register
GTICASR	—	—	General PWM timer input capture source select register A
GTICBSR	—	—	General PWM timer input capture source select register B
GTUDDTYC	—	—	General PWM timer count direction and duty setting register
GTADSMR	—	—	General PWM timer A/D converter start request signal monitoring register
GTEITC	—	—	General PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General PWM timer extended interrupt skipping setting register 1
GTEITLI2	—		General PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General PWM timer extended buffer transfer skipping setting register
GTSECSR	—	—	General PWM timer operation enable bit simultaneous control channel select register
GTSECR	—	—	General PWM timer operation enable bit simultaneous control register

Table 2.34 Comparative Listing of GTIOA and GTIOB Bit Settings

Bit	RX62T (GPT/GPTa) GTIOA/GTIOB[5:0] Bits	RX72T (GPTW) GTIOA/GTIOB[4:0] Bits
b5	0: Compare match 1: Input capture	—
b4	• When b5 = 0 0: Initial output is low-level 1: Initial output is high-level • When b5 = 1 x: Don't care	0: Initial output is low-level 1: Initial output is high-level
b3, b2	• When b5 = 0 0 0: Output retained at cycle end 0 1: Low-level output at cycle end 1 0: High-level output at cycle end 1 1: Toggle output at cycle end • When b5 = 1 x: Don't care	0 0: Output retained at cycle end 0 1: Low-level output at cycle end 1 0: High-level output at cycle end 1 1: Toggle output at cycle end
b1, b0	• When b5 = 0 0 0: Output retained at GPTn.GTCCRA/GPTn.GTCCRB compare match 0 1: Low-level output at GPTn.GTCCRA/GPTn.GTCCRB compare match 1 0: High-level output at GPTn.GTCCRA/GPTn.GTCCRB compare match 1 1: Toggle output at GPTn.GTCCRA/GPTn.GTCCRB compare match • When b5 = 1 0 0: Input capture at rising edge 0 1: Input capture at falling edge 1 0: Input capture at both edges 1 1: Input capture at both edges	0 0: Output retained at GTCCRA/GTCCRB register compare match 0 1: Low-level output at GTCCRA/GTCCRB register compare match 1 0: High-level output at GTCCRA/GTCCRB register compare match 1 1: Toggle output at GTCCRA/GTCCRB register compare match

2.17 Compare Match Timer

Table 2.35 is a comparative overview of compare match timer.

Table 2.35 Comparative Overview of Compare Match Timer

Item	RX62T (CMT)	RX72T (CMT)
Count clocks	Four internal clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency-divided clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output at CMT1 compare match.
Event link function (input)	—	• Ability to link to a specified module • Support for CMT1 count start, event counter, or count restart operation
Low power consumption function	Each unit can be placed in the module-stop state.	Each unit can be placed in the module-stop state.

2.18 Watchdog Timer

Table 2.36 is a comparative overview of watchdog timer, and Table 2.37 is a comparison of watchdog timer registers.

Table 2.36 Comparative Overview of Watchdog Timer

Item	RX62T (WDT)	RX72T (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Count clocks	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2,048, PCLK/8,192, PCLK/32,768, PCLK/131,072	Division by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting up using an 8-bit up-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• In watchdog timer mode, counting starts when the value of the TCSR.TMS bit is 1 (watchdog timer mode) and the value of the TCSR.TME bit is 1 (counting by TCNT starts). • In interval timer mode, counting starts when the value of the TCSR.TMS bit is 0 (interval timer mode) and the value of the TCSR.TME bit is 1 (counting by TCNT starts).	• Auto-start mode: Counting starts automatically after a reset is canceled. • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• A reset occurs. (The up-counter and registers return to their initial values.) • A overflow occurs. • When the value of the TCSR.TME bit is 0. (The TCNT counter is initializes to 00h.)	• A reset occurs. (The down-counter and registers return to their initial values.) • In a low power consumption state • A counter underflows or a refresh error occurs (register start mode only)
Window function	—	Window start and end positions can be specified (for periods when refreshed are permitted or prohibited).
Watchdog timer reset issuance source	It is possible to select whether or not the WDTOVF# signal is output externally and the microcontroller is simultaneously reset internally when the counter overflows in watchdog timer mode.	• When the down-counter underflows • When a refresh occurs outside the refresh-enabled interval (refresh error)
Non-maskable interrupt or interrupt source	In interval timer mode, an interval timer interrupt (WOVI) is generated when the TCNT counter overflows.	• When the down-counter underflows • When a refresh occurs outside the refresh-enabled interval (refresh error)

Item	RX62T (WDT)	RX72T (WDTA)
Reading the counter value	The count value of the up-counter can be read by reading the TCNT register.	The count value of the down-counter can be read by reading the WDTSR register.
Channels	8 bits × 1 channel	14 bits × 1 channel
Operating modes	Switchable between watchdog timer mode and interval timer mode	Switchable between auto-start mode and register-start mode

Table 2.37 Comparison of Watchdog Timer Registers

Register	Bit	RX62T (WDT)	RX72T (WDTA)
TCNT	—	Timer counter	—
TCSR	—	Timer control/status register	—
RSTCSR	—	Reset control/status register	—
WINA	—	Write window A register	—
WINB	—	Write window B register	—
WDTRR	—	—	WDT refresh register
WDTCR	—	—	WDT control register
WDTSR	—	—	WDT status register
WDTRCR	—	—	WDT reset control register

2.19 Independent Watchdog Timer

Table 2.38 is a comparative overview of independent watchdog timer, and Table 2.39 is a comparison of independent watchdog timer registers.

Table 2.38 Comparative Overview of Independent Watchdog Timer

Item	RX62T (IWDT)	RX72T (IWDTa)
Count source	On-chip oscillator clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	IWDTCLK, IWDTCLK/16, IWDTCLK/32, IWDTCLK/64, IWDTCLK/128, IWDTCLK/256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	Counting is started by a refresh of the down-counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset is canceled. • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• A reset occurs. (The down-counter and registers return to their initial values.) • A counter underflows error is generated.	• A reset occurs. (The down-counter and registers return to their initial values.) • In a low power consumption state (depending on register setting) • A counter underflows or a refresh error occurs (register start mode only)
Window function	—	Window start and end positions can be specified (for periods when refreshed are permitted or prohibited).
Reset output sources	Down-counter underflow	• Down-counter underflow • When a refresh occurs outside the refresh-enabled interval (refresh error)
Non-maskable interrupt/interrupt sources	—	• Down-counter underflow • When a refresh occurs outside the refresh-enabled interval (refresh error)
Reading the counter value	The down-counter value can be read from the IWDTSR register.	The down-counter value can be read from the IWDTSR register.
Output signals (internal signals)	Reset output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62T (IWDT)	RX72T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selection of clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selection of timeout period of independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selection of window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selection of window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selection of reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Register start mode (controlled by IWDT registers)	• Selection of clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selection of time-out period of independent watchdog timer (IWDTCR.TOPS[1:0] bits)	• Selection of clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selection of timeout period of independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selection of window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selection of window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selection of reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.39 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX62T (IWDT)	RX72T (IWDTa)
IWDTCR	—	IWDT control register	IWDT control register
		Initial values after a reset are different.	
	CKS[3:0]	Clock selection bits b7 b4 0 0 — : IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 ——: IWDTCLK/256	Clock frequency dividing ratio selection bits b7 b4 0 0 0 0: No frequency division 0 0 1 0: Division by 16 0 0 1 1: Division by 32 0 1 0 0: Division by 64 0 1 0 1: Division by 256 1 1 1 1: Division by 128
	RPES[1:0]	—	Window end position select bits
	RPSS[1:0]	—	Window start position select bits
IWDTSR	REFEF	—	Refresh error flag
IWDTRCR	—	—	IWDT reset control register
IWDTCSTPR	—	—	IWDT count stop control register

2.20 Serial Communications Interface

Table 2.40 is a comparative overview of serial communications interfaces, Table 2.41 is a comparative listing of serial communications interface channels, and Table 2.42 is a comparison of serial communications interface registers.

Table 2.40 Comparative Overview of Serial Communications Interface

Item		RX62T (SCIb)	RX72T (SCIj, SCIi, SCIh)
Serial communications modes		• Asynchronous operation • Clock synchronous operation • Smart card interface	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first	Selectable between LSB-first and MSB-first
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error	• Transmit end, transmit data empty, receive data full, receive error, receive data ready (SCI11), and data match (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11) • Completion of generation of a start condition, restart condition, or stop condition (simple I^2C mode)
Low power consumption function		Ability to set module-stop state for each channel	Ability to transition each channel to module stop state
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	—	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI11)
	Data match detection	—	Ability to compare receive data and comparison data, and generates an interrupt when they match (SCI1, SCI5, SCI6, SCI8, SCI9, and SCI11)
	Start-bit detection	Selectable between RXD pin low level and falling edge	Selectable between low level and falling edge
	Break detection	Ability to detect a break by reading the RXDn (n = 0 to 2) pin level directly when a framing error occurs	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or reading the SPTR.RXDMON flag.

Item		RX62T (SCIb)	RX72T (SCIj, SCIi, SCIh)
Asynchronous mode	Clock source	Selectable between internal or external clock	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	—	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	Noise filtering can be applied to the RXDn (n = 0 to 2) pin inputs.	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	—	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception (SCI11)
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	• Support for fast mode (Refer to description of bit rate register (BRR) for details on setting the transfer rate.)
	Noise cancellation	—	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Ability to place output pins in high-impedance state by applying a high-level signal to the SS# pin.
	Clock settings	—	Ability to select among four clock phase and clock polarity settings
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Item		RX62T (SCIb)	RX72T (SCIj, SCIi, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Ability to output break field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start frame reception	—	• Ability to detect break field low width/detection completion interrupt function • Control field 0 and control field 1 data comparison/match interrupt function • Ability to select between two data types for comparison (primary and secondary) in control field 1 • Ability to set priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Bit rate measurement function
	I/O control function	—	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	—	Usable as reload timer
Bit rate modulation function		—	Ability to reduce errors by correcting output from the on-chip baud rate generator

Table 2.41 Comparative Listing of Serial Communications Interface Channels

Item	RX62T (SCIb)	RX72T (SCIj, SCIi, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Smart card interface mode	SCI0, SCI1, SCI2	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple I^2C mode	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
Simple SPI mode	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11, SCI12
FIFO mode	—	SCI11
Data match detection	—	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11
Extended serial mode	—	SCI12
TMR clock input	—	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLK	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12 PCLKA: SCI11

Table 2.42 Comparison of Serial Communications Interface Registers

Register	Bit	RX62T (SCIb)	RX72T (SCIj,SCIi,SCIh)
SMR (When SCMR.SMIF = 0)	CHR	Character length bit (Valid in asynchronous mode only.) 0: Transmit/receive using 8-bit data length. 1: Transmit/receive using 7-bit data length.	Character length bit (Valid in asynchronous mode only.) Selection made in combination with SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive using 9-bit data length. 0 1: Transmit/receive using 9-bit data length. 1 0: Transmit/receive using 8-bit data length. (initial value) 1 1: Transmit/receive using 7-bit data length.
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode
SCR (When SCMR.SMIF = 0)	CKE[1:0]	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator SCKn pin can function as an I/O port. 0 1: On-chip baud rate generator Outputs a clock with the same frequency as the bit rate output from the SCKn pin. 1 0: External clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. 1 1: External clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1.	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator SCKn pin enters high-impedance state. 0 1: On-chip baud rate generator Outputs a clock with the same frequency as the bit rate output from the SCKn pin. 1 x: External clock or TMR clock When an external clock is used, a clock with a frequency 16 times the bit rate should be input on the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. When using the TMR clock, the SCKn pin enters the high-impedance state. The TMR clock is selectable for SCI5, SCI6, and SCI12.

Register	Bit	RX62T (SCIb)	RX72T (SCIj,SCIi,SCIh)
SCR (When SCMR.SMIF = 0)	CKE[1:0]	(Clock synchronous mode) b1 b0 0 0: Internal clock The SCKn pin functions as the clock output pin. 0 1: Internal clock The SCKn pin functions as the clock output pin. 1 0: External clock The SCKn pin functions as the clock input pin. 1 1: External clock The SCKn pin functions as the clock input pin.	(Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.
SCMR	SDIR	Bit order select bit This bit is usable in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode 0: LSB-first transmit/receive 1: MSB-first transmit/receive	Transmit/receive data transfer direction bit This bit is usable in the following modes: • Smart card interface mode • Asynchronous mode (multi-processor mode) • Clock synchronous mode • Simple SPI mode When operating in simple I²C mode, set this bit to 1. 0: LSB-first transmit/receive 1: MSB-first transmit/receive
	CHR1	—	Character length bit 1
SEMR	ACS0	—	Asynchronous mode clock source select bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
	NFEN	Noise cancelling function select bit (Valid only in asynchronous mode) 0: Disables noise cancellation for the RXDn pin 1: Enables noise cancellation for the RXDn pin	Digital noise filter function enable bit (Asynchronous mode) 0: Noise cancellation function for RXDn input signal disabled 1: Noise cancellation function for RXDn input signal enabled (Simple I²C mode) 0: Noise cancellation function for SSCLn and SSDAn input signals disabled 1: Noise cancellation function for SSCLn and SSDAn input signals enabled In modes other than the above, clear the NFEN bit to 0.
	BGDM	—	Baud rate generator double-speed mode select bit

Register	Bit	RX62T (SCIb)	RX72T (SCIj,SCIi,SCIh)
RDRH	—	—	Receive data register H
RDRL	—	—	Receive data register L
RDRHL	—	—	Receive data register HL
FRDR	—	—	Receive FIFO data register
TDRH	—	—	Transmit data register H
TDRL	—	—	Transmit data register L
TDRHL	—	—	Transmit data register HL
FTDR	—		Transmit FIFO data register
SSRFIFO	—	—	Serial status register
MDDR	—	—	Modulation duty register
SNFR	—	—	Noise filter setting register
SIMR1	—	—	I^2C mode register 1
SIMR2	—	—	I^2C mode register 2
SIMR3	—	—	I^2C mode register 3
SISR	—	—	I^2C status register
SPMR	—	—	SPI mode register
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Compare data register
DCCR	—	—	Data compare control register
SPTR	—	—	Serial port register
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control field 0 data register
CF0CR	—	—	Control field 0 compare enable register
CF0RR	—	—	Control field 0 receive data register
PCF1DR	—	—	Primary control field 1 data register
SCF1DR	—	—	Secondary control field 1 data register
CF1CR	—	—	Control field 1 compare enable register
CF1RR	—	—	Control field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.21 I²C Bus Interface

Table 2.43 is a comparative overview of I²C bus interface, and Table 2.44 is a comparison of I²C bus interface registers.

Table 2.43 Comparative Overview of I²C Bus Interface

Item	RX62T (RIIC)	RX72T (RIICa)
Communication format	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed
Transfer speed	Up to 400 kbps	Support for fast mode (up to 400 kbps)
SCL clock	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation
Issuing and detecting conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions
Slave address	• Ability to set up to three slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses	• Ability to set up to three different slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses
Acknowledgment	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected
Wait function	• Ability to implement a wait by holding the SCL clock signal low • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles (WAIT function)	• Ability to implement a wait by holding the SCL clock signal low • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Ability to delay output timing of transmitted data, including the acknowledge bit	Ability to delay output timing of transmitted data, including the acknowledge bit

Item	RX62T (RIIC)	RX72T (RIICa)
Arbitration	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission
Timeout detection function	Ability to detect extended stopping of the SCL clock using built-in time-out function	Ability to detect extended stopping of the SCL clock using built-in time-out function
Noise cancellation	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.
Interrupt sources	Four sources • Communication error/event occurrence (AL detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection) • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	Four modes: Master transmit mode, master receive mode, slave transmit mode, and slave receive mode

Item	RX62T (RIIC)	RX72T (RIICa)
Event link function (output)	—	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete

Table 2.44 Comparison of I²C Bus Interface Registers

Register	Bit	RX62T (RIIC)	RX72T (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.22 CAN Module

Table 2.45 is a comparative overview of CAN module, and Table 2.46 is a comparison of CAN module registers.

Table 2.45 Comparative Overview of CAN Module

Item	RX62T (CAN)	RX72T (CAN)
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) • fCAN: CAN clock source	• Programmable bit rate up to 1 Mbps (fCAN ≥ 8 MHz) • fCAN: CAN clock source
Message box	• 32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: — 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: — 24 mailboxes can be configured for either transmission or reception. — The remaining mailboxes can be configured as four FIFO transmission stages and four FIFO reception stages.	• 32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: — 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: — 24 mailboxes can be configured for either transmission or reception. — The remaining mailboxes can be configured as four FIFO transmission stages and four FIFO reception stages.
Reception	• Ability to receive data frames and remote frames • Selectable ID reception format (only standard IDs, only extended IDs, or both standard and extended IDs) • Ability to select one-shot reception function • Ability to select among overwrite mode (messages are overwritten) and overrun mode (messages are discarded) • Ability to enable or disable reception complete interrupt individually for each mailbox	• Ability to receive data frames and remote frames • Selectable ID reception format (only standard IDs, only extended IDs, or both standard and extended IDs) • Ability to select one-shot reception function • Ability to select among overwrite mode (messages are overwritten) and overrun mode (messages are discarded) • Ability to enable or disable reception complete interrupt individually for each mailbox
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • Ability to enable or disable masks individually for each mailbox	• Eight acceptance masks (one mask for every four mailboxes) • Ability to enable or disable masks individually for each mailbox

Item	RX62T (CAN)	RX72T (CAN)
Transmission	• Ability to transmit data frames and remote frames • Ability to select ID transmission format (only standard IDs, only extended IDs, or both standard and extended IDs) • Ability to select one-shot transmission function • Ability to select between ID priority mode and mailbox number priority mode • Ability to abort transmission requests (and ability to confirm abort completion with a flag) • Ability to enable or disable transmission complete interrupt individually for each mailbox	• Ability to transmit data frames and remote frames • Ability to select ID transmission format (only standard IDs, only extended IDs, or both standard and extended IDs) • Ability to select one-shot transmission function • Ability to select between ID priority mode and mailbox number priority mode • Ability to abort transmission requests (and ability to confirm abort completion with a flag) • Ability to enable or disable transmission complete interrupt individually for each mailbox
Bus-off recovery methods	• Ability to select method of recovery from the bus-off state • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by software • Transition to error-active state by software	• Ability to select method of recovery from the bus-off state • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by software • Transition to error-active state by software
Error status monitoring	• Ability to monitor CAN bus errors (stuffing error, form error, ACK error, CRC error, bit error, and ACK delimiter error) • Ability to transitions to error states (error-warning, error-passive, bus-off start, and bus-off recovery) • Ability to read error counters	• Ability to monitor CAN bus errors (stuffing error, form error, ACK error, CRC error, bit error, and ACK delimiter error) • Ability to transitions to error states (error-warning, error-passive, bus-off start, and bus-off recovery) • Ability to read error counters
Time stamp function	• Time stamp function using 16-bit counter • Ability to select reference clock among 1-, 2-, 4- and 8-bit time durations	• Time stamp function using 16-bit counter • Ability to select reference clock among 1-, 2-, 4- and 8-bit time durations
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts)
CAN sleep mode	Ability to reduce current consumption by stopping the CAN clock	Ability to reduce current consumption by stopping the CAN clock
Software support units	Three software support units • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support

Item	RX62T (CAN)	RX72T (CAN)
CAN clock source	Peripheral module clock (PCLK)	Peripheral module clock (PCLKB) or CANMCLK
Test modes	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Ability to specify transition to module stop state	Ability to specify transition to module stop state

Table 2.46 Comparison of CAN Module Registers

Register		Bit	RX62T (CAN)	RX72T (CAN)
BCR		CCLKS	—	CAN clock source select bit
MKIVLR		— (RX62T) MB0 to MB31 (RX72T)	Mask invalid register	Mask invalid register
MIER	Normal mailbox mode	— (RX62T) MB0 to MB31 (RX72T)	Interrupt enable bits	Interrupt enable bits
	FIFO mailbox mode	— (RX62T) MB0 to MB23 (RX72T)	Interrupt enable bits	Interrupt enable bits
		— (RX62T) MB24 (RX72T)	Transmit FIFO interrupt enable bit	Transmit FIFO interrupt enable bit
		— (RX62T) MB25 (RX72T)	Transmit FIFO interrupt generation timing control bit	Transmit FIFO interrupt generation timing control bit
		— (RX62T) MB28 (RX72T)	Receive FIFO interrupt enable bit	Receive FIFO interrupt enable bit
		— (RX62T) MB29 (RX72T)	Receive FIFO interrupt generation timing control bit	Receive FIFO interrupt generation timing control bit
STR		—	Status register	Status register
			Initial values after a reset are different.	

2.23 Serial Peripheral Interface

Table 2.47 is a comparative overview of serial peripheral interface, and Table 2.48 is a comparison of serial peripheral interface registers.

Table 2.47 Comparative Overview of Serial Peripheral Interface

Item	RX62T (RSPI)	RX72T (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Ability to perform serial communication in master or slave mode • Communication mode: Selectable between full-duplex and transmit-only • Ability to switch the polarity of the serial transfer clock • Ability to switch the phase of the serial transfer clock	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Ability to perform serial communication in master or slave mode • Communication mode: Selectable between full-duplex and transmit-only • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK
Data format	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to perform byte swapping of transmit and receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 8 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 8). — Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers

Item	RX62T (RSPI)	RX72T (RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)
SSL control function	• Four SSL signals (SSL0 to SSL3) per channel • In single-master mode, SSL0 to SSL3 signals are output. • In multi-master mode, the SSL0 signal is input, and the SSL1 to SSL3 signals are either output or in the high-impedance state. • In slave mode, the SSL0 signal is input, and SSL1 to SSL3 signals are in the high-impedance state. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) per channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode, the SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode, the SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity

Item	RX62T (RSPI)	RX72T (RSPIc)
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified.	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function
Event link function (output)	—	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmission-completed event signal
Other functions	• Function for disabling (initializing) the RSPI • Loopback mode	• Function for switching between CMOS and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify transition to module stop state	Ability to specify transition to module stop state

Table 2.48 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX62T (RSPI)	RX72T (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred. 1: A mode fault error occurred.	Mode fault error flag 0: No mode fault error or underrun error occurred. 1: A mode fault error or underrun error occurred.
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Available access sizes: • Longword (SPDCR.SPLW = 1) • Word (SPDCR.SPLW = 0)	RSPI data register Available access sizes: • Longword (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Word (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Byte (SPDCR.SPLW = 0, SPDCR.SPBYT = 1)
SPBR	SPR0 to SPR7 (RX62T) — (RX72T)	RSPI bit rate register	RSPI bit rate register
SPDCR	SLSEL[1:0]	SSL pin output selection bits	—
	SPBYT	—	RSPI byte access specification bit
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2

2.24 CRC Calculator

Table 2.49 is a comparative overview of CRC calculator, and Table 2.50 is a comparison of CRC calculator registers.

Table 2.49 Comparative Overview of CRC Calculator

Item	RX62T (CRC)	RX72T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated 8n-bit data units (where n is a whole number).	CRC codes are generated 8n-bit data units (where n is a whole number).	CRC codes are generated 32n-bit data units (where n is a whole number).
CRC processing method	8-bit parallel execution	8-bit parallel execution	32-bit parallel execution
CRC generation polynomial	Ability to select among three generation polynomials • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	Ability to select among three generation polynomials • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$	Ability to select among two generation polynomials • 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	Ability to select between CRC code generation for LSB-first or MSB-first communication	The bit order of the CRC calculation result can be switched to accommodate LSB-first or MSB-first for communication.	
Low power consumption function	Ability to specify transition to module stop state	Ability to transition to module stop state	

Table 2.50 Comparison of CRC Calculator Registers

Register	Bit	RX62T (CRC)	RX72T (CRCA)
CRCCR	GPS[1:0] (RX62T) GPS[2:0] (RX72T)	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation 1 1 1: No calculation
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Available access sizes: • Byte	CRC data input register Available access sizes: • Longword (for 32-bit CRC generation) • Byte (for 16-bit or 8-bit CRC generation)
CRCDOR	—	CRC data output register Available access sizes: • Word When generating 8-bit CRCs, the lower-order byte (bits b7 to b0) is used.	CRC data output register Available access sizes: • Longword (for 32-bit CRC generation) • Word (for 16-bit CRC generation) • Byte (for 8-bit CRC generation)

2.25 12-Bit A/D Converter

Table 2.51 is a comparative overview of 12-Bit A/D converter, Table 2.52 is a comparison of 12-Bit A/D converter registers, and Table 2.53 is a comparative listing A/D conversion start triggers.

Table 2.51 Comparative Overview of 12-Bit A/D Converter

Item	RX62T (S12ADA)	RX72T (S12ADH)
Number of units	2 units (S12AD0, S12AD1)	3 units (S12AD, S12AD1, S12AD2)
Input channels	Eight channels (four channels × two units)	S12AD: 8 channels, S12AD1: 8 channels, S12AD2: 14 channels
Extended analog function	—	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• 1.0 µs per channel (when A/D conversion clock (ADCLK) = 50 MHz and AVCC0 = 4.0 V to 5.5 V) • 2.0 µs per channel (when A/D conversion clock (ADCLK) = 25 MHz and AVCC0 = 3.0 V to 3.6 V)	• 0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
Data registers	• 10 registers • A/D conversion results are stored in 12-bit A/D data registers.	• 30 registers (S12AD: 8, S12AD1: 8, S12AD2: 14) for analog input, one for A/D-converted data duplication in double trigger mode per unit, and two for A/D-converted data duplication during extended operation in double trigger mode per unit. • One register for temperature sensor (S12AD2) • One register for internal reference voltage (S12AD2) • One register for self-diagnosis per unit • A/D conversion results are stored in 12-bit A/D data registers. • In A/D-converted value addition mode, the value obtained by adding up A/D-converted results is stored as (conversion accuracy bit count + 2 bits / 4 bits) in the A/D data registers. • Double trigger mode (selectable in single scan or group scan mode) — The first piece of A/D-converted analog input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX62T (S12ADA)	RX72T (S12ADH)
Data registers	• There are two A/D data registers for AN000 and AN100 input, and the conversion result storage destination is switched according to the trigger type.	• Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog input data on one selected channel is stored in the duplication register prepared for each trigger.
A/D conversion clock	4 clocks: PCLK, PCLK/2, PCLK/4, and PCLK/8	• The available peripheral module clock (PCLK) and A/D conversion clock (ADCLK) frequency ratio settings are as follows: PCLK:ADCLK frequency ratio = 1:1, 1:2, 2:1, or 4:1 • ADCLK is set by the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from 60 MHz (maximum) to 8 MHz (minimum).
Operating modes	• Single mode — A/D conversion is performed only once on the analog input of one channel. • Scan mode — Single-cycle scan mode: A/D conversion is performed only once on the analog inputs of up to four channels. — Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to four channels. — 2-channel scan mode: Channels in each unit are divided into two groups, and the conversion startup source can be separately selected for each group.	The operating mode can be set independently for three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2). • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of the groups to be used. (Only the combination of groups A and B can be selected when the number of the groups is two.) — Analog inputs on arbitrarily selected channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into groups A and B or into groups A, B, and C, and A/D conversion is performed only once on the inputs selected in group units.

Item	RX62T (S12ADA)	RX72T (S12ADH)
Operating modes		— The conditions for starting scanning of groups A, B, and C (synchronous trigger) can be selected independently, allowing A/D conversion of each group to be started at different times. • Group scan mode (group priority control selected): — If a higher-priority group trigger is input during scanning of a lower-priority group, scan of the lower-priority group is stopped and scan of the higher-priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of (rescan) the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion is not completed.
Conditions for A/D conversion start	• Software trigger • Triggering by multi-function timer pulse unit 3 (MTU3) or the general-purpose PWM timer (GPT) • External trigger — A/D conversion can be triggered on S12AD0 by the ADTRG0# pin, and on S12AD1 by the ADTRG1# pin.	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC). • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), or ADTRG2# (S12AD2) pin (independently for three units).
Functions	• Sample-and-hold function (three channels/unit) A dedicated sample-and-hold circuit is provided for each of channels 0 to 2 (AN000 to AN002) of S12AD0 and channels 0 to 2 (AN100 to AN102) of S12AD1, enabling simultaneous sampling on multiple channels (up to three channels) of each unit. • A/D converter self-diagnostic function	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (ability to specify constant sampling) • Variable sampling time function (ability to specify on per channel basis) • 12-bit A/D converter self-diagnostic function • Ability to select between A/D-converted value addition mode and average mode

Item	RX62T (S12ADA)	RX72T (S12ADH)
Functions		• Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data)
	• A/D data register auto-clear function	• A/D data register auto-clear function
	• Window-comparator function (three channels per unit)	• For functionality equivalent to the window comparator function of RX62T, refer to the Comparator C chapter in RX72T Group User's Manual: Hardware. • Comparison function (windows A and B) • Ability to specify order of channel conversion for each unit
	• Input signal amplification function using programmable gain amplifier (three channels per unit)	• Input signal amplification function using programmable gain amplifier (Each unit has three channels; either single-ended input or pseudo-differential input can be selected.)
Interrupt sources	• An interrupt request (S12ADI) can be generated on completion of A/D conversion in each unit.	• In modes other than double trigger mode and group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (independently for each of three units). • In double trigger mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (independently for each of three units). • In group scan mode, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, a group B scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) can be generated on completion of group B scan, and a group C scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) can be generated on completion of group C scan. • When double trigger group scan mode is selected, a scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan of group A, and a corresponding scan end interrupt request (S12GBADI/ S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of group B or group C scan.

Item	RX62T (S12ADA)	RX72T (S12ADH)
Interrupt sources	• An interrupt request (CMPI) is generated (and can be used as a POE source) in response to detection by the comparator. • The S12ADI interrupt can be used to activate the data-transfer controller (DTC).	• A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition of the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/ S12GCADI2 interrupts can trigger the DMA controller (DMAC) and data transfer controller (DTC).
Event link function	—	• An event signal is output when all scans are finished. • An event signal is output according to the comparison function window conditions in single scan mode. • Ability to start scanning by a trigger from the ELC
Low power consumption function	Each unit can be placed in the module stop state	Ability to specify transition to module stop state

Table 2.52 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX62T (S12ADA)	RX72T (S12ADH)
ADDRy	—	A/D data register y (y = 0A, 0B, 1 to 3)	A/D data register y (y = 0 to 7: S12AD, y = 0 to 7: S12AD1, y = 0 to 11, 16, 17: S12AD2)
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADTSDR	—	—	A/D temperature sensor data register
ADOCDR	—	—	A/D internal reference voltage data register
ADRD	AD11 to AD0 (RX62T) — (RX72T)	Converted value 11 to 0	12-bit A/D-converted value
	DIAGST[1:0] (RX62T) — (RX72T)	Self-diagnostic status bits	Self-diagnostic status bits
ADCSR	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	Clock select bits	—
	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	ADIE	A/D conversion end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS[1:0]	A/D conversion mode select bits (b6, b5) b6 b5 0 0: Single mode 0 1: Single-cycle scan mode 1 0: Continuous scan mode 1 1: 2-channel scan mode	Scan mode select bits (b14, b13) b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.
	ADST	A/D start bit (b7)	A/D conversion start bit (b15)
ADANS	—	A/D channel select register	
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 13)
ADADS0	—	—	A/D-converted value addition/average function channel select register 0
ADADS1	—	—	A/D-converted value addition/average function channel select register 1
ADADC	—	—	A/D-converted value addition/average count select register

Register	Bit	RX62T (S12ADA)	RX72T (S12ADH)
ADCER	SHBYP	Dedicated sample-and-hold circuit select bit	—
	ADPRC[1:0]	A/D data register bit precision set bits	—
	ADIE2	2-Channel scan interrupt select bit	—
	ADIEW	Double trigger interrupt select bit	—
ADSTRGR	ADSTRS0[4:0] (RX62T) TRSA[5:0] (RX72T)	A/D start trigger group 0 select bits (b4 to b0) Refer to Table 2.53 for details.	A/D conversion start trigger select bits (b13 to b8) Refer to Table 2.53 for details.
	ADSTRS1[4:0] (RX62T) TRSB[5:0] (RX72T)	A/D start trigger group 1 select bits (b12 to b8) Refer to Table 2.53 for details.	A/D conversion start trigger select for group B bits (b5 to b0) Refer to Table 2.53 for details.
ADPG	—	A/D programmable gain amplifier register	—
ADCMPMD0	—	Comparator operating-mode selection register 0	—
ADCMPMD1	—	Comparator operating-mode selection register 1	—
ADCMPNR0	—	Comparator filter-mode register 0	—
ADCMPNR1	—	Comparator filter-mode register 1	—
ADCMPFR	—	Comparator detection flag register	—
ADCMPSEL	—	Comparator interrupt selection register	—
ADSSTRn	—	A/D sampling state register	A/D sampling state register n (n = 0 to 11, L, T, or O)
		Initial values after a reset are different.	
ADEXICR	—	—	A/D conversion extended input control register
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSHCR	—	—	A/D sample-and-hold circuit control register
ADSHMSR	—	—	A/D sample-and-hold operating mode select register
ADDISCR	—	—	A/D disconnection detection control register
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1
ADCMPANSER	—	—	A/D comparison function window A extended input select register

Register	Bit	RX62T (S12ADA)	RX72T (S12ADH)
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A comparison condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0
ADPGADCR0	—	—	A/D programmable gain amplifier differential input control register
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register

Table 2.53 Comparative Listing A/D Conversion Start Triggers

Bit	RX62T (S12ADA)	RX72T (S12ADH)
ADSTRS1[4:0] (RX62T) TRSB[5:0] (RX72T)	A/D start trigger group 1 select bits b12 b8 0 0 0 0 0: ADTRGn# 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 0 1 1 1 1: TRG7AN or TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: GTADTRA0N 1 0 0 1 0: GTADTRB0N 1 0 0 1 1: GTADTRA1N 1 0 1 0 0: GTADTRB1N 1 0 1 0 1: GTADTRA2N 1 0 1 1 0: GTADTRB2N 1 0 1 1 1: GTADTRA3N 1 1 0 0 0: GTADTRB3N 1 1 0 0 1: GTADTRA0N or GTADTRB0N 1 1 0 1 0: GTADTRA1N or GTADTRB1N 1 1 0 1 1: GTADTRA2N or GTADTRB2N 1 1 1 0 0: GTADTRA3N or GTADTRB3N	Group B A/D conversion start trigger select bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Bit	RX62T (S12ADA)	RX72T (S12ADH)
ADSTRS1[4:0] (RX62T) TRSA[5:0] (RX72T)	A/D start trigger group 0 select bits b4 b0 0 0 0 0 0: ADTRGn# 0 0 0 0 1: TRGA0N 0 0 0 1 0: TRGA1N 0 0 0 1 1: TRGA2N 0 0 1 0 0: TRGA3N 0 0 1 0 1: TRGA4N 0 0 1 1 0: TRGA6N 0 0 1 1 1: TRGA7N 0 1 0 0 0: TRG0N 0 1 0 0 1: TRG4AN 0 1 0 1 0: TRG4BN 0 1 0 1 1: TRG4AN or TRG4BN 0 1 1 0 0: TRG4ABN 0 1 1 0 1: TRG7AN 0 1 1 1 0: TRG7BN 0 1 1 1 1: TRG7AN or TRG7BN 1 0 0 0 0: TRG7ABN 1 0 0 0 1: GTADTRA0N 1 0 0 1 0: GTADTRB0N 1 0 0 1 1: GTADTRA1N 1 0 1 0 0: GTADTRB1N 1 0 1 0 1: GTADTRA2N 1 0 1 1 0: GTADTRB2N 1 0 1 1 1: GTADTRA3N 1 1 0 0 0: GTADTRB3N 1 1 0 0 1: GTADTRA0N or GTADTRB0N 1 1 0 1 0: GTADTRA1N or GTADTRB1N 1 1 0 1 1: GTADTRA2N or GTADTRB2N 1 1 1 0 0: GTADTRA3N or GTADTRB3N	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRGn# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: ELCTRG00N*1/ELCTRG10N*2/ ELCTRG20N*3 1 1 0 0 1 1: ELCTRG01N*1/ELCTRG11N*2/ ELCTRG21N*3 1 1 1 0 1 0: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.26 RAM

Table 2.54 is a comparative overview of RAM, and Table 2.55 is a comparison of RAM registers.

Table 2.54 Comparative Overview of RAM

Item	RX62T (RAM)	RX72T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Capacity	16 KB or 8 KB	128 KB	16 KB
Address	• 0000 0000h to 0000 3FFFh (16 KB) • 0000 0000h to 0000 1FFFh (8 KB)	0000 0000h to 0001 FFFFh	00FF C000h to 00FF FFFFh
Memory bus	Memory bus 1	Memory bus 1	Memory bus 3
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• The ECC function can be enabled or disabled. [When MEMWAIT = 0] • The ECC function is disabled: Access takes two cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Access takes two cycles for reading or writing. • The ECC function is enabled (when an error has occurred): Access takes three cycles for reading or writing. [When MEMWAIT = 1] • The ECC function is disabled: Access takes three cycles for reading or writing. • The ECC function is enabled (when no error has occurred): Reading takes three cycles and writing takes four cycles. • The ECC function is enabled (when an error has occurred): Access takes five cycles for reading or writing.
Data retention function	Not available in deep software standby mode	Not available in deep software standby mode	

Item	RX62T (RAM)	RX72T	
		Without ECC Error Correction (RAM)	With ECC Error Correction (ECCRAM)
Low power consumption function	Ability to specify transition to module stop state	Transition to module stop state can be enabled separately for RAM and ECCRAM.	
Error checking	—	• Detection of 1-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.	• ECC error correction: Correction of 1-bit errors and detection of 2-bit errors • A non-maskable interrupt or interrupt is generated in response to an error.

Table 2.55 Comparison of RAM Registers

Register	Bit	RX62T (RAM)	RX72T (RAM, ECCRAM)
ECCRAMMODE	—	—	ECCRAM operating mode control register
ECCRAM2STS	—	—	ECCRAM 2-bit error status register
ECCRAM1STSEN	—	—	ECCRAM 1-bit error information update enable register
ECCRAM1STS	—	—	ECCRAM 1-bit error status register
ECCRAMPRCR	—	—	ECCRAM protection register
ECCRAM2ECAD	—	—	ECCRAM 2-bit error address capture register
ECCRAM1ECAD	—	—	ECCRAM 1-bit error address capture register
ECCRAMPRCR2	—	—	ECCRAM protection register 2
ECCRAMETST	—	—	ECCRAM test control register
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.27 Flash Memory

Table 2.56 is a comparative overview of flash memory, and Table 2.57 is a comparison of flash memory registers.

Table 2.56 Comparative Overview of Flash Memory

Item	RX62T		RX72T	
	Flash Memory for Code Storage	Flash Memory for Data Storage	Code Flash Memory	Data Flash Memory
Memory capacity	User area: 256 KB, 128 KB, 64 KB	Data area: 32 KB, 8 KB	• User area: 1 MB, 512 KB • User boot area: 32 KB	Data area: 32 KB
Address	[User area] • Capacity of 64 KB — FFFF 0000h to FFFF FFFFh (for reading) — 00FF 0000h to 00FF FFFFh (for writing/erasing) • Capacity of 128 KB — FFFE 0000h to FFFF FFFFh (for reading) — 00FE 0000h to 00FF FFFFh (for writing/erasing) • Capacity of 256 KB — FFFC 0000h to FFFF FFFFh (for reading) — 00FC 0000h to 00FF FFFFh (for writing/erasing)	• Capacity of 32 KB 0010 0000h to 0010 7FFFh • Capacity of 8 KB 0010 0000h to 0010 1FFFh	[User area] • Capacity of 512 KB FFF8 0000h to FFFF FFFFh • Capacity of 1 MB FFF0 0000h to FFFF FFFFh [User boot area] FF7F 8000h to FF7F FFFFh	0010 0000h to 0010 7FFFh
ROM cache	—		• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—

Item	RX62T		RX72T	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**Code Flash Memory**	**Data Flash Memory**
Read cycle	Support for fast read operation using one cycle of ICLK.	A read operation takes three cycles of PCLK for word or byte access.	• While ROM cache operation is enabled: When the cache is hit, one cycle; when the cache is missed: — One to two cycles if ICLK ≤ 120 MHz — Two to three cycles if ICLK > 120 MHz • When ROM cache operation is disabled: — One cycle if ICLK ≤ 120 MHz — Two cycles if ICLK > 120 MHz	A read operation takes eight cycles of FCLK for word or byte access.
Programming/ erasing method	• The chip incorporates a dedicated sequencer (FCU) for programming the ROM. • Programming and erasing the ROM are accomplished by issuing commands to the FCU. • Programming/ erasure through data transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/ erasure of flash memory by a user program (self-programming)	• The chip incorporates a dedicated sequencer (FCU) for programming the data flash. • Programming and erasing the data flash are accomplished by issuing commands to the FCU. • Programming/ erasure through data transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/ erasure of flash memory by a user program (self-programming)	• A dedicated sequencer (FCU) is incorporated for programming the flash memory. • Programming and erasing the code flash memory/data flash memory are handled using FACI commands specified in the FACI command issuing area (007E 0000h). • Programming/erasure through transfer by a flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)	
Value after erasure	FFh	Undefined	FFh	Undefined
Unique ID	—		A 12-byte ID code provided for each MCU	
Security function	Protects against illicit tampering or reading of data in flash memory		Protects against illicit tampering or reading of data in flash memory	

Item	RX62T		RX72T	
	Flash Memory for Code Storage	**Flash Memory for Data Storage**	**Code Flash Memory**	**Data Flash Memory**
Protection function	Protects against erroneous rewriting of the flash memory (software protection and error protection)		Protects against erroneous rewriting of the flash memory (software protection, error protection, and boot program protection)	
Trusted memory (TM) function	—		Protects against illicit reading of blocks 8 and 9 in the code flash memory	
Background operation (BGO)	• The CPU is able to execute program code from areas other than the ROM/data flash while the ROM is being programmed or erased. • Execution of program code from the ROM area is possible while the data flash memory is being programmed or erased.		• The CPU is able to execute program code from areas other than the ROM/data flash while the ROM is being programmed or erased. • The user area can be read while the data area is being programmed or erased.	
Units of programming and erasure	• Unit of programming for the user area: 256 bytes • Unit of erasure for the user area: Block	• Unit of programming for the data area: 8 bytes or 128 bytes • Unit of erasure for the data area: Block	• Unit of programming for the user area or user boot area: 256 bytes • Unit of erasure for the user area: Block	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block
Blank checking	—	• The blank checking command can be executed to check the erasure state of the data flash. • The size of the area that can be blank checked is 8 bytes or 2 KB.	—	• The blank checking command can be executed to check the erasure state of the data flash. • The size of the area to be blank-checked is 4 bytes to 32 KB (specifed in 4-byte increments).
On-board programming (serial programming/ self-programming)	• Programming in boot mode — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically.		• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased. • Programming/erasure in boot mode (USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in user boot mode — Support for original boot programs created by the user.	

Item	RX62T		RX72T	
	Flash Memory for Code Storage	Flash Memory for Data Storage	Code Flash Memory	Data Flash Memory
On-board programming (serial programming/ self-programming)	• Programming by a routine for flash memory programming within the user program — Allows ROM/data flash programming without resetting the system.		• Programming/erasure by self-programming — Allows user area/data area programming and erasure without resetting the system.	
Off-board programming (programming and erasure using parallel programmer)	A PROM programmer can be used to program the data area.	A PROM programmer cannot be used to program the data area.	Programming and erasure of the user area and user boot area by a parallel programmer is possible.	Programming or erasure of the data area by a parallel programmer is not possible.

Table 2.57 Comparison of Flash Memory Registers

Register	Bit	RX62T	RX72T
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	Data flash programming/ erasure protection violation bit	—
	DFLRPE	Data flash read protection violation bit	—
	DFLAE (RX62T) DFAE (RX72T)	Data flash access violation bit	Data flash memory access violation flag
	ROMAE (RX62T) CFAE (RX72T)	ROM access violation bit	Code flash memory access violation flag
FAEINT	DFLWPEIE	Data flash programming/ erasure protection violation interrupt enable bit	—
	DFLRPEIE	Data flash read protection violation interrupt enable bit	—
	DFLAEIE (RX62T) DFAEIE (RX72T)	Data flash access violation interrupt enable bit	Data flash memory access violation interrupt enable bit
	ROMAEIE (RX62T) CFAEIE (RX72T)	ROM access violation interrupt enable bit	Code flash memory access violation interrupt enable bit
FCURAME	—	FCU RAM enable register	—
FSTATR0 (RX62T) FSTATR (RX72T)	FLWEERR	—	Flash write/erase protect error flag
	PRGSPD	Programming suspend status bit (b0)	Programming suspend status flag (b8)
	ERSSPD	Erasure suspend status bit (b1)	Erasure suspend status flag (b9)
	DBFULL	—	Data Buffer Full Flag
	SUSRDY	Suspend ready bit (b3)	Suspend ready flag (b11)
	PRGERR	Programming error bit (b4)	Programming error flag (b12)
	ERSERR	Erasure error bit (b5)	Erasure error flag (b13)
	ILGLERR	Illegal command error bit (b6)	Illegal error command flag (b14)
	FRDY	Flash ready bit (b7)	Flash ready flag (b15)
FSTATR1	—	Flash status register 1	—

Register	Bit	RX62T	RX72T
FENTRYR	FENTRY0(RX62T) FENTRYC (RX72T)	ROM P/E mode entry bit 0	Code flash memory P/E mode entry bit
	FEKEY[7:0] (RX62T) KEY[7:0] (RX72T)	Key code bits	Key code bits
FPROTR	FPKEY[7:0] (RX62T) KEY[7:0] (RX72T)	Key code bits	Key code bits
FRESETR	—	Flash reset register	—
PCKAR (RX62T) FPCKAR (RX72T)	PCKA[7:0]	Peripheral clock notification bits These bits are used to set the peripheral clock (PCLK) at programming/erasure of the ROM or data flash.	Flash sequencer processing clock frequency notification bits These bits are used to set the frequency of the FlashIF clock (FCLK) and notify the flash sequencer of the frequency used.
	KEY[7:0]	—	Key code bits
DFLRE0	—	Data flash read enable register 0	—
DFLRE1	—	Data flash read enable register 1	—
DFLWE0	—	Data flash programming/ erasure enable register 0	—
DFLWE1	—	Data flash programming/ erasure enable register 1	—
DFLBCCNT	—	Data flash blank check control register	—
DFLBCSTAT (RX62T) FBCSTAT (RX72T)	—	Data flash blank check status register DFLBCSTAT is a 16-bit register.	Data flash blank check status register DFLBCSTAT is an 8-bit register.
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FBCCNT	—	—	Data flash blank check control register
FPSADDR	—	—	Data flash programming start address register
UIDRn	—	—	Unique ID register n (n = 0 to 2)

2.28 Packages

As indicated in Table 2.58, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.58 Packages

Package Type	Renesas Code	
	RX62T	RX72T
112-pin LQFP	○	×
100-pin LFQFP	PLQP0100KB-A	PLQP0100KB-B
80-pin LQFP	○	×
64-pin LQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by blue text. Items that exists on both groups with different specifications are indicated by red text. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 100-Pin Package (RX72T: With PGA Pseudo-Differential Input and USB Pins)

Table 3.1 is a comparative listing of the pin functions of 100-pin package products (RX72T: with PGA Pseudo-Differential Input and USB Pins).

Table 3.1 Comparative Listing of 100-Pin Package Pin Functions (RX72T: With PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and USB Pin)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	UPSEL/PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/USB0_OVRCURB/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and USB Pin)
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/ GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/ CTS1#/RTS1#/SS1#/CTS11#/RTS11#/ SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/ TMRI0/TMRI6/RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11/IRQ6
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/ IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA/USB0_VBUS
24	TRDATA3/PD1/GTIOC3A/MISO-C	USB0_DM
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	USB0_DP
26	TRDATA1/PB7/SCK2-A	VCC_USB
27	TRDATA0/PB6/RXD2-A/CRX-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/USB0_OVRCURA/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/ SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0/USB0_VBUSEN
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/ USB0_OVRCURB/IRQ3_DS
31	PLLVSS	VSS/VSS_USB
32	PB3/MTIOC0A-A/SCK0	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and USB Pin)
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/USB0_ID/USB0_OVRCURA/ IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0/ USB0_EXICEN/USB0_VBUSEN
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE4#/CTS8#/ RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and USB Pin)
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/RSPCK-A	P27/CS3#/MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/POE9#/IRQ15
65	P23/CTX-B/LTX/MOSI-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/CRX-B/LRX/MISO-A/ADTRG#	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN5	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN4	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P47/AN103
83	P50/AN6	P46/AN102/CMPC50/CMPC51
84	P47/AN103/CVREFH	P45/AN101/CMPC40/CMPC41
85	P46/AN102	P44/AN100/CMPC30/CMPC31
86	P45/AN101	PH4/AN107/PGAVSS1
87	P44/AN100	P43/AN003
88	P43/AN003/CVREFL	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000	PH0/AN007/PGAVSS0
92	AVCC0	AVCC1
93	VREFH0	AVCC0
94	VREFL0	AVSS0

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and USB Pin)
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.2 100-Pin Package (RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

Table 3.2 is a comparative listing of the pin functions of 100-pin package products (RX72T: with PGA pseudo-differential input and without USB pins).

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions (RX72T: With PGA Pseudo-Differential Input and Without USB Pins)

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and Without USB Pin)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and Without USB Pin)
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/ IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	TRDATA3/PD1/GTIOC3A/MISO-C	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/SCK2-A	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	TRDATA0/PB6/RXD2-A/CRX-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/ SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	PLLVSS	VSS
32	PB3/MTIOC0A-A/SCK0	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and Without USB Pin)
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE0#/CTS9#/RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/MTIOC3A#/MTCLKA#/GTIOC3B/GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/MTIOC3C#/MTCLKB#/GTIOC3A/GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/MTIOC0B#/MTCLKD#/TMCI6/SCK8/CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3
64	P24/RSPCK-A	P27/CS3#/MTIOC1A/MTIOC0C/MTIOC1A#/MTIOC0C#/POE9#/IRQ15

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and Without USB Pin)
65	P23/CTX-B/LTX/MOSI-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
66	P22/CRX-B/LRX/MISO-A/ADTRG#	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
69	P65/AN5	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
70	P64/AN4	P65/A12/IRQ9/AN211/CMPC53/DA1
71	AVCC	P64/A13/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P47/AN103
83	P50/AN6	P46/AN102/CMPC50/CMPC51
84	P47/AN103/CVREFH	P45/AN101/CMPC40/CMPC41
85	P46/AN102	P44/AN100/CMPC30/CMPC31
86	P45/AN101	PH4/AN107/PGAVSS1
87	P44/AN100	P43/AN003
88	P43/AN003/CVREFL	P42/AN002/CMPC20/CMPC21
89	P42/AN002	P41/AN001/CMPC10/CMPC11
90	P41/AN001	P40/AN000/CMPC00/CMPC01
91	P40/AN000	PH0/AN007/PGAVSS0
92	AVCC0	AVCC1
93	VREFH0	AVCC0
94	VREFL0	AVSS0
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100 Pins	RX62T	RX72T (With PGA Pseudo-Differential Input and Without USB Pin)
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

3.3 100-Pin Package (RX72T: Without PGA Pseudo-Differential Input and USB Pins)

Table 3.3 is a comparative listing of the pin functions of 100-pin package products (RX72T: without PGA pseudo-differential input and USB pins).

Table 3.3 Comparative Listing of 100-Pin Package Pin Functions (RX72T: Without PGA Pseudo-Differential Input and USB Pins)

100 Pins	RX62T	RX72T (Without PGA Pseudo-Differential Input and USB Pin)
1	PE5/IRQ0-B	PE5/BCLK/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK9/CTS9#/RTS9#/SS9#/IRQ0/ADST0
2	EMLE	EMLE
3	VSS	VSS
4	MDE	UB/P00/A11/MTIOC9A/MTIOC9A#/CACREF/RXD9/SMISO9/SSCL9/RXD12/SMISO12/SSCL12/RXDX12/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD1	MD/FINED
7	MD0	P01/A10/MTIOC9C/MTIOC9C#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE12#/TXD9/SMOSI9/SSDA9/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ4/ADST2/COMP1
8	PE4/MTCLKC-C/POE10#-B/IRQ1-B	PE4/A9/MTCLKC/MTCLKC#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE10#/SCK9/IRQ1
9	PE3/MTCLKD-C/POE11#/IRQ2-A	PE3/A8/MTCLKD/MTCLKD#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/POE11#/CTS9#/RTS9#/SS9#/IRQ2_DS
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	PE2/POE10#-A/NMI	PE2/POE10#/NMI
16	PE1/SSL3-C	PE1/WR0#/WR#/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/IRQ15
17	PE0/SSL2-C/CRX-C	PE0/WR1#/BC1#/WAIT#/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2/CRX0/IRQ7
18	TRST#/PD7/GTIOC0A-B/SSL1-C/CTX-C	TRST#/PD7/MTIOC9A/MTIOC9A#/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/TMRI1/TMRI5/TXD5/SMOSI5/SSDA5/SSLA1/CTX0/IRQ8
19	TMS/PD6/GTIOC0B-B/SSL0-C	TMS/PD6/MTIOC9C/MTIOC9C#/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/TMO1/CTS1#/RTS1#/SS1#/CTS11#/RTS11#/SS11#/SSLA0/IRQ5/ADST0
20	TDI/PD5/GTIOC1A-B/RXD1	TDI/PD5/GTIOC1A/GTETRGA/GTIOC1A#/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/RXD11/SMISO11/SSCL11/IRQ6

100 Pins	RX62T	RX72T (Without PGA Pseudo-Differential Input and USB Pin)
21	TCK/PD4/GTIOC1B-B/SCK1	TCK/PD4/GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/TMCI6/SCK1/SCK11/ IRQ2
22	TDO/PD3/GTIOC2A-B/TXD1	TDO/PD3/GTIOC2A/GTETRGC/GTIOC2A#/ TMO0/TXD1/SMOSI1/SSDA1/TXD11/ SMOSI11/SSDA11
23	TRCLK/PD2/GTIOC2B-B/MOSI-C	TRCLK/PD2/A7/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/TMCI1/TMO4/ SCK5/SCK8/MOSIA
24	TRDATA3/PD1/GTIOC3A/MISO-C	TRDATA3/PD1/A6/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/TMO2/RXD8/ SMISO8/SSCL8/MISOA
25	TRDATA2/PD0/GTIOC3B/RSPCK-C	TRDATA2/PD0/A5/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/TMO6/TXD8/ SMOSI8/SSDA8/RSPCKA
26	TRDATA1/PB7/SCK2-A	TRDATA1/PB7/A4/GTIOC1B/GTIOC1B#/ SCK5/SCK11/SCK12
27	TRDATA0/PB6/CRX-A/RXD2-A	TRDATA0/PB6/A3/GTIOC2A/GTIOC2A#/ RXD5/SMISO5/SSCL5/RXD11/SMISO11/ SSCL11/RXD12/SMISO12/SSCL12/ RXDX12/CRX0/IRQ2
28	TRSYNC/PB5/TXD2-A/CTX-A	TRSYNC/PB5/A2/GTIOC2B/GTIOC2B#/ TXD5/SMOSI5/SSDA5/TXD11/SMOSI11/ SSDA11/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0
29	PLLVCC	VCC
30	PB4/GTETRG/POE8#/IRQ3	PB4/A1/GTETRGA/GTETRGB/GTETRGC/ GTETRGD/POE8#/CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/SS11#/IRQ3_DS
31	PLLVSS	VSS
32	PB3/MTIOC0A-A/SCK0	PB3/A7/MTIOC0A/MTIOC0A#/CACREF/ SCK6/ RSPCKA/IRQ9
33	PB2/MTIOC0B-A/TXD0/SDA	PB2/A6/MTIOC0B/MTIOC0B#/GTADSM0/ TMRI0/TXD6/SMOSI6/SSDA6/SDA/ADSM0
34	PB1/MTIOC0C/RXD0/SCL	PB1/A5/MTIOC0C/MTIOC0C#/GTADSM1/ TMCI0/RXD6/SMISO6/SSCL6/SCL/IRQ4/ ADSM1
35	PB0/MTIOC0D/MOSI-B	PB0/A0/A4/BC0#/MTIOC0D/MTIOC0D#/ TMO0/TXD6/SMOSI6/SSDA6/CTS11#/ RTS11#/SS11#/MOSIA/IRQ8/ADTRG2#
36	PA5/MTIOC1A/MISO-B/ADTRG1#-A	PA5/A3/MTIOC1A/MTIOC1A#/TMCI3/ RXD6/SMISO6/SSCL6/RXD8/SMISO8/ SSCL8/MISOA/IRQ1/ADTRG1#
37	PA4/MTIOC1B/RSPCK-B/ADTRG0#-A	PA4/A2/MTIOC1B/MTIOC1B#/TMCI7/ SCK6/TXD8/SMOSI8/SSDA8/RSPCKA/ ADTRG0#
38	PA3/MTIOC2A/SSL0-B	PA3/A1/MTIOC2A/MTIOC2A#/GTADSM0/ TMRI7/TXD9/SMOSI9/SSDA9/SCK8/SSLA0
39	PA2/MTIOC2B/SSL1-B	PA2/A0/BC0#/MTIOC2B/MTIOC2B#/ GTADSM1/TMO7/CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/SCK11/SSLA1

100 Pins	RX62T	RX72T (Without PGA Pseudo-Differential Input and USB Pin)
40	PA1/MTIOC6A/SSL2-B	PA1/MTIOC6A/MTIOC6A#/TMO4/TXD9/ SMOSI9/SSDA9/RXD11/SMISO11/SSCL11/ SSLA2/CRX0/IRQ14_DS/ADTRG0#
41	PA0/MTIOC6C/SSL3-B	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK9/ TXD11/SMOSI11/SSDA11/SSLA3/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/CS0#/WAIT#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ POE4#/CTS8#/RTS8#/SS8#/IRQ4_DS
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC6B#/GTIOC4A/ GTIOC7A/GTIOC4A#/GTIOC7A#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC7A#/GTIOC5A/ GTIOC8A/GTIOC5A#/GTIOC8A#
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC7B#/GTIOC6A/ GTIOC9A/GTIOC6A#/GTIOC9A#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6D#/GTIOC4B/ GTIOC7B/GTIOC4B#/GTIOC7B#
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC8B/GTIOC5B#/GTIOC8B#
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC9B/GTIOC6B#/GTIOC9B#
51	P76/MTIOC4D/GTIOC2B-A	P76/D0[A0/D0]/MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/GTIOC2B#/GTIOC6B#
52	P75/MTIOC4C/GTIOC1B-A	P75/D1[A1/D1]/MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#
53	P74/MTIOC3D/GTIOC0B-A	P74/D2[A2/D2]/MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#
54	P73/MTIOC4B/GTIOC2A-A	P73/D3[A3/D3]/MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/GTIOC2A#/GTIOC6A#
55	P72/MTIOC4A/GTIOC1A-A	P72/D4[A4/D4]/MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/GTIOC1A#/GTIOC5A#
56	P71/MTIOC3B/GTIOC0A-A	P71/D5[A5/D5]/MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/GTIOC0A#/GTIOC4A#
57	P70/POE0#/IRQ5	P70/D6[A6/D6]/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/POE0#/CTS9#/ RTS9#/SS9#/IRQ5_DS
58	P33/MTIOC3A/MTCLKA-A/SSL3-A	P33/D7[A7/D7]/MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0/SSLA3/IRQ13_DS
59	P32/MTIOC3C/MTCLKB-A/SSL2-A	P32/D8[A8/D8]/MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6/SSLA2/IRQ12_DS
60	VCC	VCC
61	P31/MTIOC0A-B/MTCLKC-A/SSL1-A	P31/D9[A9/D9]/MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/TMRI6/SSLA1/IRQ6
62	VSS	VSS
63	P30/MTIOC0B-B/MTCLKD-A/SSL0-A	P30/D10[A10/D10]/MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/TMCI6/SCK8/ CTS8#/RTS8#/SS8#/SSLA0/IRQ7/COMP3

100 Pins	RX62T	RX72T (Without PGA Pseudo-Differential Input and USB Pin)
64	P24/RSPCK-A	P24/D11[A11/D11]/MTIC5U/MTIC5U#/ TMCI2/TMO6/CTS8#/RTS8#/SS8#/SCK8/ RSPCKA/IRQ4/COMP0
65	P23/LTX/MOSI-A/CTX-B	P23/D12[A12/D12]/MTIC5V/MTIC5V#/ TMO2/CACREF/TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/SSDA12/TXDX12/ SIOX12/MOSIA/CTX0/IRQ11/COMP1
66	P22/LRX/MISO-A/CRX-B/ADTRG#	P22/D13[A13/D13]/MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/MTIOC9B/TMRI2/ TMO4/RXD8/SMISO8/SSCL8/RXD12/ SMISO12/SSCL12/RXDX12/MISOA/CRX0/ IRQ10/ADTRG2#/COMP2
67	P21/MTCLKA-B/IRQ6/ADTRG1#-B	P21/D14[A14/D14]/MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/TMCI4/TXD8/ SMOSI8/SSDA8/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/MOSIA/ IRQ6_DS/AN217/ADTRG1#/COMP5
68	P20/MTCLKB-B/IRQ7/ADTRG0#-B	P20/D15[A15/D15]/MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/TMRI4/CTS8#/ RTS8#/SS8#/SCK8/RSPCKA/IRQ7_DS/ AN216/ADTRG0#/COMP4
69	P65/AN5	P65/A12/IRQ9/AN211/CMPC53/DA1
70	P64/AN4	P64/A13/IRQ8/AN210/CMPC33/DA0
71	AVCC	AVCC2
72	VREF	AVCC2
73	AVSS	AVSS2
74	P63/AN3	P63/A12/A14/IRQ7/AN209/CMPC23
75	P62/AN2	P62/A13/A15/IRQ6/AN208/CMPC43
76	P61/AN1	P61/A14/A16/IRQ5/AN207/CMPC13
77	P60/AN0	P60/A15/A17/IRQ4/AN206/CMPC03
78	P55/AN11	P55/A16/A18/IRQ3/AN203/CMPC32
79	P54/AN10	P54/A17/A19/IRQ2/AN202/CMPC22
80	P53/AN9	P53/A18/A20/IRQ1/AN201/CMPC12
81	P52/AN8	P52/IRQ0/AN200/CMPC02
82	P51/AN7	P51/AN205/CMPC52
83	P50/AN6	P50/AN204/CMPC42
84	P47/AN103/CVREFH	P47/AN103
85	P46/AN102	P46/AN102/CMPC50/CMPC51
86	P45/AN101	P45/AN101/CMPC40/CMPC41
87	P44/AN100	P44/AN100/CMPC30/CMPC31
88	P43/AN003/CVREFL	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000	P40/AN000/CMPC00/CMPC01
92	AVCC0	AVCC1
93	VREFH0	AVCC0
94	VREFL0	AVSS0
95	AVSS0	AVSS1
96	P82/MTIC5U/SCK2-B	P82/ALE/WAIT#/MTIC5U/MTIC5U#/ TMO4/SCK6/SCK12/IRQ3/COMP5

100 Pins	RX62T	RX72T (Without PGA Pseudo-Differential Input and USB Pin)
97	P81/MTIC5V/TXD2-B	P81/CS2#/MTIC5V/MTIC5V#/TMCI4/ TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/RXD2-B	P80/CS1#/MTIC5W/MTIC5W#/TMRI4/ RXD6/SMISO6/SSCL6/RXD12/SMISO12/ SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTCLKC-B/IRQ1-A	P11/RD#/MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/ GTETRGC/TMO3/POE9#/IRQ1_DS
100	P10/MTCLKD-B/IRQ0-A	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/GTETRGB/GTETRGD/TMRI3/ POE12#/CTS6#/RTS6#/SS6#/IRQ0_DS

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX72T Group and the RX62T/RX62G Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

Migration between the RX62T/RX62G Group (100 pins) and the RX72T Group (100 pins: without PGA pseudo-differential input and USB) is simple because are largely pin-to-pin compatible with only a few suggestions. Note that some pins need to be handled differently between the two groups. Refer to Table 3.3, Comparative Listing of 100-Pin Package Pin Functions (RX72T: Without PGA Pseudo-Differential Input and USB Pins), for details.

4.1.1 VCL Pin (External Capacitor)

When using a smoothing capacitor connected to the VCL pin to stabilize the internal power supply, use a 0.1 µF capacitor for the RX62T/RX62G Group and a 0.47 µF capacitor for the RX72T Group.

4.1.2 PLLVCC Pin

The RX72T Group does not have a PLLVCC pin.

4.1.3 Mode Setting Pins

On the RX62T/RX62G Group the pins for setting the mode on release from the reset state are MD0, MD1, and MDE, but on the RX72T Group they are MD and UB (multiplexed with P00).

4.1.4 Inputting an External Clock

When an external clock is input on the EXTAL pin, the counter-phase clock can be input on the XTAL pin on the RX62T/RX62G Group, but the XTAL pin must be left open on the RX72T Group.

4.1.5 PGA Pseudo-Differential Input–Related Pins (P40 to P42, P44 to P46, PH0, and PH4)

On the RX72T Group a negative voltage may be input on the PGA pseudo-differential input pins from the reset state. Therefore, regardless of whether or not the PGA is used, it is necessary to change the settings of the PGA-related registers in order to use the pin functions of P40 to P42, P44 to P46, PH0, and PH4 after cancellation of a reset.

For details, refer to the descriptions of the VOLSR.PGAVLS bit, the initial setting sequence of the A/D converter, and the PIDR register in RX72T Group User's Manual: Hardware.

Note that the above-mentioned setting changes are necessary even on products not equipped with PGA pseudo-differential inputs.

4.1.6 Inserting Decoupling Capacitors between AVCC and AVSS Pins

To prevent destruction of the RX72T Group's analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217) by abnormal voltage such as an excessive surge, insert capacitors between AVCCn and AVSSn, and connect a protective circuit to protect the analog input pins (AN000 to AN007, AN100 to AN107, AN200 to AN211, AN216, and AN217).

For details, refer to the 12-Bit A/D Converter chapter in RX72T Group User's Manual: Hardware.

4.2 Notes on Functional Design

Some software that runs on the RX62T/RX62G Group is compatible with the RX72T Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics differ between the groups.

This section presents notes on software regarding the settings of functions that differ between the RX72T Group and the RX62T/RX62G Group.

For differences in modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware listed in 5, Reference Documents.

4.2.1 Running RAM Self-Diagnostics on Save Register Banks

On the RX72T Group the save register banks are configured in the RAM. The save register banks are buffered, so writing to a bank with the SAVE instruction and then reading from the same bank with the RSTR instruction immediately afterwards may result in data being read from the buffer rather than from the RAM memory cells. When running RAM self-diagnostics on a save register bank, follow the steps below to ensure that the previously written data is read from the RAM rather than from the buffer.

(1) Use the SAVE instruction to write data to the bank on which self-diagnostics will be run.
(2) Use the SAVE instruction to write data to a bank other than that written to in step (1).
(3) Use the RSTR instruction to read data from the bank written to in step (1).

4.2.2 RIIC Operating Voltage Setting

When using the RIIC on the RX72T Group, it is necessary to specify the power supply voltage range in order to maintain the proper slope characteristics.

The initial setting is VCC = 4.5 V or greater. If a power supply voltage lower than 4.5 V will be used, change the voltage range setting before starting RIIC operation.

For details, refer to the description of the VOLSR.RICVLS bit in RX72T Group User's Manual: Hardware.

4.2.3 USB Operating Voltage Setting

When using the USB module on the RX72T Group, it is necessary to set the UBS power supply control bit to 1 before starting USB operation.

For details, refer to the description of the VOLSR.USBVON bit in RX72T Group User's Manual: Hardware.

4.2.4 Exception Vector Table

Addresses allocated in the vector table are fixed on the RX62T/RX62G Group. On the RX72T Group, the vector table addresses are relocatable using the value set in the exception table register (EXTB) as the start address.

4.2.5 Voltage Level Setting

On the RX72T Group, values for the voltage level setting register (VOLSR) for operating modes, the voltage detection level select register (LVDLVLR) of the voltage detection circuit, and option function select register 1 (OFS1) for the option-setting memory need to be changed to appropriate values depending on the operating voltage. Make sure to set these values using a program.

4.2.6 Endian Setting

On the RX62T/RX62G Group the endian setting is specified by the MDE pin, but on the RX72T Group the endian setting is specified in the MDE register in the option-setting memory.

4.2.7 Option-Setting Memory

ID codes used for ID code protection and ID code protection on connection of the on-chip debugger are located in the ROM (flash memory for code storage) on the RX62T/RX62G Group and in the option-setting memory on the RX72T Group. Note that the setting procedures differ between the two groups.

4.2.8 Clock Frequency Settings

On the RX62T/RX62G Group the clock frequency settings must be such that ICLK ≥ PCLK, but on the RX72T Group the settings must be as indicated below:

Requirements for clock frequency settings: ICLK ≥ BCLK, PCLKC ≥ PCLKA ≥ PCLKB

Requirements for clock frequency ratios: (N: integer)

ICLK:FCLK = N:1 or 1:N,

ICLK:PCLKA = N:1 or 1:N,

ICLK:PCLKB = N:1 or 1:N,

ICLK:PCLKC = N:1 or 1:N,

ICLK:PCLKD = N:1 or 1:N,

PCLKA:PCLKC = 1:1 or 1:2,

PCLKB:PCLKD = 1:1, 2:1, 4:1, or 1:2

Also, on the RX72T Group it is necessary to change the value of the MEMWAIT register when setting the frequency of ICLK to a frequency greater than 120 MHz.

4.2.9 Main Clock Oscillator

On the RX62T/RX62G Group the main clock starts oscillating after a reset is canceled, but on the RX72T Group the LOCO clock is used for operation after a reset is canceled, so it is necessary to use a program to start oscillation of the main clock.

4.2.10 PLL Circuit

On the RX62T/RX62G Group the multiplication factor setting range of the PLL circuit is 8×, but on the RX72T Group it is 10× to 30× (in 0.5× increments). Change the setting to an appropriate value when using the PLL circuit. Also, on the RX72T Group use a program to switch the PLL clock.

4.2.11 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects when the operation of the main clock oscillator stops and supplies a LOCO clock using the output of the low-speed on-chip oscillator as the clock source for the system clock, instead of the main clock or PLL clock.

Note that on the RX72T Group, when the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the system clock source, the system clock does not switch to the LOCO clock even if main clock oscillation stop is detected.

4.2.12 All-Module Clock Stop Mode

On the RX72T Group, 1 must be written to MSTPA24, MSTPA27, MSTPA29, and MSTPD0 to MSTPD7 when a transition is made to all-module clock stop mode.

4.2.13 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX72T Group, setting the DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.2.14 Register Write Protection Function

A register write protection function has been added on the RX72T Group to prevent important registers from being overwritten in case of program runaway. The initial setting is protection enabled, but the value of the protect bit needs to be changed in order to use functions that utilize the protected registers.

4.2.15 Software Configurable Interrupts

On the RX62T/RX62G Group the interrupt sources have fixed vector numbers, but on the RX72T Group the MTU and GPTW interrupt sources are classified as software configurable interrupt A and set in software configurable interrupt A source select register n (SLIARn). This allows interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.16 Initialization of Port Direction Register (PDR)

The method of initializing the PDR differs between the RX62T/RX62G Group and RX72T Group, even on products with the same pin count.

4.2.17 Note on Controlling Switching to General I/O Port Pin Operation by POE3

On the RX72T Group, when an output disable request is generated by making a setting in POE3, pins for which the setting is 1 in the corresponding PMMCRn register (n = 0 to 3) of the POE3 are switched to general I/O port pin operation. Therefore, set the bits in the corresponding POECRn register (n = 0 to 3) to 0 beforehand.

4.2.18 Bus Priority

On the RX62T/RX62G Group the bus priority is fixed at internal main bus 2 > internal main bus 1, but on the RX72T Group the bus priority can be set in the bus priority control register (BUSPRI).

4.2.19 Pin Assignments

On the RX62T/RX62G Group the port function registers listed in section 15, I/O Ports, in RX62T Group, RX62G Group User's Manual: Hardware are used to assign pins to module functions, but on the RX72T Group the pin function control registers described in the multi-function pin controller section of the documentation of the RX72T Group can be used to assign functions of multiple modules to the pins corresponding to the registers. Note that the pin function control registers are covered by the register write protection function. It is necessary to disable protection before writing to these registers.

4.2.20 Operating Frequencies of the GPTW and MTU3d

On the RX72T Group, the count clock for the GPTW and MTU3d is PCLKC, and the bus clock is PCLKA. Note that restrictions apply to the combinations of frequencies that may be used.

4.2.21 DMAC Activation by the MTU

On the RX72T Group, if the DMAC is activated by the MTU, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may lead to a wait before the DMA transfer starts, even though the activation source has been cleared.

4.2.22 MTIOC Pin Output Level when Counter Stopped

When operating with the MTIOC pin in the output state, clearing the CSTn bit to 0 causes the counter to stop. When this happens in complementary PWM mode or reset synchronous PWM mode on the RX72T Group, the initial output level set in the TOCR1A or TOCR2A register is output on the MTIOC pin.

When operating in other than complementary PWM mode or reset synchronous PWM mode, the output compare output level of the MTIOC is maintained.

When a write to the TIOR register occurs while the value of the CSTn bit is 0, the output level of the pin is updated to the initial output value setting.

4.2.23 Note on Timer Mode Register Setting for ELC Event Input

When using the MTU for ELC operation on the RX72T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.24 Port Output Enable

The port output enable registers on the RX72T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.25 Control in Response to Output Disabling Request on Port Output Enable 3

When a request to disable outputs is generated on the RX72T Group, pins for which the corresponding bits in the POECR1 to POECR3 and POECR7 registers are set to 1 enter the high-impedance state, and pins for which the corresponding bits in the PMMCR0 to PMMCR3 registers are set to 1 are switched to general I/O port pin operation.

When both bits are set to 1 for the same pin, the settings of the POECR1 to POECR3 and POECR7 registers take priority, and the pins enter the high-impedance state.

After a pin is switched to general I/O port pin operation, the settings of the corresponding bits in the PDR and PODR registers determine the state of the pin.

4.2.26 Setting the Active Level with MTU or GPTW Set to Inverted Output

On the RX72T Group the MPC.PmnPFS register can be used to specify normal output or inverted output for the MTU and GPTW.

When inverted output is selected on the MTU, the active level specified by the MTU.TOCR1j and MTU.TOCR2j registers (j = A, B) and the active level of the signals which are output to the pins is inverted. To use detection of simultaneous conduction in this case, specify in the ALR1 and ALR2 registers the active level based on the signals which are output to the pins.

When inverted output is selected on the GPTW, the active level of the signals which are output to the pins is inverted. To use detection of simultaneous conduction in this case, specify in the ALR3 to ALR5 registers the active level based on the signals which are output to the pins.

4.2.27 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX72T Group, their level cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state.

This limitation does not apply when port switching control is selected instead of high-impedance control.

4.2.28 Note on Using POE and POEG Together

When using the POE and POEG together on the RX72T Group, do not apply output disable control by both the POE and POEG to the same GPTW output pin.

4.2.29 General PWM Timer

Registers for the general PWM timer on the RX72T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.30 Watchdog Timer and Independent Watchdog Timer

On the RX72T Group it is possible to select either maskable or non-maskable as the type of the WDT underflow and refresh error interrupts and the IWDT underflow and refresh error interrupts.

4.2.31 Eliminating I^2C Bus Interface Noise

The RX62T Group has integrated analog noise filters on the SCL and SDA lines, but the RX72T Group has no integrated analog noise filters.

4.2.32 12-Bit A/D Converter

Registers for the 12-bit A/D converter on the RX72T Group are quite different from those on the RX62T/RX62G Group. Note that software compatibility is low with regard to this function.

4.2.33 A/D Conversion Start Bit

On the RX72T Group, when the single-scan continuous function is used (ADGSPCR.GBRP bit = 1) with group priority control operation mode enabled on the 12-bit A/D converter (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the value of the ADCSR.ADST bit is maintained as 1.

4.2.34 Restrictions on Comparison Function

On the RX72T Group the comparison function of the 12-bit A/D converter has the following restrictions:

1. Use of self-diagnostics and double trigger mode are prohibited. (ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB are not covered by the comparison function)
2. To use matching or unmatching output, it is necessary to select single scan mode.
3. When temperature sensor or internal reference voltage is selected for window A, operation of window B is prohibited.
4. When temperature sensor or internal reference voltage is selected for window B, operation of window A is prohibited.
5. The same channel cannot be set for both window A and window B.
6. It is necessary to make settings such that high-side reference value ≥ low-side reference value.

4.2.35 Generation of A/D Scan Conversion End Interrupt

On the RX72T Group, when scanning was started by a software trigger, an A/D scan conversion end interrupt is generated if the ADCSR.ADIE bit is set to 1 when the scan ends, even when double-trigger mode has been selected.

4.2.36 D/A Converter Settings

When making D/A converter settings on the RX72T Group, first set comparator C as the output destination using the D/A destination select register (DADSELR), then wait for the D/A converter output to stabilize before enabling comparator operation.

Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.2.37 Transferring Firmware to FCU RAM

On the RX62T/RX62G Group it is necessary to store FCU firmware in the FCU RAM in order to use FCU commands, but this processing is not needed on the RX72T Group.

4.2.38 ROM Cache

The RX72T Group has an 8 KB ROM cache, and ROM cache operation is disabled after a reset is canceled.

To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.39 Using Flash Memory Programming Commands

On the RX62T/RX62G Group, programming and erasing the flash memory are performed by issuing commands to the FCU. On the RX72T Group, programming and erasing the flash memory are performed by controlling the FCU with the FACI commands specified in the FACI command issuing area.

Table 4.1 is a comparative listing of FCU and FACI commands.

Table 4.1 Comparison of FCU and FACI Command Specifications

Item	FCU Command (RX62T)	FACI Command (RX72T)
Command issuing area	ROM programming/erasure address (00FC 0000h to 00FF FFFFh)	FACI command issuing area (007E 0000h)
Available command	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2/blank check • Lock bit programming	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Lock-bit read • Blank check • Configuration setting • Lock-bit programming

5. Reference Documents

User's Manual: Hardware

RX62T Group, RX62G Group User's Manual: Hardware, Rev. 2.00 (R01UH0034EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX72T Group User's Manual: Hardware, Rev. 1.00 (R01UH0803EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A094A/E
- TN-RX*-A095A/E
- TN-RX*-A096A/E
- TN-RX*-A098A/E
- TN-RX*-A099A/E
- TN-RX*-A119A/E
- TN-RX*-A141A/E
- TN-RX*-A152A/E
- TN-RX*-A161A/E
- TN-RX*-A185B/E
- TN-RX*-A193A/E
- TN-RX*-A0218A/E
- TN-RX*-A0219A/E
- TN-RX*-A0227A/E
- TN-RX*-A0231A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 22, 2019	—	First edition issued
1.10	Oct. 14, 2020	5	1 Table 1.1 Comparison of Built-In Functions of RX72T Group and RX62T Group revised
		9	2.2 Table 2.3 Comparative Overview of Operating Modes revised
		10 to 12	2.3 Table 2.5 to Table 2.7 deleted, Figure 2.1 to Figure 2.3 added
		22	2.6 Table 2.12 Comparison of Clock Generation Circuit Registers revised
		27	2.8 Exception Handling added
		30	2.9 Table 2.17 Comparison of Interrupt Controller Registers revised
		37	2.13 Table 2.22 and Table 2.23 revised
		38	2.13 Table 2.24 I/O Port Functions added
		39	2.13 Table 2.25 Comparison of I/O Port Registers revised
		42	2.14 Table 2.27 Comparison of Multi-Function Timer Pulse Unit 3 Registers revised
		43	2.14 Table 2.28 Comparison of TPSC Bit Settings (Other Than MTU5) added
		46	2.14 Table 2.29 Comparison of TPSC Bit Settings (MTU5) added
		50	2.15 Table 2.31 Comparison of Port Output Enable 3 Registers revised
		65	2.16 Table 2.33 Comparison of General PWM Timer Registers revised
		72	2.16 Table 2.34 Comparative Listing of GTIOA and GTIOB Bit Settings added
		74	2.18 Table 2.36 Comparative Overview of Watchdog Timers revised
		78	2.19 Table 2.39 Comparison of Independent Watchdog Timer Registers revised
		83	2.20 Table 2.42 Comparison of Serial Communications Interface Registers revised
		97	2.24 Table 2.50 Comparison of CRC Calculator Registers revised
		98	2.25 Table 2.51 Comparative Overview of 12-Bit A/D Converters revised
		103	2.25 Table 2.52 Comparison of 12-Bit A/D Converter Registers revised
		106	2.25 Table 2.53 Comparison of A/D Conversion Start Triggers added
		110	2.27 Table 2.56 Comparative Overview of Flash Memory revised
		116	3.1 Table 3.1 Comparative Listing of 100-Pin Package Pin Functions (RX72T: With PGA Pseudo-Differential Input and USB Pins) revised
		121	3.2 Table 3.2 Comparative Listing of 100-Pin Package Pin Functions (RX72T: With PGA Pseudo-Differential Input and Without USB Pins) revised

Rev.	Date	Description	
		Page	Summary
1.10	Oct. 14, 2020	126	3.3 Table 3.3 Comparative Listing of 100-Pin Package Pin Functions (RX72T: Without PGA Pseudo-Differential Input and USB Pins) revised
		131	4.1.4 General I/O Ports deleted
		132	4.2.1 added and 4.2.4 revised
		133, 134	4.2.11, 4.2.13, 4.2.16, and 4.2.17 added
		135	4.2.22, 4.2.23, and 4.2.25 added
		135, 136	4.2.26 to 4.2.28, 4.2.30, 4.2.31, and 4.2.33 added
		136	4.2.34 and 4.2.35 added
		137	4.2.39 Table 4.1 Comparison of FCU and FACI Command Specifications revised
		138	5 Reference Documents revised
		139	Related Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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