RX23W Group, RX230/RX231 Group

Differences Between the RX23W Group and the RX231 Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX23W Group and RX231 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 85-pin package version of the RX23W Group and the 100-pin package version and chip version B of the RX231 Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX23W Group and RX231 Group

Contents

1. Comparison of Built-In Functions of RX23W Group and RX231 Group

A comparison of the built-in functions of the RX23W Group and RX231 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX23W Group and RX231 Group.

Table 1.1 Comparison of Built-In Functions of RX23W Group and RX231 Group

Function	RX231	RX23W
CPU	○	
Operating modes	■	
Address space	○	
Resets	■	
Option-setting memory (OFSM)	■	
Voltage detection circuit (LVDAb)	■	
Clock generation circuit	●/■	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	▲/■	
Battery backup function	○	
Register write protection function	■	
Exception handling	○	
Interrupt controller (ICUb)	■	
Buses	■	
Memory-protection unit (MPU)	○	
DMA controller (DMACA)	○	
Data transfer controller (DTCa)	○	
Event link controller (ELC)	■	
I/O ports	●/■	
Multi-function pin controller (MPC)	▲/■	
Multi-function timer pulse unit 2 (MTU2a)	■	
Port output enable 2 (POE2a)	■	
16-bit timer pulse unit (TPUa)	■	
8-bit timer (TMR)	▲	
Compare match timer (CMT)	○	
Realtime clock (RTCe)	■	
Low-power timer (LPT)	○	
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	
USB 2.0 Host/Function module (USBd): RX231, (USBc): RX23W	■	
Serial communications interface (SCIg, SCIh)	■	
IrDA interface	○	
I^2C bus interface (RIICa)	○	
CAN module (RSCAN)	○	
Serial sound interface (SSI)	○	
Serial peripheral interface (RSPIa)	■	
CRC calculator (CRC)	○	
SD host interface (SDHIa)	○	
Bluetooth Low Energy (BLE)	×	○
Trusted Secure IP (TSIP-Lite)	○	
Capacitive touch sensing unit (CTSU)	■	
12-bit A/D converter (S12ADE)	■	

Function	RX231	RX23W
12-bit D/A converter (R12DAA)		■
Temperature sensor (TEMPSA)		○
Comparator B (CMPBa)		■
Data operation circuit (DOC)		○
RAM		■
Flash memory (FLASH)		■
Packages		●/■

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

2.1 Operating Modes

Table 2.1 is a comparative overview of operating modes, and Table 2.2 is a comparison of operating mode registers.

Table 2.1 Comparative Overview of Operating Modes

Item	RX231	RX23W
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	On-chip ROM disabled extended mode	—
	On-chip ROM enabled extended mode	—

Table 2.2 Comparison of Operating Mode Registers

Register	Bit	RX231	RX23W
SYSCR0	—	System control register 0	—

2.2 Resets

Table 2.3 is a comparative overview of resets, and Table 2.4 is a comparison of reset registers.

Table 2.3 Comparative Overview of Resets

Item	RX231	RX23W
RES# pin reset	RES# pin input voltage low	RES# pin input voltage low
Power-on reset	VCC rise (voltage monitored: VPOR)	VCC rise (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC fall (voltage monitored: Vdet0)	VCC fall (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC fall (voltage monitored: Vdet1)	VCC fall (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC fall (voltage monitored: Vdet2)	—
Independent watchdog timer reset	Independent watchdog timer underflow, or refresh error	Independent watchdog timer underflow, or refresh error
Watchdog timer reset	Watchdog timer underflow, or refresh error	Watchdog timer underflow, or refresh error
Software reset	Register setting	Register setting

Table 2.4 Comparison of Reset Registers

Register	Bit	RX231	RX23W
RSTSR0	LVD2RF	Voltage monitoring 2 reset detect flag	—

2.3 Option-Setting Memory

Table 2.5 is a comparison of option-setting memory registers.

Table 2.5 Comparison of Option-Setting Memory Registers

Register	Bit	RX231 (OFSM)	RX23W (OFSM)
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	Voltage detection 0 level select bits b1 b0 0 0: Setting prohibited. 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected

2.4 Voltage Detection Circuit

Table 2.6 is a comparative overview of the voltage detection circuits, and Table 2.7 is a comparison of voltage detection circuit registers.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX231 (LVDAb)			RX23W (LVDAb)	
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1
				Input voltages to VCC and the CMPA2 pin can be switched using the LVCMPCR.EXVCCINP2 bit		
	Detection voltage	Voltage selectable from four levels using OFS1.VDSEL [1:0] bits	Voltage selectable from 14 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits	Selectable from among three different levels by using OFS1 register	Selectable from among ten different levels by using LVDLVLR.LVD1LVL[3:0] bits
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or the CMPA2 pin CPU restart timing selectable: after specified time with VCC or the CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or the CMPA2 pin	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC

Item		RX231 (LVDAb)			RX23W (LVDAb)	
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt
			Non-maskable or maskable interrupt is selectable	Non-maskable or maskable interrupt is selectable		Non-maskable or maskable selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC or the CMPA2 pin and VCC or the CMPA2 pin > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either
Event link function		—	Available Vdet1 passage detection event output	Available Vdet2 passage detection event output	—	Available Vdet1 passage detection event output

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX231 (LVDAb)	RX23W (LVDAb)
LVD2CR1	—	Voltage monitoring 2 circuit control register 1	—
LVD2SR	—	Voltage monitoring 2 circuit status register	—
LVCMPCR	EXVCCINP2	Voltage detection 2 comparison voltage external input select bit	—
	LVD2E	Voltage detection 2 enable bit	—
LVDLVLR	LVD1LVL [3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.
	LVD2LVL [1:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage)	—

Register	Bit	RX231 (LVDAb)	RX23W (LVDAb)
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	—

2.5 Clock Generation Circuit

Table 2.8 is a comparative overview of the clock generation circuits, and Table 2.9 is a comparison of clock generation circuit registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX231	RX23W
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the MTU2, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN. • Generates the SSI clock (SSISCK) to be supplied to the SSI. • Generates the LPT clock (LPTCLK) to be supplied to the LPT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the MTU2, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN. • Generates the SSI clock (SSISCK) to be supplied to the SSI. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the Bluetooth-dedicated clock (BLECLK). • Generates the Bluetooth-dedicated low-speed clock (BLELOCO).

Item	RX231	RX23W
Operating frequency	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.) • SSISCK: 20 MHz (max.) • LPTCLK: Same frequency as that of the selected oscillator	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • UCLK: 48 MHz • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.) • SSISCK: 20 MHz (max.) • LPTCLK: Same frequency as that of the selected oscillator • BLECLK: 32 MHz • BLELOCO: 32.768 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pin: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pin: XCIN, XCOUT • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) • VCO oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) • VCO oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)

Item	RX231	RX23W
USB-dedicated PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 6 MHz, 8 MHz, and 12 MHz • Frequency multiplication ratio: Selectable from 4, 6, 8, and 12 • VCO oscillation frequency: 48 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 6 MHz, 8 MHz, and 12 MHz • Frequency multiplication ratio: Selectable from 4, 6, 8, and 12 • VCO oscillation frequency: 48 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz and 54 MHz	Oscillation frequency: 32 MHz and 54 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz
Bluetooth-dedicated clock oscillator	—	• Oscillation frequency: 32 MHz • Connectable resonator: Crystal resonator • Connection pins: XTAL1_RF and XTAL2_RF
Bluetooth-dedicated low-speed on-chip oscillator	—	Oscillation frequency: 32.768 kHz

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX231	RX23W
SCKCR	BCK[3:0] (RX231) Reserved bits (RX23W)	External bus clock (BCLK) select bits (b19 to b16)	— (b19 to b16) Set to the same value as the ICK[3:0] bits or PCKB[3:0] bits, whichever corresponds to the higher frequency.
	PSTOP1	BCLK pin output control bit	—
BCKCR	—	External bus clock control register	—

2.6 Low Power Consumption

Table 2.10 is a comparative overview of the low power consumption functions, and Table 2.11 is a comparison of low power consumption registers.

Table 2.10 Comparative Overview of Low Power Consumption Functions

Item	RX231	RX23W
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX231	RX23W
SBYCR	OPE	Output port enable bit	—
MSTPCRB	MSTPB25	Serial communication interface 6 module stop bit	Bluetooth Low Energy module stop bit
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC26	Serial communication interface 9 module stop bit	—

2.7 Register Write Protection Function

Table 2.12 is a comparative overview of the register write protection functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX231	RX23W
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, BCKCR, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR0 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to the battery backup function: VBATTCR, VBATTSR, VBTLVDICR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR • Registers related to the battery backup function: VBATTCR, VBATTSR, VBTLVDICR

2.8 Interrupt Controller

Table 2.13 is a comparative overview of the interrupt controllers, and Table 2.14 is a comparison of interrupt controller registers.

Table 2.13 Comparative Overview of Interrupt Controllers

Item		RX231 (ICUb)	RX23W (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0, IRQ1, and IRQ4 to IRQ7 • Number of sources: 6 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt generated by writing to a register. • One interrupt source
	Event link interrupt	The ELSR8I, ELSR18I or ELSR19I interrupt is generated by an ELC event	The ELSR8I, ELSR18I or ELSR19I interrupt is generated by an ELC event
	Interrupt priority level	Priority levels are specified by registers.	Priority levels are specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	The DTC and DMAC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	WDT underflow/ refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	IWDT underflow/ refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage monitoring circuit 1 (LVD1)

Item		RX231 (ICUb)	RX23W (ICUb)
Non-maskable interrupts	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	—
	VBATT voltage monitoring interrupt	Voltage monitoring interrupt of the VBATT	Voltage monitoring interrupt of the VBATT
Return from low power consumption modes	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by a non-maskable interrupt or any other interrupt source.
	Deep sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by a non-maskable interrupt or any other interrupt source.
	Software standby mode	Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm/periodic interrupt.	Return is initiated by a non-maskable interrupt, interrupt IRQ0, IRQ1, or IRQ4 to IRQ7, or an RTC alarm/periodic interrupt.

Table 2.14 Comparison of Register Interrupt Controller Registers

Register	Bit	RX231 (ICUb)	RX23W (ICUb)
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0, 1, 4 to 7)
IRQFLTE0	FLTEN2	IRQ2 digital filter enable bit	—
	FLTEN3	IRQ3 digital filter enable bit	—
IRQFLTC0	FCLKSEL2 [1:0]	IRQ2 digital filter sampling clock bits	—
	FCLKSEL3 [1:0]	IRQ3 digital filter sampling clock bits	—
NMISR	LVD2ST	Voltage monitoring 2 interrupt status flag	—
NMIER	LVD2EN	Voltage monitoring 2 interrupt enable bit	—
NMICLR	LVD2CLR	LVD2 clear bit	—

2.9 Buses

Table 2.15 is a comparative overview of the buses, and Table 2.16 is a comparison of bus registers.

Table 2.15 Comparative Overview of Buses

Item		RX231	RX23W
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USB0, CAN, and CTSU) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USB0, CAN, and CTSU) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX231	RX23W
Internal peripheral buses	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)
External bus CS area	CS area	• Connected to the external devices • Operates in synchronization with the external-bus clock (BCLK)	—

Table 2.16 Comparison of Bus Registers

Register	Bit	RX231	RX23W
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	csn recovery cycle register (n = 0 to 3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn wait control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn wait control register 2 (n = 0 to 3)	—
BUSPRI	BPEB[1:0]	External bus priority control bits	—

2.10 Event Link Controller

Table 2.17 is a comparative overview of the event link controllers, Table 2.18 lists the correspondences between event signal names set in ELSRn.ELS[7:0] bits and signal numbers, and Table 2.19 is a comparison of event link controller registers.

Table 2.17 Comparative Overview of Event Link Controllers

Item	RX231 (ELC)	RX23W (ELC)
Event link functions	• 63 types of event signals can be directly linked to modules. • Operation of timer modules when inputting an event signal can be selected. • Event linkage operation is possible for ports B and E. — Single port: Event linkage operation can be set for a single specified port. — Port group: Event linkage operation can be set by grouping multiple specified ports among a total of eight ports.	• 60 types of event signals can be directly linked to modules. • Operation of timer modules when inputting an event signal can be selected. • Event linkage operation is possible for ports B and E. — Single port: Event linkage operation can be set for a single specified port. — Port group: Event linkage operation can be set by grouping multiple specified ports among a total of eight ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.18 Correspondences between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX231 (ELC)	RX23W (ELC)
08h	Multi-function timer pulse unit 2	MTU1 compare match 1A	MTU1 compare match 1A
09h		MTU1 compare match 1B	MTU1 compare match 1B
0Ah		MTU1 overflow	MTU1 overflow
0Bh		MTU1 underflow	MTU1 underflow
0Ch		MTU2 compare match 2A	MTU2 compare match 2A
0Dh		MTU2 compare match 2B	MTU2 compare match 2B
0Eh		MTU2 overflow	MTU2 overflow
0Fh		MTU2 underflow	MTU2 underflow
10h		MTU3 compare match 3A	MTU3 compare match 3A
11h		MTU3 compare match 3B	MTU3 compare match 3B
12h		MTU3 compare match 3C	MTU3 compare match 3C
13h		MTU3 compare match 3D	MTU3 compare match 3D
14h		MTU3 overflow	MTU3 overflow
15h		MTU4 compare match 4A	MTU4 compare match 4A
16h		MTU4 compare match 4B	MTU4 compare match 4B
17h		MTU4 compare match 4C	MTU4 compare match 4C
18h		MTU4 compare match 4D	MTU4 compare match 4D
19h		MTU4 overflow	MTU4 overflow
1Ah		MTU4 underflow	MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1	CMT1 compare match 1

Value of ELS[7:0] Bits	Peripheral Module	RX231 (ELC)	RX23W (ELC)
22h	8-bit timer	TMR0 compare match A0	TMR0 compare match A0
23h		TMR0 compare match B0	TMR0 compare match B0
24h		TMR0 overflow	TMR0 overflow
28h		TMR2 compare match A2	TMR2 compare match A2
29h		TMR2 compare match B2	TMR2 compare match B2
2Ah		TMR2 overflow	TMR2 overflow
2Eh	Realtime clock	RTC periodic event (selectable among 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (selectable among 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	Independent watchdog timer	IWDT underflow or refresh error	IWDT underflow or refresh error
32h	Low-power timer	LPT compare match	LPT compare match
34h	12-bit A/D converter	S12AD comparison conditions met	S12AD comparison conditions met
35h		S12AD comparison conditions not met	S12AD comparison conditions not met
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full	SCI5 receive data full
3Ch		SCI5 transmit data empty	SCI5 transmit data empty
3Dh		SCI5 transmit end	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full	RIIC0 receive data full
50h		RIIC0 transmit data empty	RIIC0 transmit data empty
51h		RIIC0 transmit end	RIIC0 transmit end
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error)	RSPI0 error (mode fault, overrun, or parity error)
53h		RSPI0 idle	RSPI0 idle
54h		RSPI0 receive data full	RSPI0 receive data full
55h		RSPI0 transmit data empty	RSPI0 transmit data empty
56h		RSPI0 transmit end	RSPI0 transmit end
58h	12-bit A/D converter	S12AD A/D conversion end	S12AD A/D conversion end
59h	Comparator B0	Comparator B0 comparison result change	—
5Ah	Comparator B0 and B1	Comparator B0/B1 common comparison result change	—
5Bh	Voltage detection circuit	LVD1 voltage detection	LVD1 voltage detection
5Ch		LVD2 voltage detection	—
5Dh	DMA controller	DMAC0 transfer end	DMAC0 transfer end
5Eh		DMAC1 transfer end	DMAC1 transfer end
5Fh		DMAC2 transfer end	DMAC2 transfer end
60h		DMAC3 transfer end	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end	DTC transfer end
62h	Clock generation circuit	Clock generation circuit oscillation stop detection	Clock generation circuit oscillation stop detection

Value of ELS[7:0] Bits	Peripheral Module	RX231 (ELC)	RX23W (ELC)
63h	I/O ports	Input port group 1 input edge detection	Input port group 1 input edge detection
64h		Input port group 2 input edge detection	Input port group 2 input edge detection
65h		Single input port 0 input edge detection	Single input port 0 input edge detection
66h		Single input port 1 input edge detection	Single input port 1 input edge detection
67h		Single input port 2 input edge detection	Single input port 2 input edge detection
68h		Single input port 3 input edge detection	Single input port 3 input edge detection
69h	Event link controller	Software event	Software event
6Ah	Data operation circuit	DOC data operation condition met	DOC data operation condition met
Settings other than the above are prohibited.			

Table 2.19 Comparison of Event Link Controller Registers

Register	Bit	RX231 (ELC)	RX23W (ELC)
ELOPC	LPTMD[1:0]	b5 b4 0 0: Output the compare match event to the ICU as an interrupt request. 1 1: Event output is disabled. Settings other than the above are prohibited.	b5 b4 0 0: Output the LPT compare match 0 event to the ICU as an interrupt request. 1 1: Event output is disabled. Settings other than the above are prohibited.

2.11 I/O Ports

Table 2.20 is a comparative overview of the I/O ports of 100-pin (RX231) and 85- or 83-pin (RX23W) products, and Table 2.21 is a comparative overview of the I/O ports of 64-pin (RX231) and 56-pin (RX23W) products. Table 2.22 is a comparison of I/O port functions, and Table 2.23 is a comparison of I/O port registers.

Table 2.20 Comparative Overview of I/O Ports of 100-Pin (RX231) and 85- or 83-Pin (RX23W) Products

Port Symbol	RX231 (100-Pin)	RX23W (85-Pin, 83-Pin)
PORT0	P03, P05, P07	P03, P05, P07
PORT1	P12 to P17	P14 to P17
PORT2	P20 to P27	P21, P22, P25 to P27
PORT3	P30 to P37	P30, P31, P35 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	—
PORTA	PA0 to PA7	—
PORTB	PB0 to PB7	PB0, PB1, PB3, PB5, PB7
PORTC	PC0 to PC7	PC0, PC2 to PC7
PORTD	PD0 to PD7	PD3
PORTE	PE0 to PE7	PE0 to PE4
PORTH	PH0 to PE3	—
PORTJ	PJ3	PJ3

Table 2.21 Comparative Overview of I/O Ports of 64-Pin (RX231) and 56-Pin (RX23W) Products

Port Symbol	RX231 (64-Pin)	RX23W (56-Pin)
PORT0	P03, P05	P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P44, P46	P41, P45 to P47
PORT5	P54, P55	—
PORTA	PA0, PA1, PA3, PA4, PA6	—
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB7
PORTC	PC2 to PC7	PC0, PC2 to PC7
PORTD	—	PD3
PORTE	PE0 to PE5	PE2 to PE4
PORTH	PH0 to PH3	—

Table 2.22 Comparison of I/O Port Functions

Item	Port Symbol	RX231	RX23W
Input pull-up	PORT0	P03, P05, P07	P03, P05, P07
	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P21, P22, P25 to P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1, PB3, PB5, PB7
	PORTC	PC0 to PC7	PC0, PC2 to PC7
	PORTD	PD0 to PD7	PD3
	PORTE	PE0 to PE7	PE0 to PE4
	PORTH	PH0 to PH3	—
	PORTJ	PJ3	PJ3
Open-drain output	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P21, P22, P25 to P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORT5	P50 to P52, P54	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1, PB3, PB5, PB7
	PORTC	PC0 to PC7	PC0, PC2 to PC7
	PORTE	PE0 to PE7	PE0 to PE4
	PORTJ	PJ3	PJ3
Driving ability switching	PORT0	P03, P05, P07	P03, P05, P07
	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P21, P22, P25 to P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1, PB3, PB5, PB7
	PORTC	PC0 to PC7	PC0, PC2 to PC7
	PORTD	PD0 to PD7	PD3
	PORTE	PE0 to PE7	PE0 to PE4
	PORTH	PH0 to PH3	—
	PORTJ	PJ3	PJ3
5 V tolerant	PORT1	P12, P13, P16, P17	P16, P17
	PORT3	P30 to P32	P30, P31
	PORTB	PB5	PB5

Table 2.23 Comparison of I/O Port Registers

Register	Bit	RX231	RX23W
PSRA	—	Port switching register A	—
PSRB	—	Port switching register B	—

2.12 Multi-Function Pin Controller

Table 2.24 is a comparison of the assignments of multiplexed pins, and Table 2.25 to Table 2.36 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX23W Group only and **orange text** pins that exist on the RX231 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.24 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Interrupt	NMI (input)	P35	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○
		PD0	○	×	×	×
		PH1	○ *2	○ *2	×	×
	IRQ1 (input)	P31	○	○	○	○
		PD1	○	×	×	×
		PH2	○ *2	○ *2	×	×
	IRQ2 (input)	P32	○	×		
		P12	○	×		
		PD2	○	×		
	IRQ3 (input)	P33	○	×		
		P13	○	×		
		PD3	○	×		
	IRQ4 (input)	PB1	○	○	○	○
		P14	○	○	○	○
		P34	○	×	×	×
		PD4	○	×	×	×
	IRQ5 (input)	PA4	○	○	×	×
		P15	○	○	○	○
		PD5	○	×	×	×
		PE5	○	○	×	×
	IRQ6 (input)	PA3	○	○	×	×
		P16	○	○	○	○
		PD6	○	×	×	×
		PE6	○	×	×	×
	IRQ7 (input)	PE2	○	○	○	○
		P17	○	○	○	○
		PD7	○	×	×	×
		PE7	○	×	×	×
Clock generation circuit	CLKOUT (output)	PE3	○	○	○	○
		PE4	○	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×	×
		PB3	○	○	○	×
	MTIOC0B (input/output)	P13	○	×	×	×
		P15	○	○	○	○
		PA1	○	○	×	×
	MTIOC0C (input/output)	P32	○	×	×	×
		PB1	○	○	○	○
	MTIOC0D (input/output)	P33	○	×		
		PA3	○	○		

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Multi-function timer unit 2	MTIOC1A (input/output)	P20	○	×	×	×
		PE4	○	○	○	○
	MTIOC1B (input/output)	P21	○	×	○	×
		PB5	○	○	○	×
	MTIOC2A (input/output)	P26	○	○	○	○
		PB5	○	○	○	×
	MTIOC2B (input/output)	P27	○	○	○	○
		PE5	○	○	×	×
	MTIOC3A (input/output)	P14	○	○	○	○
		P17	○	○	○	○
		PC1	○	×	×	×
		PC7	○	○	○	○
	MTIOC3B (input/output)	P17	○	○	○	○
		P22	○	×	○	×
		PB7	○	○	○	○
		PC5	○	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○
		PC0	○	×	○	○
		PC6	○	○	○	○
		PJ3	○	×	○	×
	MTIOC3D (input/output)	P16	○	○	○	○
		P23	○	×	×	×
		PB6	○	○	×	×
		PC4	○	○	○	○
	MTIOC4A (input/output)	P24	○	×	×	×
		PA0	○	○	×	×
		PB3	○	○	○	×
		PE2	○	○	○	○
	MTIOC4B (input/output)	P30	○	○	○	○
		P54	○	○	×	×
		PC2	○	○	○	○
		PD1	○	×	×	×
		PE3	○	○	○	○
	MTIOC4C (input/output)	P25	○	×	○	×
		PB1	○	○	○	○
		PE1	○	○	○	×
		PE5	○	○	×	×
	MTIOC4D (input/output)	P31	○	○	○	○
		P55	○	○	×	×
		PC3	○	○	○	○
		PD2	○	×	×	×
		PE4	○	○	○	○
	MTIC5U (input)	PA4	○	○		
		PD7	○	×		
	MTIC5V (input)	PA6	○	○		
		PD6	○	×		
	MTIC5W (input)	PB0	○	○		
		PD5	○	×		

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Multi-function timer unit 2	MTCLKA (input)	P14	○	○	○	○
		P24	○	×	×	×
		PA4	○	○	×	×
		PC6	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○
		P25	○	×	○	×
		PA6	○	○	×	×
		PC7	○	○	○	○
	MTCLKC (input)	P22	○	×	○	×
		PA1	○	○	×	×
		PC4	○	○	○	○
	MTCLKD (input)	P23	○	×	×	×
		PA3	○	○	×	×
		PC5	○	○	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○	○
		PD7	○	×	×	×
	POE1# (input)	PB5	○	○	○	×
		PD6	○	×	×	×
	POE2# (input)	P34	○	×		
		PA6	○	○		
		PD5	○	×		
	POE3# (input)	P33	○	×	×	×
		PB3	○	○	○	×
		PD4	○	×	×	×
	POE8# (input)	P17	○	○	○	○
		P30	○	○	○	○
		PD3	○	×	○	○
		PE3	○	○	○	○
16-bit timer pulse unit	TIOCA0 (input/output)	PA0	○	○		
	TIOCB0 (input/output)	P17	○	○	○	○
		PA1	○	○	×	×
	TIOCC0 (input/output)	P32	○	×		
	TIOCD0 (input/output)	P33	○	×		
		PA3	○	○		
	TIOCA1 (input/output)	PA4	○	○		
	TIOCB1 (input/output)	P16	○	○	○	○
		PA5	○	×	×	×
	TIOCA2 (input/output)	PA6	○	○		
	TIOCB2 (input/output)	P15	○	○	○	○
		PA7	○	×	×	×
	TIOCA3 (input/output)	P21	○	×	○	×
		PB0	○	○	○	○
	TIOCB3 (input/output)	P20	○	×	×	×
		PB1	○	○	○	○
	TIOCC3 (input/output)	P22	○	×	○	×
		PB2	○	×	×	×
	TIOCD3 (input/output)	P23	○	×	×	×
		PB3	○	○	○	×
	TIOCA4 (input/output)	P25	○	×	○	×
		PB4	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
16-bit timer pulse unit	TIOCB4 (input/output)	P24	○	×	×	×
		PB5	○	○	○	×
	TIOCA5 (input/output)	P13	○	×		
		PB6	○	○		
	TIOCB5 (input/output)	P14	○	○	○	○
		PB7	○	○	○	○
	TCLKA (input)	P14	○	○	○	○
		PC2	○	○	○	○
	TCLKB (input)	P15	○	○	○	○
		PA3	○	○	×	×
		PC3	○	○	○	○
	TCLKC (input)	P16	○	○	○	○
		PB2	○	×	×	×
		PC0	○	×	○	○
	TCLKD (input)	P17	○	○	○	○
		PB3	○	○	○	×
		PC1	○	×	×	×
8-bit timer	TMO0 (output)	P22	○	×	○	×
		PB3	○	○	○	×
		PH1	○ *2	○ *2	×	×
	TMCI0 (input)	P21	○	×	○	×
		PB1	○	○	○	○
		PH3	○ *2	○ *2	×	×
	TMRI0 (input)	P20	○	×		
		PA4	○	○		
		PH2	○ *2	○ *2		
	TMO1 (output)	P17	○	○	○	○
		P26	○	○	○	○
	TMCI1 (input)	P12	○	×	×	×
		P54	○	○	×	×
		PC4	○	○	○	○
	TMRI1 (input)	P24	○	×	×	×
		PB5	○	○	○	×
	TMO2 (output)	P16	○	○	○	○
		PC7	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○
		P31	○	○	○	○
		PC6	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○
		PC5	○	○	○	○
	TMO3 (output)	P13	○	×		
		P32	○	×		
		P55	○	○		
	TMCI3 (input)	P27	○	○	○	○
		P34	○	×	×	×
		PA6	○	○	×	×
	TMRI3 (input)	P30	○	○	○	○
		P33	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Serial communications interface	RXD0 (input) / SMISO0 (input/output) / SSCL0 (input/output)	P21	○	×		
	TXD0 (output) / SMOSI0 (input/output) / SSDA0 (input/output)	P20	○	×		
	SCK0 (input/output)	P22	○	×		
	CTS0# (input) / RTS0# (output) / SS0# (input)	P23	○	×		
	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○
		P30	○	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○
		P26	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○
		P27	○	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○
		P31	○	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA2	○	×	×	×
		PA3	○	○	×	×
		PC2	○	○	○	○
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	×	×
		PC3	○	○	○	○
	SCK5 (input/output)	PA1	○	○	×	×
		PC1	○	×	×	×
		PC4	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	×	×
		PC0	○	×	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	P33	○	×		
		PB0	○	○		
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P32	○	×		
		PB1	○	○		
	SCK6 (input/output)	P34	○	×		
		PB3	○	○		
	CTS6# (input) / RTS6# (output) / SS6# (input)	PB2	○	×		
		PJ3	○	×		
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○	○	○	○
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Serial communications interface	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○	○	○	○
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○	○		
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○	○		
	SCK9 (input/output)	PB5	○	○		
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4	○	×		
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○	×
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○	×
	SCK12 (input/output)	PE0	○	○	○	×
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○	×
I²C bus interface	SCL (input/output)	P16	○	○	○	○
		P12	○	×	×	×
	SDA (input/output)	P17	○	○	○	○
		P13	○	×	×	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	×
		PB0	○	○	○	○
		PC5	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○
		PA6	○	○	×	×
		PC6	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○
		PA7	○	×	×	×
		PC7	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	×	×
		PC4	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	×
		PC0	○	×	○	○
	SSLA2 (output)	PA1	○	○		
		PC1	○	×		
	SSLA3 (output)	PA2	○	×	×	×
		PC2	○	○	○	○
Realtime clock	RTCOUT (output)	P16	○	○	○	○
		P32	○	×	×	×
	RTCIC0 (input)*1	P30	○	○	○	○
	RTCIC1 (input)*1	P31	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Realtime clock	RTCIC2 (input)*1	P32	○	×		
IrDA interface	IRTXD5 (output)	PA4	○	○	×	×
		PC3	○	○	○	○
	IRRXD5 (input)	PA2	○	×	×	×
		PA3	○	○	×	×
		PC2	○	○	○	○
CAN module	CRXD0 (input)	P15	○	○	○	○
		P55	○	○	×	×
	CTXD0 (output)	P14	○	○	○	○
		P54	○	○	×	×
Serial sound interface	SSISCK0 (input/output)	P23	○	×	×	×
		P31	○	○	○	○
		PA1	○	○	×	×
	SSIWS0 (input/output)	P21	○	×	○	×
		P27	○	○	○	○
		PA6	○	○	×	×
	SSITXD0 (output)	P17	○	○	○	○
		PA4	○	○	×	×
	SSIRXD0 (input)	P20	○	×	×	×
		P26	○	○	○	○
		PA3	○	○	×	×
	AUDIO_MCLK (input)	P22	○	×	○	×
		P30	○	○	○	○
		PE3	○	○	○	○
SD host interface	SDHI_CLK (output)	PB1	○	○	○	×
	SDHI_CMD (input/output)	PB0	○	○	○	×
	SDHI_D0 (input/output)	PC3	○	○	○	×
	SDHI_D1 (input/output)	PB6	○	○	×	×
		PC4	○	○	○	×
	SDHI_D2 (input/output)	PB7	○	○	○	×
	SDHI_D3 (input/output)	PC2	○	○	○	×
	SDHI_CD (input)	PB5	○	○	○	×
	SDHI_WP (input)	PB3	○	○	○	×
USB 2.0 Host/Function module	USB0_VBUS (input)	P16	○	○	○	○
		PB5	○	○	○	×
	USB0_EXICEN (output)	P21	○	×	○	×
		PC6	×	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○
		P24	○	×	×	×
		P26	×	○	○	○
		P32	○	×	×	×
	USB0_OVRCURA (input)	P14	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○
		P22	○	×	○	×
	USB0_ID (input)	P20	○	×	×	×
		PC5	×	○	○	○
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	×
	AN001 (input)*1	P41	○	○	○	○
	AN002 (input)*1	P42	○	○	○	×
	AN003 (input)*1	P43	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
12-bit A/D converter	AN004 (input)*1	P44	○	○	○	×
	AN005 (input)*1	P45	○	×	○	○
	AN006 (input)*1	P46	○	○	○	○
	AN007 (input)*1	P47	○	×	○	○
	AN016 (input)*1	PE0	○	○	○	×
	AN017 (input)*1	PE1	○	○	○	×
	AN018 (input)*1	PE2	○	○	○	○
	AN019 (input)*1	PE3	○	○	○	○
	AN020 (input)*1	PE4	○	○	○	○
	AN021 (input)*1	PE5	○	○		
	AN022 (input)*1	PE6	○	×		
	AN023 (input)*1	PE7	○	×		
	AN024 (input)	PD0	○	×		
	AN025 (input)	PD1	○	×		
	AN026 (input)	PD2	○	×		
	AN027 (input)	PD3	○	×	○	○
	AN028 (input)	PD4	○	×		
	AN029 (input)	PD5	○	×		
	AN030 (input)	PD6	○	×		
	AN031 (input)	PD7	○	×		
	ADTRG0# (input)	P07	○	×	○	×
		P16	○	○	○	○
		P25	○	×	○	×
D/A converter	DA0 (output)*1	P03	○	○	○	×
	DA1 (output)*1	P05	○	○	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	×
		PC7	○	○	○	○
		PH0	○ *2	○ *2	×	×
LVD voltage detection input	CMPA2 (input)*1	PE4	○	○		
Comparator B	CMPB0 (input)*1	PE1	○	○		
	CVREFB0 (input)*1	PE2	○	○		
	CMPB1 (input)*1	PA3	○	○		
	CVREFB1 (input)*1	PA4	○	○		
	CMPB2 (input)*1	P15	○	○	○	○
	CVREFB2 (input)*1	P14	○	○	○	○
	CMPB3 (input)*1	P26	○	○	○	○
	CVREFB3 (input)*1	P27	○	○	○	○
	CMPOB0 (output)	PE5	○	○		
	CMPOB1 (output)	PB1	○	○		
	CMPOB2 (output)	P17	○	○	○	○
	CMPOB3 (output)	P30	○	○	○	○
Capacitive touch sensing unit (CTSU)	TSCAP (output)	PC4	○	○	○	○
	TS0 (output)	P34	○	×		
	TS1 (output)	P33	○	×		
	TS2 (output)	P27	○	○	○	○
	TS3 (output)	P26	○	○	○	○
	TS4 (output)	P25	○	×	○	×
	TS5 (output)	P24	○	×		

Module/ Function	Pin Function	Port Allocation	RX231 (MPC)		RX23W (MPC)	
			100-Pin	64-Pin	85/83-Pin	56-Pin
Capacitive touch sensing unit (CTSU)	TS6 (output)	P23	○	×		
	TS7 (output)	P22	○	×	○	×
	TS8 (output)	P21	○	×	○	×
	TS9 (output)	P20	○	×		
	TS12 (output)	P15	○	○	○	○
	TS13 (output)	P14	○	○	○	○
	TS15 (output)	P55	○	○		
	TS16 (output)	P54	○	○		
	TS17 (output)	P53	○	×		
	TS18 (output)	P52	○	×		
	TS19 (output)	P51	○	×		
	TS20 (output)	P50	○	×		
	TS22 (output)	PC6	○	○	○	○
	TS23 (output)	PC5	○	○	○	○
	TS27 (output)	PC3	○	○	○	○
	TS30 (output)	PC2	○	○	○	○
	TS33 (output)	PC1	○	×		
	TS35 (output)	PC0	○	×	○	○
External bus	CS0# (output)	P24	○	×		
		PC7	○	×		
	CS1# (output)	P25	○	×		
		PC6	○	×		
	CS2# (output)	P26	○	×		
		PC5	○	×		
	CS3# (output)	P27	○	×		
		PC4	○	×		
	A0 to A7 (output)	PA0 to PA7	○	×		
	A8 to A15 (output)	PB0 to PB7	○	×		
	A16 to A23 (output)	PC0 to PC7	○	×		
	D0 to D7 (input/output)	PD0 to PD7	○	×		
	D8 to D15 (input/output)	PE0 to PE7	○	×		
	BCLK (output)	P53	○	×		
	RD# (output)	P52	○	×		
	WR# (output)	P50	○	×		
	WR0# (output)	P50	○	×		
	WR1# (output)	P51	○	×		
	BC0# (output)	PA0	○	×		
	BC1# (output)	P51	○	×		
	WAIT# (input)	P51	○	×		
		P55	○	×		
		PC5	○	×		
	ALE (output)	P54	○	×		

Notes: 1. For these pin functions, ensure that the corresponding pin is set as general input (PORTm.PDR.Bn and PORTm.PMR.Bn bits cleared to 0).
2. The relevant pin is implemented on the RX230 only.

Table 2.25 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX231 (n = 2 to 7)	RX23W (n = 4 to 7)
P12PFS	—	P12 pin function control register	—
P13PFS	—	P13 pin function control register	—
P14PFS	PSEL[4:0]	Pin function select bits	Pin function select bits
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (100-pin) P13: IRQ3 (100-pin) P14: IRQ4 (100/64/48-pin) P15: IRQ5 (100/64/48-pin) P16: IRQ6 (100/64/48-pin) P17: IRQ7 (100/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P14: IRQ4 (85/83/56-pin) P15: IRQ5 (85/83/56-pin) P16: IRQ6 (85/83/56-pin) P17: IRQ7 (85/83/56-pin)

Table 2.26 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 1, 2, 5 to 7)
P20PFS	—	P20 pin function control register	—
P21PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: TIOCA3 00101b: TMCI0 01010b: RXD0/SMISO0/SSCL0 10001b: USB0_EXICEN 10111b: SSIWS0 11001b: TS8	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: TIOCA3 00101b: TMCI0 10001b: USB0_EXICEN 10111b: SSIWS0 11001b: TS8
P22PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00011b: TIOCC3 00101b: TMO0 01010b: SCK0 10001b: USB0_OVRCURB 10111b: AUDIO_MCLK 11001b: TS7	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00011b: TIOCC3 00101b: TMO0 10001b: USB0_OVRCURB 10111b: AUDIO_MCLK 11001b: TS7
P23PFS	—	P23 pin function control register	—
P24PFS	—	P24 pin function control register	—

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 1, 2, 5 to 7)
P26PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10111b: SSIRXD0 11001b: TS3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10001b: USB0_VBUSEN 10111b: SSIRXD0 11001b: TS3

Table 2.27 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX231 (n = 0 to 4)	RX23W (n = 0, 1)
P32PFS	—	P32 pin function control register	—
P33PFS	—	P33 pin function control register	—
P34PFS	—	P34 pin function control register	—
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/64/48-pin) P31: IRQ1 (100/64/48-pin) P32: IRQ2 (100-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (85/83/56-pin) P31: IRQ1 (85/83/56-pin)

Table 2.28 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX231 (n = 0 to 5)	RX23W
P5nPFS	—	P5n pin function control register	—

Table 2.29 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W
PAnPFS	—	PAn pin function control register	—

Table 2.30 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 0, 1, 3, 5, 7)
PB0PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: TIOCA3 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11010b: SDHI_CMD	Pin function select bits b4 b0 00000b: Hi-Z 00011b: TIOCA3 01101b: RSPCKA 11010b: SDHI_CMD

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 0, 1, 3, 5, 7)
PB1PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00011b: TIOCB3 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11010b: SDHI_CLK	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00011b: TIOCB3 00101b: TMCI0 11010b: SDHI_CLK
PB2PFS	—	PB2 pin function control register	—
PB3PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00011b: TIOCD3 00100b: TCLKD 00101b: TMO0 00111b: POE3# 01011b: SCK6 11010b: SDHI_WP	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00011b: TIOCD3 00100b: TCLKD 00101b: TMO0 00111b: POE3# 11010b: SDHI_WP
PB4PFS	—	PB4 pin function control register	—
PB5PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00011b: TIOCB4 00101b: TMRI1 00111b: POE1# 01010b: SCK9 10001b: USB0_VBUS 11010b: SDHI_CD	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00011b: TIOCB4 00101b: TMRI1 00111b: POE1# 10001b: USB0_VBUS 11010b: SDHI_CD
PB6PFS	—	PB6 pin function control register	—
PB7PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: TIOCB5 01010b: TXD9/SMOSI9/SSDA9 11010b: SDHI_D2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: TIOCB5 11010b: SDHI_D2

Table 2.31 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 0, 2 to 7)
PC1PFS	—	PC1 pin function control register	—
PC5PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS23	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 10001b: USB0_ID 11001b: TS23
PC6PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS22	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 10001b: USB0_EXICEN 11001b: TS22

Table 2.32 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 3)
PD0PFS	—	PD0 pin function control register	—
PD1PFS	—	PD1 pin function control register	—
PD2PFS	—	PD2 pin function control register	—
PD4PFS	—	PD4 pin function control register	—
PD5PFS	—	PD5 pin function control register	—
PD6PFS	—	PD6 pin function control register	—
PD7PFS	—	PD7 pin function control register	—
PDnPFS	ISEL	Interrupt input function select bit	—
	ASEL	Analog function select bit	—

Table 2.33 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 0 to 4)
PE5PFS	—	PE5 pin function control register	—
PE6PFS	—	PE6 pin function control register	—
PE7PFS	—	PE7 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (100/64/48-pin) PE5: IRQ5 (100/64-pin) PE6: IRQ6 (100-pin) PE7: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (85/83/56-pin)

Register	Bit	RX231 (n = 0 to 7)	RX23W (n = 0 to 4)
PEnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (100/64-pin) PE1: AN017, CMPB0 (100/64/48-pin) PE2: AN018, CVREFB0 (100/64/48-pin) PE3: AN019 (100/64/48-pin) PE4: AN020 (100/64/48-pin) PE5: AN021 (100/64-pin) PE6: AN022 (100-pin) PE7: AN023 (100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (85/83-pin) PE1: AN017 (85/83-pin) PE2: AN018 (85/83/56-pin) PE3: AN019 (85/83/56-pin) PE4: AN020 (85/83/56-pin)

Table 2.34 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX231 (n = 0 to 3)	RX23W
PHnPFS	—	PHn pin function control register Implemented on the RX230 Group only.	—

Table 2.35 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX231 (n = 3)	RX23W (n = 3)
PJ3PFS	PSEL[4:0]	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 01011b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C

Table 2.36 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX231 (MPC)	RX23W (MPC)
PFCSE	—	CS output enable register	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—

2.13 Multi-Function Timer Pulse Unit 2

Table 2.37 is a comparative overview of multi-function timer pulse unit 2, and Table 2.38 is a comparison of multi-function timer pulse unit 2 registers.

Table 2.37 Comparative Overview of Multi-Function Timer Pulse Unit 2

Item	RX231 (MTU2a)	RX23W (MTU2a)
Pulse input/output	Max. 16 lines	Max. 15 lines
Pulse input	3 lines	—
Count clocks	Seven and eight clocks for each channel (four clocks for MTU5)	Seven and eight clocks for each channel
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 11-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation • Ability to specify AC synchronous motor (brushless DC motor) drive mode using complementary PWM output and reset-synchronized PWM output and ability to select between two types of waveform output (chopping and level)	[MTU0, MTU3, MTU4] • Ability to specify buffer operation • Ability to specify AC synchronous motor (brushless DC motor) drive mode using complementary PWM output and reset-synchronized PWM output and ability to select between two types of waveform output (chopping and level)
	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation
	[MTU3, MTU4] Ability to produce six-phase waveform output, including three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3, MTU4] Ability to produce six-phase waveform output, including three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation
	[MTU5] • Dead time compensation counter • Input capture function (noise filter setting function) • Counter clear operation	—
Complementary PWM mode	• Interrupts at counter peaks and troughs • Ability to skip A/D converter start triggers	• Interrupts at counter peaks and troughs • Ability to skip A/D converter start triggers
Interrupt sources	28 sources	25 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data

Item	RX231 (MTU2a)	RX23W (MTU2a)
Trigger generation	Ability to generate A/D converter start trigger	Ability to generate A/D converter start trigger
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.38 Comparison of Multi-Function Timer Pulse Unit 2 Registers

Register	Bit	RX231 (MTU2a)	RX23W (MTU2a)
TCNTCMPCLR	—	Timer compare match clear register	—

2.14 Port Output Enable 2

Table 2.39 is a comparative overview of the port output enable 2 modules, and Table 2.40 is a comparison of port output enable 2 registers.

Table 2.39 Comparative Overview of Port Output Enable 2 Modules

Item	RX231 (POE2a)	RX23W (POE2a)
High-impedance control by input level detection	• Ability to specify falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles for each of the POE0# to POE3# and POE8# input pins • Ability to put pins for complementary PWM output from the MTU in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins • Ability to put pins for output from MTU0 in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin.	• Ability to specify falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles for each of the POE0#, POE1#, POE3#, and POE8# input pins • Ability to put pins for complementary PWM output from the MTU in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins • Ability to put pins for output from MTU0 in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin.
High-impedance control by output level comparison	Ability to compare levels output on pins for complementary PWM output from the MTU and put them in the high-impedance state when simultaneous output of the active level continues for one or more cycles of the PCLK clock	Ability to compare levels output on pins for complementary PWM output from the MTU and put them in the high-impedance state when simultaneous output of the active level continues for one or more cycles of the PCLK clock
High-impedance control by oscillation stop detection	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state when oscillation by the clock generation circuit stops	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state when oscillation by the clock generation circuit stops
High-impedance control by software (registers)	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state by writing to the POE registers	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state by writing to the POE registers
High-impedance control by event signals	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state in response to an event signal from the event link controller (ELC)	Ability to put pins for complementary PWM output from the MTU and output pins for MTU0 in the high-impedance state in response to an event signal from the event link controller (ELC)
Interrupts	Ability to generate interrupts in response to the results of POE0# to POE3# and POE8# input-level detection or MTU complementary PWM output-level comparison	Ability to generate interrupts in response to the results of POE0#, POE1#, POE3#, and POE8# input-level detection or MTU complementary PWM output-level comparison

Table 2.40 Comparison of Port Output Enable 2 Registers

Register	Bit	RX231 (POE2a)	RX23W (POE2a)
ICSR1	POE2M[1:0]	POE2 mode select bits	—
	POE2F	POE2 flag	—
ICSR2	POE8E	POE8 high-impedance enable bit 0: Does not place the MTIOC0A, MTIOC0B, MTIOC0C, and MTIOC0D pins in the high-impedance state. 1: Places the MTIOC0A, MTIOC0B, MTIOC0C, and MTIOC0D pins in the high-impedance state.	POE8 high-impedance enable bit 0: Does not place the MTIOC0A, MTIOC0B, and MTIOC0C pins in the high-impedance state. 1: Places the MTIOC0A, MTIOC0B, and MTIOC0C pins in the high-impedance state.
POECR1	PE3ZE	MTIOC0D high-impedance enable bit	—
ICSR3	OSTSTE	OSTST high-impedance enable bit 0: Does not place the MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D pins in the high-impedance state 1: Places the MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D pins in the high-impedance state	OSTST high-impedance enable bit 0: Does not place the MTIOC0A, MTIOC0B, MTIOC0C, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D pins in the high-impedance state 1: Places the MTIOC0A, MTIOC0B, MTIOC0C, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, and MTIOC4D pins in the high-impedance state

2.15 16-Bit Timer Pulse Unit

Table 2.41 is a comparative overview of the 16-bit timer pulse units, and Table 2.42 is a comparison of 16-bit timer pulse unit registers.

Table 2.41 Comparative Overview of 16-Bit Timer Pulse Units

Item	RX231 (TPUa)	RX23W (TPUa)
Pulse input/output	Max. 16 lines	Max. 10 lines
Count clock	Seven and eight clocks for each channel	Seven and eight clocks for each channel
Available operations	• Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation • Cascaded operation	• Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Synchronous register input/output by synchronous counter operation • Up to 9-phase PWM output in combination with synchronous operation • Cascaded operation
Buffer operation	• Channels 0 and 3 • Automatic transfer of register data	• Channels 0 and 3 • Automatic transfer of register data
Phase coefficient mode	Channels 1, 2, 4, and 5	Channels 1, 2, 4, and 5
Interrupt sources	26 sources	26 sources
Trigger generation	Ability to generate A/D converter start trigger	Ability to generate A/D converter start trigger
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.42 Comparison of 16-Bit Timer Pulse Unit Registers

Register	Bit	RX231 (TPUa)	RX23W (TPUa)
TMDR	ICSELB	TGRB input capture input select bit 0: Input capture input source is TIOCBn pin. 1: Input capture input source is TIOCAn pin. (n = 0 to 5)	TGRB input capture input select bit 0: Input capture input source is TIOCBn pin. 1: Input capture input source is TIOCAn pin. (n = 3, 4) This bit is reserved on the TPU0, TPU1, TPU2, and TPU5, each of which lack TIOCAn pins. The bit is read as 0. The write value should be 0.

Register	Bit	RX231 (TPUa)	RX23W (TPUa)
TMDR	ICSELD	TGRD input capture input select bit 0: Input capture input source is TIOCDn pin. 1: Input capture input source is TIOCCn pin. (n = 0, 3) This bit is reserved on the TPU1, TPU2, TPU4, and TPU5, each of which lack TGRC and TGRD registers. The bit is read as 0. The write value should be 0.	TGRD input capture input select bit 0: Input capture input source is TIOCDn pin. 1: Input capture input source is TIOCCn pin. (n = 3) This bit is reserved on the TPU0, TPU1, TPU2, TPU4, and TPU5, each of which lack TIOCCn and TIOCDn pins. The bit is read as 0. The write value should be 0.
TIORH	IOA[3:0]	TGRA control bits	TGRA control bits This bit is reserved on the TPU0, TPU1, TPU2, and TPU5, each of which lack TIOCAn pins. The bit is read as 0.
NFCR	NFAEN	Noise filter enable A bit 0: The noise filter for TIOCAm is disabled. 1: The noise filter for TIOCAm is enabled. (m = 0 to 5)	Noise filter enable A bit 0: The noise filter for TIOCAm is disabled. 1: The noise filter for TIOCAm is enabled. (m = 3, 4) This bit is reserved on the TPU0, TPU1, TPU2, TPU4, and TPU5. The bit is read as 0. It cannot be written to.
	NFCEN	Noise filter enable C bit 0: The noise filter for TIOCCm is disabled. 1: The noise filter for TIOCCm is enabled. (m = 0, 3) This bit is reserved on the TPU1, TPU2, TPU4, and TPU5. The bit is read as 0. It cannot be written to.	Noise filter enable C bit 0: The noise filter for TIOCCm is disabled. 1: The noise filter for TIOCCm is enabled. (m = 3) This bit is reserved on the TPU0, TPU1, TPU2, and TPU5. The bit is read as 0. It cannot be written to.
	NFDEN	Noise filter enable D bit 0: The noise filter for TIOCDm is disabled. 1: The noise filter for TIOCDm is enabled. (m = 0, 3) This bit is reserved on the TPU1, TPU2, TPU4, and TPU5. The bit is read as 0. It cannot be written to.	Noise filter enable D bit 0: The noise filter for TIOCDm is disabled. 1: The noise filter for TIOCDm is enabled. (m = 3) This bit is reserved on the TPU0, TPU1, TPU2, and TPU5. The bit is read as 0. It cannot be written to.

2.16 8-Bit Timer

Table 2.43 is a comparison of 8-bit timer registers.

Table 2.43 Comparison of 8-Bit Timer Registers

Register	Bit	RX231 (TMR)	RX23W (TMR)
TCR	CCLR[1:0]	Counter clear bits b4 b3 0 0: Clearing is disabled 0 1: Cleared by compare match A 1 0: Cleared by compare match B 1 1: Cleared by external counter reset signal (Select edge or level with TCCR.TMRIS bit.)	Counter clear bits b4 b3 0 0: Clearing is disabled 0 1: Cleared by compare match A 1 0: Cleared by compare match B 1 1: Cleared by external counter reset signal*1 (Select edge or level with TCCR.TMRIS bit.)
TCCR	TMRIS	Timer reset detection condition select bit	Timer reset detection condition select bit This bit is reserved on the TMR0. The bit is read as 0. The write value should be 0.

Note: 1. Do not use this setting on TMR0.

2.17 Realtime Clock

Table 2.44 is a comparison of realtime clock registers.

Table 2.44 Comparison of Realtime Clock Registers

Register	Bit	RX231 (RTCe)	RX23W (RTCe)
RTCCRn	—	Time capture control register n (n = 0 to 2)	Time capture control register n (n = 0 or 1)
RSECCPn/ BCNT0CPn	—	Second capture register n/BCNT0 capture register n (n = 0 to 2)	Second capture register n/BCNT0 capture register n (n = 0 or 1)
RMINCPn/ BCNT1CPn	—	Minute capture register n/BCNT1 capture register n (n = 0 to 2)	Minute capture register n/BCNT1 capture register n (n = 0 or 1)
RHRCPn/ BCNT2CPn	—	Hour capture register n/BCNT2 capture register n (n = 0 to 2)	Hour capture register n/BCNT2 capture register n (n = 0 or 1)
RDAYCPn/ BCNT3CPn	—	Day capture register n/BCNT3 capture register n (n = 0 to 2)	Day capture register n/BCNT3 capture register n (n = 0 or 1)
RMONCPn	—	Month capture register n (n = 0 to 2)	Month capture register n (n = 0 or 1)

2.18 USB 2.0 Host/Function Module

Table 2.45 is a comparison of USB 2.0 Host/Function module registers.

Table 2.45 Comparison of USB 2.0 Host/Function Module Registers

Register	Bit	RX231 (USBd)	RX23W (USBc)
USBMC	VDCEN	USB regulator on/off control bit	—

2.19 Serial Communications Interface

Table 2.46 is a comparative overview of the serial communications interfaces, Table 2.47 is a comparison of SCI channel specifications, and Table 2.48 is a comparison of serial communications interface registers.

Table 2.46 Comparative Overview of Serial Communications Interfaces

Item		RX231 (SCIg, SCIh)	RX23W (SCIg, SCIh)
Number of channels		• SCIg: 6 channels • SCIh: 1 channel	• SCIg: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI12).

Item		RX231 (SCIg, SCIh)	RX23W (SCIg, SCIh)
Asynchronous mode	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX231 (SCIg, SCIh)	RX23W (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error, error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error, error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.47 Comparison of SCI Channel Specifications

Item	RX231 (SCIg, SCIh)	RX23W (SCIg, SCIh)
Synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI8, SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI8, SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI8, SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI8, SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI8, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI12
Event link function	SCI5	SCI5

Table 2.48 Comparison of Serial Communications Interface Registers

Register	Bit	RX231 (SCIg, SCIh)	RX23W (SCIg, SCIh)
SCR	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP = 1) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP = 1) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.

2.20 Serial Peripheral Interface

Table 2.49 is a comparative overview of the serial peripheral interfaces, and Table 2.50 is a comparison of serial peripheral interface registers.

Table 2.49 Comparative Overview of Serial Peripheral Interfaces

Item	RX231 (RSPIa)	RX23W (RSPIa)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/ reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/ reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection

Item	RX231 (RSPIa)	RX23W (RSPIa)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity	• Three SSL pins (SSLA0, SSLA1, and SSLA3) for each channel • In single-master mode, SSLA1 and SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 and SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 and SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)

Item	RX231 (RSPIa)	RX23W (RSPIa)
Event link function (output)	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, or parity error signal • RSPI idle signal • Transmission-completed signal	The following events can be output to the event link controller. (RSPI0) • Receive buffer full signal • Transmit buffer empty signal • Mode fault, overrun, or parity error signal • RSPI idle signal • Transmission-completed signal
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.50 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX231 (RSPIa)	RX23W (RSPIa)
SSLP	SSL2P	SSL2 signal polarity setting bit	—
SPCMDm (m = 0 to 7)	SSLA[2:0]	SSL signal assertion setting bits b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited.	SSL signal assertion setting bits b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 1: SSL3 Settings other than the above are prohibited.

2.21 Capacitive Touch Sensing Unit

Table 2.51 is a comparative overview of the capacitive touch sensing units, and Table 2.52 is a comparison of capacitive touch sensing unit registers.

Table 2.51 Comparative Overview of Capacitive Touch Sensing Units

Item		RX231 (CTSU)	RX23W (CTSU)
Operating clock		PCLK, PCLK/2, or PCLK/4	PCLK, PCLK/2, or PCLK/4
Pins	Electrostatic capacitance measurement pins	TS00, TS01, TS02, TS03, TS04, TS05, TS06, TS07, TS08, TS09, TS12, TS13, TS15, TS16, TS17, TS18, TS19, TS20, TS22, TS23, TS27, TS30, TS33, TS35 (24 channels)	TS2, TS3, TS4, TS7, TS8, TS12, TS13, TS22, TS23, TS27, TS30, TS35 (12 channels)
	Low-pass filter (LPF) connection pin	TSCAP	TSCAP
Measurement modes		• Self-capacitance single scan mode: Electrostatic capacitance on one channel is measured by the self-capacitance method. • Self-capacitance multi-scan mode: Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method. • Mutual capacitance full scan mode: Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.	• Self-capacitance single scan mode: Electrostatic capacitance on one channel is measured by the self-capacitance method. • Self-capacitance multi-scan mode: Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method. • Mutual capacitance full scan mode: Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.
Noise prevention		Synchronous noise prevention, high-range noise prevention	Synchronous noise prevention, high-range noise prevention
Measurement start conditions		• Software trigger • External trigger (event input from event link controller (ELC))	• Software trigger • External trigger (event input from event link controller (ELC))

Table 2.52 Comparison of Capacitive Touch Sensing Unit Registers

Register	Bit	RX231 (CTSU)	RX23W (CTSU)
CTSUMCH0	CTSUMCH0 [5:0]	CTSU measurement channel 0 bits • Self-capacitance single scan mode b5 b0 0 0 0 0 0 0: TS0 0 0 0 0 0 1: TS1 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set.	CTSU measurement channel 0 bits • Self-capacitance single scan mode b5 b0 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set.

Register	Bit	RX231 (CTSU)	RX23W (CTSU)
CTSUMCH0	CTSUMCH0 [5:0]	• Measurement modes other than self-capacitance single scan b5 b0 0 0 0 0 0 0: TS0 0 0 0 0 0 1: TS1 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement stopped	• Measurement modes other than self-capacitance single scan b5 b0 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement stopped
CTSUMCH1	CTSUMCH1 [5:0]	CTSU measurement channel 1 bits b5 b0 0 0 0 0 0 0: TS0 0 0 0 0 0 1: TS1 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 0 0 1: TS9 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 0 1 1 1 1: TS15 : : 0 1 0 1 0 0: TS20 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 0 1: TS33 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement stopped	CTSU measurement channel 1 bits b5 b0 0 0 0 0 1 0: TS2 0 0 0 0 1 1: TS3 0 0 0 1 0 0: TS4 0 0 0 1 1 1: TS7 0 0 1 0 0 0: TS8 0 0 1 1 0 0: TS12 0 0 1 1 0 1: TS13 0 1 0 1 1 0: TS22 0 1 0 1 1 1: TS23 0 1 1 0 1 1: TS27 0 1 1 1 1 0: TS30 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement stopped

Register	Bit	RX231 (CTSU)	RX23W (CTSU)
CTSUCHAC0	CTSUCHAC00	CTSU channel enable control 00 bit	—
	CTSUCHAC01	CTSU channel enable control 01 bit	—
	CTSUCHAC02	CTSU channel enable control 02 bit	CTSU channel enable control 02 bit
	CTSUCHAC03	CTSU channel enable control 03 bit	CTSU channel enable control 03 bit
	CTSUCHAC04	CTSU channel enable control 04 bit	CTSU channel enable control 04 bit
	CTSUCHAC05	CTSU channel enable control 05 bit	—
	CTSUCHAC06	CTSU channel enable control 06 bit	—
	CTSUCHAC07	CTSU channel enable control 07 bit	CTSU channel enable control 07 bit
CTSUCHAC1	CTSUCHAC10	CTSU channel enable control 10 bit	CTSU channel enable control 08 bit
	CTSUCHAC11	CTSU channel enable control 11 bit	—
	CTSUCHAC12	CTSU channel enable control 12 bit	—
	CTSUCHAC13	CTSU channel enable control 13 bit	—
	CTSUCHAC14	CTSU channel enable control 14 bit	CTSU channel enable control 12 bit
	CTSUCHAC15	CTSU channel enable control 15 bit	CTSU channel enable control 13 bit
	CTSUCHAC16	CTSU channel enable control 16 bit	—
	CTSUCHAC17	CTSU channel enable control 17 bit	—
CTSUCHAC2	CTSUCHAC20	CTSU channel enable control 20 bit	—
	CTSUCHAC21	CTSU channel enable control 21 bit	—
	CTSUCHAC22	CTSU channel enable control 22 bit	—
	CTSUCHAC23	CTSU channel enable control 23 bit	—
	CTSUCHAC24	CTSU channel enable control 24 bit	—
	CTSUCHAC25	CTSU channel enable control 25 bit	—
	CTSUCHAC26	CTSU channel enable control 26 bit	CTSU channel enable control 22 bit
	CTSUCHAC27	CTSU channel enable control 27 bit	CTSU channel enable control 23 bit
CTSUCHAC3	CTSUCHAC30	CTSU channel enable control 30 bit	—
	CTSUCHAC31	CTSU channel enable control 31 bit	—
	CTSUCHAC32	CTSU channel enable control 32 bit	—

Register	Bit	RX231 (CTSU)	RX23W (CTSU)
CTSUCHAC3	CTSUCHAC33	CTSU channel enable control 33 bit	CTSU channel enable control 27 bit
	CTSUCHAC34	CTSU channel enable control 34 bit	—
	CTSUCHAC35	CTSU channel enable control 35 bit	—
	CTSUCHAC36	CTSU channel enable control 36 bit	CTSU channel enable control 30 bit
	CTSUCHAC37	CTSU channel enable control 37 bit	—
CTSUCHAC4	CTSUCHAC40	CTSU channel enable control 40 bit	—
	CTSUCHAC41	CTSU channel enable control 41 bit	—
	CTSUCHAC42	CTSU channel enable control 42 bit	—
	CTSUCHAC43	CTSU channel enable control 43 bit	CTSU channel enable control 35 bit
CTSUCHTRC0	CTSUCHTRC00	CTSU channel transmit/receive control 00 bit	—
	CTSUCHTRC01	CTSU channel transmit/receive control 01 bit	—
	CTSUCHTRC02	CTSU channel transmit/receive control 02 bit	CTSU channel transmit/receive control 02 bit
	CTSUCHTRC03	CTSU channel transmit/receive control 03 bit	CTSU channel transmit/receive control 03 bit
	CTSUCHTRC04	CTSU channel transmit/receive control 04 bit	CTSU channel transmit/receive control 04 bit
	CTSUCHTRC05	CTSU channel transmit/receive control 05 bit	—
	CTSUCHTRC06	CTSU channel transmit/receive control 06 bit	—
	CTSUCHTRC07	CTSU channel transmit/receive control 07 bit	CTSU channel transmit/receive control 07 bit
CTSUCHTRC1	CTSUCHTRC10	CTSU channel transmit/receive control 10 bit	CTSU channel transmit/receive control 08 bit
	CTSUCHTRC11	CTSU channel transmit/receive control 11 bit	—
	CTSUCHTRC12	CTSU channel transmit/receive control 12 bit	—
	CTSUCHTRC13	CTSU channel transmit/receive control 13 bit	—
	CTSUCHTRC14	CTSU channel transmit/receive control 14 bit	CTSU channel transmit/receive control 12 bit
	CTSUCHTRC15	CTSU channel transmit/receive control 15 bit	CTSU channel transmit/receive control 13 bit
	CTSUCHTRC16	CTSU channel transmit/receive control 16 bit	—
	CTSUCHTRC17	CTSU channel transmit/receive control 17 bit	—
CTSUCHTRC2	CTSUCHTRC20	CTSU channel transmit/receive control 20 bit	—
	CTSUCHTRC21	CTSU channel transmit/receive control 21 bit	—

Register	Bit	RX231 (CTSU)	RX23W (CTSU)
CTSUCHTRC2	CTSUCHTRC22	CTSU channel transmit/receive control 22 bit	—
	CTSUCHTRC23	CTSU channel transmit/receive control 23 bit	—
	CTSUCHTRC24	CTSU channel transmit/receive control 24 bit	—
	CTSUCHTRC25	CTSU channel transmit/receive control 25 bit	—
	CTSUCHTRC26	CTSU channel transmit/receive control 26 bit	CTSU channel transmit/receive control 22 bit
	CTSUCHTRC27	CTSU channel transmit/receive control 27 bit	CTSU channel transmit/receive control 23 bit
CTSUCHTRC3	CTSUCHTRC30	CTSU channel transmit/receive control 30 bit	—
	CTSUCHTRC31	CTSU channel transmit/receive control 31 bit	—
	CTSUCHTRC32	CTSU channel transmit/receive control 32 bit	—
	CTSUCHTRC33	CTSU channel transmit/receive control 33 bit	CTSU channel transmit/receive control 27 bit
	CTSUCHTRC34	CTSU channel transmit/receive control 34 bit	—
	CTSUCHTRC35	CTSU channel transmit/receive control 35 bit	—
	CTSUCHTRC36	CTSU channel transmit/receive control 36 bit	CTSU channel transmit/receive control 30 bit
	CTSUCHTRC37	CTSU channel transmit/receive control 37 bit	—
CTSUCHTRC4	CTSUCHTRC40	CTSU channel transmit/receive control 40 bit	—
	CTSUCHTRC41	CTSU channel transmit/receive control 41 bit	—
	CTSUCHTRC42	CTSU channel transmit/receive control 42 bit	—
	CTSUCHTRC43	CTSU channel transmit/receive control 43 bit	CTSU channel transmit/receive control 35 bit

2.22 12-Bit A/D Converter

Table 2.53 is a comparative overview of the 12-bit A/D converters, and Table 2.54 is a comparison of 12-bit A/D converter registers.

Table 2.53 Comparative Overview of 12-Bit A/D Converters

Item	RX231 (S12ADE)	RX23W (S12ADE)
Number of units	1 unit	1 unit
Input channels	24 channels	14 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.83 μs per channel (when A/D conversion clock ADCLK = 54 MHz)	0.83 μs per channel (when A/D conversion clock ADCLK = 54 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 24 registers for analog input, 1 for A/D-converted data duplication in double trigger mode • One register for temperature sensor • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 14 registers for analog input, 1 for A/D-converted data duplication in double trigger mode. • One register for temperature sensor • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX231 (S12ADE)	RX23W (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 24 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 24 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be set.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 14 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 14 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 14 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), the event link controller (ELC), or the 16-bit timer pulse unit (TPU). • Asynchronous trigger • A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), the event link controller (ELC), or the 16-bit timer pulse unit (TPU). • Asynchronous trigger • A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX231 (S12ADE)	RX23W (S12ADE)
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).

Item	RX231 (S12ADE)	RX23W (S12ADE)
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.54 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX231 (S12ADE)	RX23W (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 7, 16 to 31)	A/D data register y (y = 0 to 7, 16 to 20, 27)
ADANSA1	ANSA1n	A/D conversion channel select bit (n = 00 to 15)	A/D conversion channel select bit (n = 00 to 04, 11)
ADANSB1	ANSB1n	A/D conversion channel select bit (n = 00 to 15)	A/D conversion channel select bit (n = 00 to 04, 11)
ADADS1	ADS1n	A/D-converted value addition/ average channel select bit (n = 00 to 15)	A/D-converted value addition/ average channel select bit (n = 00 to 04, 11)
ADCMPANSR1	CMPCHA1n	Compare window A channel select bit (n = 00 to 15)	Compare window A channel select bit (n = 00 to 04, 11)
ADCMPLR1	CMPLCHA1n	Compare window A comparison condition select bit (n = 00 to 15)	Compare window A comparison condition select bit (n = 00 to 04, 11)
ADCMPSR1	CMPSTCHA1n	Compare window A flag (n = 00 to 15)	Compare window A flag (n = 00 to 04, 11)
ADCMPBNSR	CMPCHB [5:0]	Compare window B channel select bits b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 0 1 0 0: AN020 : 0 1 1 0 1 1: AN027 0 1 1 1 0 0: AN028 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.	Compare window B channel select bits b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 0 1 0 0: AN020 0 1 1 0 1 1: AN027 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.

2.23 12-Bit D/A Converter

Table 2.55 is a comparison of 12-bit D/A converter registers.

Table 2.55 Comparison of 12-Bit D/A Converter Registers

Register	Bit	RX231 (R12DAA)	RX23W (R12DAA)
DAVREFCR	REF[2:0]	D/A reference voltage select bits b2 b0 0 0 0: Not selected 0 0 1: AVCC0/AVSS0 0 1 1: Internal reference voltage/ AVSS0 1 1 0: VREFH/VREFL Settings other than the above are prohibited.	D/A reference voltage select bits b2 b0 0 0 0: Not selected 0 0 1: AVCC0/AVSS0 0 1 1: Internal reference voltage/ AVSS0 Settings other than the above are prohibited.

2.24 Comparator B

Table 2.56 is a comparative overview of the comparator B modules, and Table 2.57 is a comparison of comparator B registers.

Table 2.56 Comparative Overview of Comparator B Modules

Item	RX231 (CMPBa)	RX23W (CMPBa)
Number of channels	2 channels × 2 units	2 channels × 1 unit
Analog input voltage	Voltage input to CMPBn pin (n = 0 to 3)	Voltage input to CMPBn pin (n = 2 or 3)
Reference input voltage	Voltage input to CVREFBn pin (n = 0 to 3) or internal reference voltage	Voltage input to CVREFBn pin (n = 2 or 3) or internal reference voltage
Comparison result	• Read from the CPBFLG.CPBnOUT flag (n = 0 to 3) • Ability to output comparison result to CMPOBn pin (n = 0 to 3).	• Read from the CPBFLG.CPBnOUT flag (n = 2 or 3) • Ability to output comparison result to CMPOBn pin (n = 2 or 3).
Interrupt request generation timing	• When comparator B0 comparison result changes • When comparator B1 comparison result changes • When comparator B2 comparison result changes • When comparator B3 comparison result changes	• When comparator B2 comparison result changes • When comparator B3 comparison result changes
Timing of event generation to ELC	• When comparator B0 comparison result changes • When comparator B0 or comparator B1 comparison result changes	—
Selectable functions	• Digital filter function Ability to specify whether or not the digital filter is applied and to select the sampling frequency • Window function Ability to specify whether or the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0 to 3) < high-side reference (VRFH)) • Reference input voltage Ability to select CVREFBn pin (n = 0 to 3) input or internal reference voltage (generated internally) • Comparator B response speed Ability to select high-speed or low-speed mode	• Digital filter function Ability to specify whether or not the digital filter is applied and to select the sampling frequency • Window function Ability to specify whether or the window function is enabled or disabled (VRFL < CMPBn (n = 2 or 3) < VRFH) • Reference input voltage Ability to select CVREFBn pin (n = 2 or 3) input or internal reference voltage (generated internally) • Comparator B response speed Ability to select high-speed or low-speed mode
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.57 Comparison of Comparator B Registers

Register	Bit	RX231 (CMPBa)	RX23W (CMPBa)
CPBCNT1	—	Comparator B control register 1	—
CPBCNT2	—	Comparator B control register 2	—
CPBFLG	—	Comparator B flag register	—
CPBINT	—	Comparator B interrupt control register	—
CPBF	—	Comparator B filter select register	—
CPBMD	—	Comparator B mode select register	—
CPBREF	—	Comparator B reference input voltage select register	—
CPBOCR	—	Comparator B output control register	—

2.25 RAM

Table 2.58 is a comparative overview of RAM.

Table 2.58 Comparative Overview of RAM

Item	RX231	RX23W
Capacity	• 64 KB (0000 0000h to 0000 FFFFh) • 32 KB (0000 0000h to 0000 7FFFh)	• 64 KB (0000 0000h to 0000 FFFFh)
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.26 Flash Memory

Table 2.59 is a comparative overview of flash memory.

Table 2.59 Comparative Overview of Flash Memory

Item	RX231	RX23W (FLASH)
Memory capacity	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh
Software commands	• The following commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.

Item	RX231	RX23W (FLASH)
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Boot mode (USB interface) — Channel 0 of the USB 2.0 Function (USB0) module is used. — The user area and data area can be programmed. — The flash memory can be programmed in self-powered or bus-powered mode. — A personal computer can be connected using only a USB cable. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Boot mode (USB interface) — Channel 0 of the USB 2.0 Function (USB0) module is used. — The user area and data area can be programmed. — The flash memory can be programmed in self-powered or bus-powered mode. — A personal computer can be connected using only a USB cable. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming	The user area and data area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes. • Connection with a parallel programmer can be controlled using ROM codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 7.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	Programs in the ROM can run while the E2 DataFlash is being programmed.	Programs in the ROM can run while the E2 DataFlash is being programmed.

2.27 Packages

As indicated in Table 2.60, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.60 Packages

Package Type	Renesas Code	
	RX231	RX23W
100-pin TFLGA	○	×
100-pin LFQFP	○	×
85-pin BGA	×	○
83-pin LGA	×	○
64-pin WFLGA	○	×
64-pin HWQFN	○	×
64-pin LFQFP	○	×
56-pin QFN	×	○
48-pin HWQFN	○	×
48-pin LFQFP	○	×

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by blue text. Items that exists on both groups with different specifications are indicated by red text. **Black text** indicates there is no differences in the item's specifications between groups.

The RX23W Group and RX231 Group do not include packages with the same pin count, but with some exceptions the pin functions are compatible. The pin design therefore makes migration relatively easy.

3.1 100-Pin Package (RX231: TFLGA)/85-Pin Package (RX23W: BGA)

Table 3.1 lists the pin functions of the 100-pin package (RX231: TFLGA) and 85-pin package (RX23W: BGA) products.

Table 3.1 100-Pin Package (RX231: TFLGA)/85-Pin Package (RX23W: BGA)

100-Pin TFLGA	85-Pin BGA	RX231 (100-Pin TFLGA)	RX23W (85-Pin BGA)
A1	B9	P05/DA1	P05/DA1
A2	—	VREFH	—
A3	C7	P07/ADTRG0#	P07/ADTRG0#
A4	D10	VREFL0	VREFL0
A5	D9	P43/AN003	P43/AN003
A6	—	PD0/D0[A0/D0]/IRQ0/AN024	—
A7	—	PD4/D4[A4/D4]/POE3#/IRQ4/AN028	—
A8	G9	PE0/D8[A8/D8]/SCK12/AN016	PE0/SCK12/AN016
A9	J9	PE1/D9[A9/D9]/MTIOC4C/TXD12/ TXDX12/SIOX12/SMOSI12/SSDA12/ AN017/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017
A10	H9	PE2/D10[A10/D10]/MTIOC4A/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7/ AN018/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/ SMISO12/SSCL12/IRQ7/AN018
B1	B8	P03/DA0	P03/DA0
B2	A10	AVSS0	AVSS0
B3	B10	AVCC0	AVCC0
B4	C9	P40/AN000	P40/AN000
B5	E10	P44/AN004	P44/AN004
B6	—	PD1/D1[A1/D1]/MTIOC4B/IRQ1/AN025	—
B7	F9	PD3/D3[A3/D3]/POE8#/IRQ3/AN027	PD3/POE8#/AN027
B8	—	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/ AN030	—
B9	—	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/ AN031	—
B10	H8	PE3/D11[A11/D11]/MTIOC4B/POE8#/ CTS12#/RTS12#/SS12#/AUDIO_MCLK/ AN019/CLKOUT	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ SS12#/AUDIO_MCLK/AN019/CLKOUT
C1	A9	VCL	VCL
C2	—	VREFL	—
C3	C6	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/MTIOC3C
C4	C10	VREFH0	VREFH0
C5	D8	P42/AN002	P42/AN002
C6	F10	P47/AN007	CLKOUT_RF/P47/AN007
C7	—	PD2/D2[A2/D2]/MTIOC4D/IRQ2/AN026	—

100-Pin TFLGA	85-Pin BGA	RX231 (100-Pin TFLGA)	RX23W (85-Pin BGA)
C8	—	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN029	—
C9	—	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	—
C10	J8	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/AN020/CLKOUT
D1	A8	XCIN	XCIN
D2	A7	XCOUT	XCOUT
D3	B7	MD/FINED	MD/FINED
D4	C5	VBATT	VBATT
D5	E9	P45/AN005	P45/AN005
D6	E8	P46/AN006	P46/AN006
D7	—	PE6/D14[A14/D14]/IRQ6/AN022	—
D8	—	PE7/D15[A15/D15]/IRQ7/AN023	—
D9	—	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	—
D10	—	PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF	—
E1	A6	XTAL/P37	XTAL/P37
E2	A5	VSS	VSS
E3	B6	RES#	RES#
E4	—	P34/MTIOC0A/TMCI3/POE2#/SCK6/TS0/IRQ4	—
E5	C8	P41/AN001	P41/AN001
E6	—	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	—
E7	—	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	—
E8	—	PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	—
E9	—	PA5/A5/TIOCB1/RSPCKA	—
E10	—	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	—
F1	A4	EXTAL/P36	EXTAL/P36
F2	A3	VCC	VCC
F3	B5	UPSEL/P35/NMI	UPSEL/P35/NMI
F4	—	P32/MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/USB0_VBUSEN/IRQ2	—
F5	—	P12/TMCI1/SCL/IRQ2	—
F6	H4	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SDHI_WP
F7	—	PB2/A10/TIOCC3/TCLKC/CTS6#/RTS6#/SS6#	—
F8	J6	PB0/A8/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CMD	PB0/MTIC5W/TIOCA3/RSPCKA/SDHI_CMD
F9	—	PA7/A7/TIOCB2/MISOA	—
F10	K5	VSS	VSS

100-Pin TFLGA	85-Pin BGA	RX231 (100-Pin TFLGA)	RX23W (85-Pin BGA)
G1	—	P33/MTIOC0D/TMRI3/POE3#/TIOCD0/ RXD6/SMISO6/SSCL6/TS1/IRQ3	—
G2	B4	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSISCK0/IRQ1	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSISCK0/IRQ1
G3	A2	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/AUDIO_MCLK/ IRQ0/CMPOB3	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/AUDIO_MCLK/ IRQ0/CMPOB3
G4	B3	P27/CS3#/MTIOC2B/TMCI3/SCK1/ SSIWS0/TS2/CVREFB3	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/ TS2/CVREFB3
G5	—	BCLK/P53/TS17	—
G6	—	P52/RD#/TS18	—
G7	J4	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4/SCK9/USB0_VBUS/ SDHI_CD	PB5/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4/USB0_VBUS/SDHI_CD
G8	—	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#	—
G9	J5	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/TXD6/SMOSI6/SSDA6/ SDHI_CLK/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/SDHI_CLK/IRQ4
G10	K4	VCC	VCC
H1	B2	P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/SSIRXD0/TS3/CMPB3	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/SSIRXD0/USB0_VBUSEN/TS3/ CMPB3
H2	A1	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/ TS4/ADTRG0#	P25/MTIOC4C/MTCLKB/TIOCA4/TS4/ ADTRG0#
H3	C3	P16/MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
H4	C2	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/ TCLKB/RXD1/SMISO1/SSCL1/CRXD0/ TS12/IRQ5/CMPB2	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/ TCLKB/RXD1/SMISO1/SSCL1/CRXD0/ TS12/IRQ5/CMPB2
H5	—	P55/WAIT#/MTIOC4D/TMO3/CRXD0/ TS15	—
H6	—	P54/ALE/MTIOC4B/TMCI1/CTXD0/TS16	—
H7	F1	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TXD8/SMOSI8/SSDA8/MISOA/ CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ TXD8/SMOSI8/SSDA8/MISOA/CACREF
H8	F2	PC6/A22/CS1#/MTIOC3C/MTCLKA/ TMCI2/RXD8/SMISO8/SSCL8/MOSIA/ TS22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA/USB0_EXICEN/ TS22
H9	—	PB6/A14/MTIOC3D/TIOCA5/RXD9/ SMISO9/SSCL9/SDHI_D1	—
H10	J3	PB7/A15/MTIOC3B/TIOCB5/TXD9/ SMOSI9/SSDA9/SDHI_D2	PB7/MTIOC3B/TIOCB5/SDHI_D2
J1	—	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/ TIOCB4/USB0_VBUSEN/TS5	—
J2	D3	P21/MTIOC1B/TMCI0/TIOCA3/RXD0/ SMISO0/SSCL0/USB0_EXICEN/ SSIWS0/TS8	P21/MTIOC1B/TMCI0/TIOCA3/ USB0_EXICEN/SSIWS0/TS8
J3	B1	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA/ SSITXD0/IRQ7/CMPOB2	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA/ SSITXD0/IRQ7/CMPOB2

100-Pin TFLGA	85-Pin BGA	RX231 (100-Pin TFLGA)	RX23W (85-Pin BGA)
J4	—	P13/MTIOC0B/TMO3/TIOCA5/SDA/ IRQ3	—
J5	E2	VSS_USB	VSS_USB
J6	D2	VCC_USB	VCC_USB
J7	—	P50/WR0#/WR#/TS20	—
J8	G1	PC4/A20/CS3#/MTIOC3D/MTCLKC/ TMCI1/POE0#/SCK5/CTS8#/RTS8#/ SS8#/SSLA0/SDHI_D1/TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ CTS8#/RTS8#/SS8#/SSLA0/SCK5/ SDHI_D1/TSCAP
J9	J1	PC0/A16/MTIOC3C/TCLKC/CTS5#/ RTS5#/SS5#/SSLA1/TS35	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/ SS5#/SSLA1/TS35
J10	—	PC1/A17/MTIOC3A/TCLKD/SCK5/ SSLA2/TS33	—
K1	—	P23/MTIOC3D/MTCLKD/TIOCD3/ CTS0#/RTS0#/SS0#/SSISCK0/TS6	—
K2	C4	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/ SCK0/USB0_OVRCURB/AUDIO_MCLK/ TS7	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/ USB0_OVRCURB/AUDIO_MCLK/TS7
K3	—	P20/MTIOC1A/TMRI0/TIOCB3/TXD0/ SMOSI0/SSDA0/USB0_ID/SSIRXD0/ TS9	—
K4	C1	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/ TCLKA/CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA/TS13/IRQ4/ CVREFB2	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/ TCLKA/CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA/TS13/IRQ4/ CVREFB2
K5	D1	USB0_DM	USB0_DM
K6	E1	USB0_DP	USB0_DP
K7	—	P51/WR1#/BC1#/WAIT#/TS19	—
K8	G2	PC5/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/SCK8/RSPCKA/TS23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA/USB0_ID/TS23
K9	H1	PC3/A19/MTIOC4D/TCLKB/TXD5/ SMOSI5/SSDA5/IRTXD5/SDHI_D0/ TS27	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/ SSDA5/IRTXD5/SDHI_D0/TS27
K10	H2	PC2/A18/MTIOC4B/TCLKA/RXD5/ SMISO5/SSCL5/SSLA3/IRRXD5/ SDHI_D3/TS30	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/ SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30
—	D4	—	VSS_RF
—	E3	—	VSS_RF
—	F3	—	VSS_RF
—	F8	—	VSS_RF
—	G3	—	VSS_RF
—	G8	—	VSS_RF
—	G10	—	DCLIN_A
—	H3	—	VSS_RF
—	H5	—	VSS_RF
—	H6	—	VSS_RF
—	H7	—	VSS_RF
—	H10	—	DCLIN_D
—	J2	—	VSS_RF
—	J7	—	VSS_RF
—	J10	—	VCC_RF
—	K1	—	VSS_RF
—	K2	—	ANT

100-Pin TFLGA	85-Pin BGA	RX231 (100-Pin TFLGA)	RX23W (85-Pin BGA)
—	K3	—	VSS_RF
—	K6	—	XTAL2_RF
—	K7	—	XTAL1_RF
—	K8	—	AVCC_RF
—	K9	—	DCLOUT
—	K10	—	VSS_RF

3.2 64-Pin Package (RX231: HWQFN)/56-Pin Package (RX23W: QFN)

Table 3.2 lists the pin functions of the 64-pin package (RX231: HWQFN) and 56-pin package (RX23W: QFN) products.

Table 3.2 64-Pin Package (RX231: HWQFN)/56-Pin Package (RX23W: QFN)

64-Pin HWQFN	56-Pin QFN	RX231 (64-Pin HWQFN)	RX23W (56-Pin QFN)
1	—	P03/DA0	—
2	1	VCL	VCL
3	2	MD/FINED	MD/FINED
4	3	XCIN	XCIN
5	4	XCOUT	XCOUT
6	5	RES#	RES#
7	6	XTAL/P37	XTAL/P37
8	7	VSS	VSS
9	8	EXTAL/P36	EXTAL/P36
10	9	VCC	VCC
11	10	UPSEL/P35/NMI	UPSEL/P35/NMI
12	—	VBATT	—
13	11	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSISCK0/IRQ1	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSISCK0/IRQ1
14	12	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/AUDIO_MCLK/ IRQ0/CMPOB3	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/ RXD1/SMISO1/SSCL1/AUDIO_MCLK/ IRQ0/CMPOB3
15	13	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/ TS2/CVREFB3	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/ TS2/CVREFB3
16	14	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/USB0_VBUSEN/SSIRXD0/TS3/ CMPB3	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/SSIRXD0/USB0_VBUSEN/TS3/ CMPB3
17	15	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA/ SSITXD0/IRQ7/CMPOB2	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD/SCK1/MISOA/SDA/ SSITXD0/IRQ7/CMPOB2
18	16	P16/MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT/TXD1/ SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
19	17	P15/MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB/RXD1/SMISO1/ SSCL1/CRXD0/TS12/IRQ5/CMPB2	P15/MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB/RXD1/SMISO1/ SSCL1/CRXD0/TS12/IRQ5/CMPB2
20	18	P14/MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA/TS13/IRQ4/ CVREFB2	P14/MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA/CTS1#/RTS1#/SS1#/ CTXD0/USB0_OVRCURA/TS13/IRQ4/ CVREFB2
21	19	VCC_USB	VCC_USB
22	20	USB0_DM	USB0_DM
23	21	USB0_DP	USB0_DP
24	22	VSS_USB	VSS_USB
25	—	P55/MTIOC4D/TMO3/CRXD0/TS15	—
26	—	P54/MTIOC4B/TMCI1/CTXD0/TS16	—
27	23	UB/PC7/MTIOC3A/MTCLKB/TMO2/ TXD8/SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/MTIOC3A/MTCLKB/TMO2/ TXD8/SMOSI8/SSDA8/MISOA/CACREF

64-Pin HWQFN	56-Pin QFN	RX231 (64-Pin HWQFN)	RX23W (56-Pin QFN)
28	24	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA/ USB0_EXICEN/TS22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/ SMISO8/SSCL8/MOSIA/ USB0_EXICEN/TS22
29	25	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA/USB0_ID/TS23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ RSPCKA/USB0_ID/TS23
30	26	PC4/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/ SSLA0/SDHI_D1/TSCAP	PC4/MTIOC3D/MTCLKC/TMCI1/ POE0#/CTS8#/RTS8#/SS8#/SSLA0/ SCK5/TSCAP
31	27	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/ SSDA5/IRTXD5/SDHI_D0/TS27	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/ SSDA5/IRTXD5/TS27
32	29	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/ SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/ SSCL5/SSLA3/IRRXD5/TS30
33	31	PB7/PC1/MTIOC3B/TIOCB5/TXD9/ SMOSI9/SSDA9/SDHI_D2	PB7/MTIOC3B/TIOCB5
34	—	PB6/PC0/MTIOC3D/TIOCA5/RXD9/ SMISO9/SSCL9/SDHI_D1	—
35	—	PB5/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4/SCK9/USB0_VBUS/ SDHI_CD	—
36	—	PB3/MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD/SCK6/ SDHI_WP	—
37	33	PB1/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/TXD6/SMOSI6/SSDA6/ SDHI_CLK/IRQ4/CMPOB1	PB1/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/IRQ4
38	34	VCC	VCC
39	35	PB0/MTIC5W/TIOCA3/RXD6/SMISO6/ SSCL6/RSPCKA/SDHI_CMD	PB0/TIOCA3/RSPCKA
40	36	VSS	VSS
41	30	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/ TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/ SSIWS0	PC0/MTIOC3C/TCLKC/CTS5#/RTS5#/ SS5#/SSLA1/TS35
42	—	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/ TXD5/SMOSI5/SSDA5/SSLA0/ SSITXD0/IRTXD5/IRQ5/CVREFB1	—
43	—	PA3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/RXD5/SMISO5/SSCL5/ SSIRXD0/IRRXD5/IRQ6/CMPB1	—
44	—	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/ SSLA2/SSISCK0	—
45	—	PA0/MTIOC4A/TIOCA0/SSLA1/ CACREF	—
46	—	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0	—
47	41	PE4/MTIOC4D/MTIOC1A/AN020/ CMPA2/CLKOUT	PE4/MTIOC4D/MTIOC1A/AN020/ CLKOUT
48	42	PE3/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/AUDIO_MCLK/AN019/ CLKOUT	PE3/MTIOC4B/POE8#/AUDIO_MCLK/ AN019/CLKOUT
49	43	PE2/MTIOC4A/RXD12/RXDX12/ SMISO12/SSCL12/IRQ7/AN018/ CVREFB0	PE2/MTIOC4A/IRQ7/AN018

64-Pin HWQFN	56-Pin QFN	RX231 (64-Pin HWQFN)	RX23W (56-Pin QFN)
50	—	PE1/MTIOC4C/TXD12/TXDX12/ SIOX12/SMOSI12/SSDA12/AN017/ CMPB0	—
51	—	PE0/SCK12/AN016	—
52	—	VREFL	—
53	49	P46/AN006	P46/AN006
54	—	VREFH	—
55	—	P44/AN004	—
56	—	P43/AN003	—
57	—	P42/AN002	—
58	51	P41/AN001	P41/AN001
59	52	VREFL0	VREFL0
60	—	P40/AN000	—
61	53	VREFH0	VREFH0
62	54	AVCC0	AVCC0
63	55	P05/DA1	P05/DA1
64	56	AVSS0	AVSS0
—	28	—	VSS_RF
—	32	—	ANT
—	37	—	XTAL2_RF
—	38	—	XTAL1_RF
—	39	—	AVCC_RF
—	40	—	DCLOUT
—	44	—	VCC_RF
—	45	—	DCLIN_D
—	46	—	DCLIN_A
—	47	—	PD3/POE8#/AN027
—	48	—	CLKOUT_RF/P47/AN007
—	50	—	P45/AN005

4. Notes on Migration

With regard to differences between the RX231 Group and RX23W Group, a number of points need to be kept in mind when migrating between MCUs.

4.1, Operating Voltage Range, describes important points related to the operating voltage. 4.2, Notes on Function Settings, describes important points related to software.

4.1 Operating Voltage Range

4.1.1 Power Supply Voltage

The power supply voltage ranges of the RX231 and RX23W are different.

Table 4.1 is a comparison of power supply voltage range specifications.

Table 4.1 Comparison of Power Supply Voltage Range Specifications

Item		RX231	RX23W
Power supply voltage	VCC	1.8 V to 5.5 V*1	1.8 V to 3.6 V*1*4
Analog power supply voltage	AVCC0	1.8 V to 5.5 V*2	1.8 V to 3.6 V*3
	VREFH0	1.8 V to AVCC0	1.8 V to AVCC0
	VREFH	1.8 V to AVCC0	None
USB power supply voltage	VCC_USB	Same potential as VCC	Same potential as VCC
VBATT power supply voltage	VBATT	1.8 V to 5.5 V	1.8 V to 3.6 V
BLE power supply voltage	VCC_RF	None	1.8 V to 3.6 V*4
	AVCC_RF	None	1.8 V to 3.6 V*4

Notes: 1. When USB is not used.
2. VCC ≥ 2.0 V: AVCC0 and VCC may be set independently within the usable range.
VCC < 2.0 V: AVCC0 = VCC
3. VCC > 2.4 V: AVCC0 may be set independently of VCC when AVCC0 ≥ 2.4 V.
VCC ≤ 2.4 V: AVCC0 may be set independently of VCC when AVCC0 ≥ VCC.
4. Ensure that VCC = VCC_RF = AVCC_RF.

4.2 Notes on Function Settings

Software operating on the RX231 Group are compatible with some software on the RX23W Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics are different between the Groups.

This section describes notes on software regarding settings of functions that are different between the RX23W Group and the RX231 Group.

For differences in modules and functions, refer to section 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware listed in section 5, Reference Documents.

4.2.1 Limitations Applying to I/O Port Register Settings

On the RX23W Group an indefinite value is returned when reading the bits in the PDR, PODR, and PMR register corresponding to pins P12, P13, P20, P32, P33, and P34. When writing to these bits, write-back the read value.

4.2.2 8-Bit Timer Cascaded Operation

On the RX23W Group there is no external counter reset input pin for TMR0, so it is not possible to clear the counter by means of an external counter reset signal. Also, there is no compare match output pin for TMR3, so it is not possible to produce compare match output. Therefore, there are some partial differences in cascaded operation between unit 0 and unit 1 on the RX23W Group.

For details, refer to RX23W Group User's Manual: Hardware, listed in section 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX230 Group, RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX23W Group User's Manual: Hardware Rev.1.00 (R01UH0823EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

- TN-RX*-A0198B/E
- TN-RX*-A0214A/E
- TN-RX*-A0217A/E
- TN-RX*-A0227A/E
- TN-RX*-A0224B/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 17, 2019	—	First edition issued
1.10	Dec. 1, 2020	4	1 Table 1.1 Comparison of Built-In Functions of RX23W Group and RX231 Group revised
		6	2.1 Table 2.1 Comparative Overview of Operating Modes revised
		9	2.4 Table 2.6 Comparative Overview of Voltage Detection Circuits revised
		19	2.9 Table 2.15 Comparative Overview of Buses revised
		21	2.10 Table 2.17 Comparative Overview of Event Link Controllers added
		24	2.11 Table 2.20 Comparative Overview of I/O Ports of 64-Pin (RX231) and 56-Pin (RX23W) Products revised
		25	2.11 Table 2.21 Comparison of I/O Port Functions added
		26	2.12 Table 2.23 Comparison of Multiplexed Pin Assignments added
		35 to 39	2.12 Table 2.24 to Table 2.34 added
		39	2.12 Table 2.35 Comparison of Multi-Function Pin Controller Registers revised
		44	2.15 Table 2.41 Comparison of 16-Bit Timer Pulse Unit Registers added
		47	2.17 Table 2.43 Comparison of Realtime Clock Registers revised
		48	2.18 Table 2.44 Comparative Overview of USB 2.0 Host/Function Modules deleted
		52	2.19 Table 2.46 Comparison of SCI Channel Specifications revised
		53	2.20 Table 2.47 Comparative Overview of Serial Peripheral Interfaces revised
		57	2.21 Table 2.50 Comparison of Capacitive Touch Sensing Unit Registers revised
		79	4. Notes on Migration: explanatory text added
		80	4.2 Notes on Function Settings: explanatory text added
		82	Related Technical Updates revised
1.20	Nov. 5, 2021	23	2.10 Event Link Controller Table 2.19 Comparison of Event Link Controller Registers added
		24	2.11 I/O Ports Table 2.20 Comparative Overview of I/O Ports of 100-Pin (RX231) and 85- or 83-Pin (RX23W) Products revised
		26 to 36, 38, 39	2.12 83-pin LGA specifications added
		52	2.19 Table 2.48 Comparison of Serial Communications Interface Registers added
		59 to 61	2.21 Table 2.52 Comparison of Capacitive Touch Sensing Unit Registers revised
		72	2.26 Flash Memory Table 2.59 Comparative Overview of Flash Memory revised
		73	2.27 Packages Table 2.60 Packages revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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