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M16C/63 Group, M16C/65 Group

Differences between M16C/63 and M16C/65

1. Abstract

This document describes differences between M16C/63 100-pin version and M16C/65 100-pin version. Refer to each device's hardware manual for details.

2. Introduction

The explanation of this application note is applied to the following MCUs:

Applicable MCUs: M16C/63 100-pin version, M16C/65 100-pin version

3. Differences

3.1 Differences in Functions

Table 3.1 lists Differences in Functions.

Table 3.1   Differences in Functions [1]

Item		M16C/63	M16C/65
Minimum Instruction Execution Time		50.0 ns (f(BCLK) = 20 MHz, VCC1 = VCC2 = 2.7 to 5.5 V) 200.0 ns (f(BCLK) = 5 MHz, VCC1 = VCC2 = 1.8 to 5.5 V)	31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V)
Operation Frequency/ Supply Voltage		5 MHz/ VCC1 = 1.8 to 5.5 V, VCC2 = 1.8 V to VCC1 20 MHz/ VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1	32 MHz/ VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 to VCC1
Clock	Clock generator	Main clock, Sub clock, 40 MHz on-chip oscillator, 125 kHz on-chip oscillator	Main clock, Sub clock, 40 MHz on-chip oscillator, 125 kHz on-chip oscillator, PLL frequency synthesizer
	Sub clock frequency divider	Divide by 2 and no division selectable in the SCM0 register	No
	Peripheral clock stop selection	f1 provide enabled/disabled selectable in the PCLKSTP1 register	No
Interrupts	Key input interrupt pins	8 pins	4 pins
Timer	Real-time clock	• Count: second, minute, hour, day of the week, month, year • Periodic interrupt: 0.25 s, 0.5 s • Automatic correction function	Count: second, minute, hour, day of the week
A/D Converter	Conversion time	2.15 μs (4.0 V $\leq$ VCC1 $\leq$ 5.5 V; ϕAD $\leq$ 20 MHz)	1.72 μs (4.0 V $\leq$ VCC1 $\leq$ 5.5 V; ϕAD $\leq$ 25 MHz)
	Voltage used	1.8 V $\leq$ Vref = AVcc $\leq$ 5.5 V	3.0 V $\leq$ Vref = AVcc $\leq$ 5.5 V
	Voltage multiplying function	Yes	No

Note:
1.   Refer to the hardware manual for electrical characteristics and more details.

3.2 Pin Characteristics

Table 3.2 lists Differences in Pin Characteristics.

Table 3.2   Differences in Pin Characteristics

M16C/63	M16C/65
P6_0/***TRHO***/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/***RTCOUT***/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$
P10_3/***$\overline{\text{KI7}}$***/AN3	P10_3/AN3
P10_2/***$\overline{\text{KI6}}$***/AN2	P10_2/AN2
P10_1/***$\overline{\text{KI5}}$***/AN1	P10_1/AN1
P10_0/***$\overline{\text{KI4}}$***/AN0	P10_0/AN0

4. Detailed Comparison

4.1 Differences in Protections

Table 4.1 lists Differences in Registers Associated with Protect Function.

Table 4.1 Differences in Registers Associated with Protect Function

Symbol	Address		Bit	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
PRCR	000Ah		0	Protect bit 0 Enable write to registers CM0, CM1, CM2, PCLKR, SCM0, PCLKSTP1 and FRA0	Protect bit 0 Enable write to registers CM0, CM1, CM2, PLC0, PCLKR, and FRA0

4.2 Differences in Voltage Detectors

Table 4.2 lists Differences in Voltage Detectors and Table 4.3 lists Differences in Registers Associated with Voltage Detector.

Table 4.2 Differences in Voltage Detectors

Item	M16C/63	M16C/65
Vdet1 detection levels	4 Levels • 2.20 V (Vdet1_0) • 3.10 V (Vdet1_6) • 3.85 V (Vdet1_B) • 4.45 V (Vdet1_F)	3 Levels • 3.09 V (Vdet1_6) • 3.84 V (Vdet1_B) • 4.44 V (Vdet1_F)

Table 4.3 Differences in Registers Associated with Voltage Detector

Symbol	Address		Bit	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
VD1LS	0028h		3 - 0	Vdet1 select bit [1] 0000: 2.20 V (Vdet1_0) 0110: 3.10 V (Vdet1_6) 1011: 3.85 V (Vdet1_B) 1111: 4.45 V (Vdet1_F) Only set the values listed above.	Vdet1 select bit [1] 0110: 3.09 V (Vdet1_6) 1011: 3.84 V (Vdet1_B) 1111: 4.44 V (Vdet1_F) Only set the values listed above.

Note:
1. These are typical values. Refer to the electrical characteristics in each MCU hardware manual for details.

4.3 Differences in Clock Generators

Table 4.4 lists Differences in Clock Generators and Table 4.5 lists Differences in Registers Associated with Clock Generator.

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Table 4.4   Differences in Clock Generators

Item	M16C/63	M16C/65
PLL frequency synthesizer	No	Yes
Sub clock oscillation method	(1) Set the PU21 bit in the PUR2 register to 0 (P8_4 to P8_7 not pulled high). (2) Set bits PD8_6 and PD8_7 in the PD8 register to 0 (P8_6, P8_7 function as input ports). **(3) Set the CM03 bit to 0 (sub clock on).** (4) Set the CM04 bit to 1 (XCIN-XCOUT oscillation function). (5) Wait until sub clock oscillation stabilizes.	(1) Set the PU21 bit in the PUR2 register to 0 (P8_4 to P8_7 not pulled high). (2) Set bits PD8_6 and PD8_7 in the PD8 register to 0 (P8_6, P8_7 function as input ports). **(3) Set the CM03 bit to 1 (XCIN-XCOUT drive capacity high).** (4) Set the CM04 bit to 1 (XCIN-XCOUT oscillation function). (5) Wait until sub clock oscillation stabilizes.
Sub clock frequency divider	Divide by 2 and no division selectable in the SCM0 register	No
Peripheral clock stop selection	f1 provide enabled/disabled selectable in the PCLKSTP1 register	No

Table 4.5   Differences in Registers Associated with Clock Generator

| Symbol | Address | | Bit | Differences | |
	M16C/63	M16C/65		M16C/63	M16C/65
CM0	0006h		3	XCIN clock stop bit 0: On 1: Off	XCIN-XCOUT drive capacity select bit 0: Low 1: High

			7	System clock select bit
				0: Main clock
				  or on-chip oscillator clock
				1: Sub clock
					System clock select bit
					0: Main clock, PLL clock
					  or on-chip oscillator clock
					1: Sub clock

CM1	0007h		1	Reserved bit	System clock select bit 1 0: Main clock 1: PLL clock
CM2	000Ch		1	System clock select bit 2 0: Main clock 1: On-chip oscillator clock	System clock select bit 2 0: Main clock or PLL clock 1: On-chip oscillator clock
SCM0	0013h	—	—	M16C/63 only	—
PCLKSTP1	0016h	—	—	M16C/63 only	—
PLC0	—	001Ch	—	—	M16C/65 only

4.4 Differences in Processor Modes

Table 4.6 lists Differences in Registers Associated with Processor Mode.

Table 4.6   Differences in Registers Associated with Processor Mode

Symbol	Address		Bit	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
PRG2C	0010h		1	Reserved bit	Internal area expansion bit 1 [1] Program ROM 1 addresses (40000h to 7FFFFh) 0: Disabled 1: Enabled

Note:
1. This bit enables the program ROM 1 (addresses 40000h to 7FFFFh) in the products with more than 512 KB program ROM 1.

4.5 Differences in Interrupts

Table 4.7 lists Differences in Interrupts and Table 4.8 lists Differences in Interrupt Vectors, and Table 4.9 lists Differences in Registers Associated with Interrupts.

Table 4.7   Differences in Interrupts

Item	M16C/63	M16C/65
Key input interrupt pins	8 pins	4 pins

Table 4.8   Differences in Interrupt Vectors

Software Interrupt Number	Vector Address	M16C/63	M16C/65
47	+188 to +191 (00BCh to 00BFh)	UART6 transmit, NACK6, real-time clock alarm	UART6 transmit, NACK6, real-time clock compare

Table 4.9   Differences in Registers Associated with Interrupts

Symbol	Address		Bit	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
KUPIC	004Dh		4	Polarity select bit 0: Select falling edge 1: Select rising edge	No register bit
IFSR3A	0205h		6	Interrupt request source select bit 0: UART6 transmission, NACK 1: Real-time clock alarm	Interrupt request source select bit 0: UART6 transmission, NACK 1: Real-time clock compare
			7	Key input interrupt polarity select bit 0: One edge 1: Both edges	Reserved bit
PCR	0366h		3	Key input enable bit ($\overline{KI4}$ to $\overline{KI7}$) 0: Enabled 1: Disabled	Reserved bit
			7	Key input enable bit ($\overline{KI0}$ to $\overline{KI3}$) 0: Enabled 1: Disabled	Key input enable bit 0: Enabled 1: Disabled

4.6 Differences in Timers

Table 4.10 lists Differences in Timers, and Table 4.11 lists Differences in Registers Associated with Timer.

Table 4.10   Differences in Timers

Item	M16C/63	M16C/65
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP11 bit in the PCLKSTP1 register.	No

Table 4.11   Differences in Registers Associated with Timer

| Symbol | Address | | Bits | Differences | |
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	1	Timer peripheral clock stop bit (timer A, timer B) 0: f1 provide enabled 1: f1 provide disabled	—

4.7 Differences in Real-Time Clocks

Table 4.12 lists Differences in Real-Time Clocks, and Table 4.13 to Table 4.15 list Differences in Registers Associated with Real-Time Clock
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Table 4.12   Differences in Real-Time Clocks

Item		M16C/63	M16C/65
Count source		fC	f1, fC
Peripheral clock stop selection		f1 provide enabled/disabled selectable using the PCKSTP10 bit in the PCLKSTP1 register	No

Count operation		Increment	• Increment
			• When using compare mode 1 or not using compare mode:
			   The count value is continuously used, and the count continues
			• When using compare mode 2:
			   When a compare match is detected, the count value is set to 0 and the count continues.
			• When using compare mode 3
			   When a compare match is detected, the count value is set to 0 and the count stops.

Count start condition		1 (count starts) is written to the RUN bit in TRHCR register	1 (count starts) is written to the TSTART bit in RTCCR1 register
Count stop condition		0 (count stops) is written to the RUN bit in TRHCR register	0 (count stops) is written to the TSTART bit in RTCCR1 register
Interrupt request generation timing		Periodic interrupt Select one of the following: • 250 ms cycles • 500 ms cycles • Update second data • Update minute data • Update hour data • Update date and day-of-the-week data • Update month data • Update year data	Periodic interrupt Select one of the following: • Update second data • Update minute data • Update hour data • Update day data • When day data is set to 000b
		Alarm interrupt • When time data and alarm data (either minute, hour, or day of the week, or combination of them) match	Compare interrupt • When time data and compare data (either second, minute, or hour, or combination of them) match
Output pin		TRHO pin	RTCOUT pin
Pin function		TRHO pin function Programmable I/O port or clock output	RTCOUT pin function Programmable I/O port or compare output
Second adjustment function		Yes	No
Clock error correction function	Automatic correction function	Yes	No
	Correction by software	Yes	No
Timer data protect		Selectable using the PROTECT bit in the TRHPRC register	No
Leap year flag		Yes (LFLAG bit in the TRHCR register)	No
A.m/p.m. bit in the 24-hour mode		PM bit in the TRHCR register is 0.	RTCPM bit in the RTCCR1 register. 12 a.m. to 11 a.m.: 0 12 p.m. to 11 p.m.: 1

Table 4.13   Differences in Registers Associated with Real-Time Clock Control

M16C/63			M16C/65		
Symbol	Address	Register Name	Symbol	Address	Register Name
PCLKSTP1	0016h	Peripheral Clock Stop Register	—	—	—
TRHCR	0347h	Timer RH Control Register	RTCCR1	0344h	Real-Time Clock Control Register 1
TRHCSR	0348h	Timer RH Count Source Select Register	RTCCSR	0346h	Real-Time Clock Count Source Select Register
TRHADJ	0349h	Clock Error Correction Register	—	—	—
TRHIFR	034Ah	Timer RH Interrupt Flag Register	—	—	—
TRHIER	034Bh	Timer RH Interrupt Enable Register	RTCCR2	0345h	Real-Time Clock Control Register 2
TRHPRC	034Fh	Timer RH Protect Register	—	—	—

Table 4.14   Differences in Registers Associated with Real-Time Clock Date Data

M16C/63			M16C/65		
Symbol	Address	Register Name	Symbol	Address	Register Name
TRHSEC	0340h	Second Data Register	RTCSEC	0340h	Real-Time Clock Second Data Register
TRHMIN	0341h	Minute Data Register	RTCMIN	0341h	Real-Time Clock Minute Data Register
TRHHR	0342h	Hour Data Register	RTCHR	0342h	Real-Time Clock Hour Data Register
TRHWK	0343h	Day-of-the-Week Data Register	RTCWK	0343h	Real-Time Clock Day Data Register
TRHDY	0344h	Date Data Register	—	—	—
TRHMON	0345h	Month Data Register	—	—	—
TRHYR	0346h	Year Data Register	—	—	—

Table 4.15   Differences in Registers Associated with Real-Time Clock Alarm

M16C/63			M16C/65		
Symbol	Address	Register Name	Symbol	Address	Register Name
—	—	—	RTCCSEC	0348h	Real-Time Clock Second Compare Data Register
TRHAMN	034Ch	Alarm Minute Register	RTCCMIN	0349h	Real-Time Clock Minute Compare Data Register
TRHAHR	034Dh	Alarm Hour Register	RTCCHR	034Ah	Real-Time Clock Hour Compare Data Register
TRHAWK	034Eh	Alarm Day-of-the-Week Register	—	—	—

4.8 Differences in Pulse Width Modulators

Table 4.16 lists Differences in PWMs, and Table 4.17 lists Differences in Registers Associated with PWM.

Table 4.16 Differences in PWMs

Item	M16C/63	M16C/65
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP16 bit in the PCLKSTP1 register.	No

Table 4.17 Differences in Registers Associated with PWM

Symbol	Address		Bits	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	6	PWM, multi-master I^{2}C peripheral clock stop bit (PWM, multi-master I^{2}C-bus interface) 0: f1 provide enabled 1: f1 provide disabled	—

4.9 Differences in Remote Control Signal Receivers

Table 4.18 lists Differences in Remote Control Signal Receivers, and Table 4.19 lists Differences in Registers Associated with Remote Control Signal Receiver.

Table 4.18 Differences in Remote Control Signal Receivers

Item	M16C/63	M16C/65
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP13 bit in the PCLKSTP1 register.	No

Table 4.19 Differences in Registers Associated with Remote Control Signal Receiver

Symbol	Address		Bits	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	3	Remote control peripheral clock stop bit (remote control signal receiver) 0: f1 provide enabled 1: f1 provide disabled	—

4.10 Differences in Serial Interfaces

Table 4.20 lists Differences in Serial Interfaces, and Table 4.21 lists Differences in Registers Associated with Serial Interface.

Table 4.20   Differences in Serial Interfaces

Item	M16C/63	M16C/65
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP12 bit and PCKSTP15 bit in the PCLKSTP1 register.	No

Table 4.21   Differences in Registers Associated with Serial Interface

| Symbol | Address | | Bits | Differences | |
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	2	UART peripheral clock stop bit (UART0 to 2, UART5 to 7) 0: f1 provide enabled 1: f1 provide disabled	—
			5	SIO peripheral clock stop bit (SI/O3, SI/O4) 0: f1 provide enabled 1: f1 provide disabled	—

4.11 Differences in Multi-Master I^{2}C-bus Interfaces

Table 4.22 lists Differences in Multi-Master I^{2}C-bus Interfaces, and Table 4.23 lists Differences in Registers Associated with Multi-Master I^{2}C-bus Interface.

Table 4.22   Differences in Multi-Master I^{2}C-bus Interfaces

Item	M16C/63	M16C/65
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP16 bit in the PCLKSTP1 register.	No

Table 4.23   Differences in Registers Associated with Multi-Master I^{2}C-bus Interface

| Symbol | Address | | Bits | Differences | |
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	6	PWM, multi-master I^{2}C peripheral clock stop bit (PWM, multi-master I^{2}C-bus interface) 0: f1 provide enabled 1: f1 provide disabled	—

4.12 Differences in A/D Converters

Table 4.24 lists Differences in A/D Converters, and Table 4.25 lists Differences in Registers Associated with A/D Converter.

Table 4.24   Differences in A/D Converters

Item	M16C/63	M16C/65
Operating clock φAD	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, or fOCO40M divided by 12	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, **f1 divided by 12**, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, or fOCO40M divided by 12
Peripheral clock stop selection	f1 provide enabled/disabled selectable using the PCKSTP14 bit in the PCLKSTP1 register.	No
Voltage multiplying function	Yes	No

Table 4.25   Differences in Registers Associated with A/D Converter

Symbol	Address		Bits	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
PCLKSTP1	0016h	—	4	AD peripheral clock stop bit 0: f1 provide enabled 1: f1 provide disabled	—
ADCON1	03D7h		3	Voltage multiply select bit 0: Voltage multiplier OFF 1: Voltage multiplier ON	No register bit

4.13   Differences in Flash Memories

Table 4.26 lists Differences in Flash Memories, Table 4.27 lists Differences in Registers Associated with Flash Memory, and Table 4.28 lists Differences in Software Commands

Table 4.26   Differences in Flash Memories

Item	M16C/63	M16C/65
Suspend function	Yes	No

Table 4.27   Differences in Registers Associated with Flash Memory

Symbol	Address		Bits	Differences	
	M16C/63	M16C/65		M16C/63	M16C/65
FMR3	0223h	—	—	M16C/63 only	—

Table 4.28   Differences in Software Commands

Software Command	MCU	First Bus Cycle		Second Bus Cycle	
		Address	Data	Address	Data
Read array	M16C/63, M16C/65 [1]	X	XXFFh	—	—
	M16C/65 [2]	B0-7	XXFFh	B8	XXFFh
Read status register	M16C/63, M16C/65 [1]	X	XX70h	X	SRD
	M16C/65 [2]	BA	XX70h	X	SRD
Clear status register	M16C/63, M16C/65 [1]	X	XX50h	—	—
	M16C/65 [2]	B0-7	XX50h	B8	XX50h
Block erase	M16C/63, M16C/65 [1]	X	XX20h	BA	XXD0h
	M16C/65 [2]	BA	XX20h	BA	XXD0h
Read lock bit status	M16C/63, M16C/65 [1]	X	XX71h	BA	XXD0h
	M16C/65 [2]	BA	XX71h	BA	XXD0h
Block blank check	M16C/63, M16C/65 [1]	X	XX25h	BA	XXD0h
	M16C/65 [2]	BA	XX25h	BA	XXD0h

Notes:
1.   Program ROM 1 is 512 KB or less.
2.   Program ROM 1 is more than 512 KB.

SRD: Data in the status register (D7 to D0)
BA: Highest-order block address (even address)
B0-7: Any even address in blocks 0 to 7, program ROM 2, or data flash
B8: Any even address in blocks after 8
X: Any even address in program ROM 1, program ROM 2, or data flash
XX: Eight high-order bits of command code (ignored)

5. Reference Documents

Hardware Manual
M16C/63 Group Hardware Manual
M16C/65 Group Hardware Manual
(The latest version of these documents can be downloaded from the Renesas Technology website.)

Technical News/Technical Update
(The latest version of these documents can be downloaded from the Renesas Technology website.)

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