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M16C/62P, M16C/62N Group

Differences between M16C/62P and M16C/62N

1. Abstract

This issue is the reference matelials ot function differences between M16C/62P and M16C/62N.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P, M16C/62N

3. Contents

3.1 Function differences

Table 3.1.1 and table 3.1.2 show the function differences (mask ROM version and flash memory version). Table 3.1.3 shows the function differences (flash memory version).

Table 3.1.1 Function differences (mask ROM version and flash memory version)-1(Note1)

Item	M16C/62P	M16C/62N
Shortest instruction execution time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	62.5ns(f(XIN)=16MHz, VCC=3.0 to 3.6V) 142.9ns(f(XIN)=7MHz, VCC=2.4 to 3.6V)
Supply voltage	VCC1=3.0 to 5.5V, VCC2=3.0V to VCC1 (f(BCLK)=24MHz) VCC1=VCC2=2.7 to 5.5V (f(BCLK)=10MHz)	3.0 to 3.6V(f(XIN)=16MHz) 2.4 to 3.6V(f(XIN)=7MHz) 2.2 to 3.6V(f(XIN)=7MHz, with software one-wait): Mask ROM version
I/O power supply	Double (VCC1, VCC2)	Single (VCC)
Package	80-pin, 100-pin, 128-pinplastic mold QFP	80-pin, 100-pinplastic mold QFP
Clock generating circuit	PLL, XIN, XCIN, on-chip oscillator	XIN, XCIN
System clock protective function	Built-in	None (protected by protect register)
Oscillation stop, re-oscillation detecton function	Built-in	None
Low power consumption	18mA(VCC1=VCC2=5V, f(BCLK)=24MHz) 8mA(VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8uA(VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)	20.0mA(VCC=3V, f(XIN)=16MHz) 3.0uA(VCC=3.3V, f(XCIN)=32kHz, wait mode)
External device connect area	04000h to 07FFFh (PM13=0) 08000h to 0FFFFh(PM10=0) 10000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (PM13=0) D0000h to FFFFFh (Microprocessor mode)	04000h to 07FFFh (PM13=0) 08000h to CFFFFh D0000h to FFFFFh (Microprocessor mode)
Upper address memory expansion mode and microprocessor mode	P4_0 to P4_3(A16 to A19), P3_4 to P3_7(A12 to A15) : Switchable between address bus and I/O port	P4_0 to P4_3(A16 to A19) : Switchable between address bus and I/O port A12 to A15: No Switchable
Access to SFR	Variable (1 to 2 waits)	1 wait fixed
Software wait to external area	Variable (0 to 3 waits)	Variable (0 to 1 wait)
Protect	Can be set for PM0, PM1, PM2, CM0, CM1, CM2, PLC0, INVC0, INVC1, PD9, S3C, S4C, TB2SC, PCLKR, VCR2, D4INT registers	Can be set for PM0, PM1, CM0, CM1, PD9, S3C, S4C registers

Note 1: About the details and the characteristics, refer to hardware manual.

Table 3.1.2 Function differences (mask ROM version and flash memory version)-2(Note1)

Item	M16C/62P	M16C/62N
Watchdog timer	Count source protective mode is available	No count source protective mode
Address match interrupt	4	2
Timers A, timer B Count source	Selectable: f1, f2, f8, f32, fC32	Selectable: f1, f8, f32, fC32
Timer A two-phase pulse signal processing	Function Z-phase (counter reset) input	No function Z-phase (counter reset) input
Timer functions for three-phase motor control	Function protect by protect register Count source is selected f1, f2, f8, f32, fC32 Dead time timer count source is selected: f1, f1 divided by 2, f2, f2 divided by 2 Three-phase output forcible shutoff function based on $\overline{\text{NMI}}$ input is available, output polarity change, carrier wave phase detection	No function protected by protect register Count source is selected :f1, f8, f32, fC32 Dead time timer count source is fixed at f1 divided by 2
Serial I/O (UART0 to UART2)	(UART, Clock synchronous, I^2C-bus^{TM} (Note 2), IEBus^{TM} (Note 3)) x 3	(UART, Clock synchronous) x 2 (UART, Clock synchronous, I^2C-bus^{TM} (Note 2), IEBus^{TM} (Note 3)) x 1
UART0 to UART2, SI/O3, SI/O4 Count source	Select from f1SIO, f2SIO, f8SIO, f32SIO	Select from f1, f8, f32
Serial I/O $\overline{\text{RTS}}$ timing	Assert low when receive buffer is read	Assert low when reception is completed
UART0 to UART2 Overrun error occur timing	This error occurs if the serial I/O started receiving the next data before reading the UiRB register (i=0 to 2) and received the 7th bit of the next data (Clock synchronous). This error occurs if the serial I/O started receiving the next data before reading the UiRB register and received the bit one before the last stop bit of the next data (UART).	This error occurs when the next data is ready before contents of UiRB register (i=0 to 2) are read out
Serial I/O $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ separate function	Have	None
UART2 data transmit timing	After data was written, transfer starts at the 2nd BRG overflow timing (same as UART0 and UART1)	After data was written, transfer starts at the 1st BRG overflow timing (Output starts one cycle of BRG overflow earlier than UART0 and UART1)
Serial I/O Sleep function	None	Have
Serial I/O I^2C mode	Start condition, stop condition: Auto-generation	Start condition, stop condition: Not auto-generation
Serial I/O I^2C mode SDA delay	SDA digital delay count source: BRG	SDA digital delay count source: 1/f(XIN)
SI/O3, SI/O4 Clock polarity	Selectable	Fixed
A/D converter	10 bits x 8 channels Expandable up to 26 channels	10 bits x 8 channels Expandable up to 18 channels
A/D converter operation clock	Selectable: fAD, fAD divided by 2, 3, 4, 6, 12	Selectable: fAD, fAD/2, fAD/4
A/D converter input pin	Select from ports P0, P2, P10	Select from ports P0, P10

Note 1: About the details and the characteristics, refer to hardware manual.

Note 2: I^2C is a trademark of Philips Semiconductors Corporation.

Note 3: IEBus is a trademark of NEC Electronics Corporation.

Table 3.1.2 Function differences (flash memory version)(Note1)

Item	M16C/62P	M16C/62N
User ROM blocks	14 blocks: 4 Kbytes X 3, 8 Kbytes X 3, 32 Kbytes X 1, 64 Kbytes X 7 (Flash memory: max. 512 Kbytes)	7 blocks: 4 Kbytes X 2, 24 Kbytes X 1, 32 Kbytes X 1, 64 Kbytes X 3 (Flash memory: max. 256 Kbytes)
CPU rewrite mode	EW1 mode is available	No EW1 mode

Note 1: About the details and the characteristics, refer to hardware manual.

3.2 Pin function differences

Table 3.2.1 shows the pin function differences.

Table 3.2.1 Pin function differences

M16C/62P	M16C/62N	Remarks
VCC1	VCC	
P8_4/INT2/ZP	P8_4/INT2	Add ZP
P6_7/TxD1/SDA1	P6_7/TxD1	Add SDA1
P6_6/RxD1/SCL1	P6_6/RxD1	Add SCL1
P6_4/CTS1/RTS1/CTS0/CLKS1	P6_4/CTS1/RTS1/CLKS1	Add CTS0
P6_3/TxD0/SDA0	P6_3/TxD0	Add SDA0
P6_2/RxD0/SCL0	P6_2/RxD0	Add SCL0
VCC2	VCC	
P2_7/AN2_7/A7(/D7/D6)	P2_7/A7(/D7/D6)	Add AN2_7
P2_6/AN2_6/A6(/D6/D5)	P2_6/A6(/D6/D5)	Add AN2_6
P2_5/AN2_5/A5(/D5/D4)	P2_5/A5(/D5/D4)	Add AN2_5
P2_4/AN2_4/A4(/D4/D3)	P2_4/A4(/D4/D3)	Add AN2_4
P2_3/AN2_3/A3(/D3/D2)	P2_3/A3(/D3/D2)	Add AN2_3
P2_2/AN2_2/A2 (/D2/D1)	P2_2/A2 (/D2/D1)	Add AN2_2
P2_1/AN2_1/A1(/D1/D0)	P2_1/A1(/D1/D0)	Add AN2_1
P2_0/AN2_0/A0(/D0/-)	P2_0/A0(/D0/-)	Add AN2_0

3.3 SFR differences

Table 3.3.1 show the SFR differences.

Table 3.3.1 SFR differences-1

M16C/62P	M16C/62N	Remarks
PM1	PM1	Change function
CM0	CM0	Change function
CM1	CM1	Add bit1
PRCR	PRCR	Change function
CM2	-	
WDC	WDC	Add bit5
VCR1	-	
VCR2	-	
CSE	-	
PLC0	-	
PM2	-	
D4INT	-	
TB4IC,U1BCNIC	TB4IC	Shard with U1BCNIC register
TB3IC,U0BCNIC	TB3IC	Shard with U0BCNIC register
RMAD2	-	
AIER2	-	
RMAD3	-	
PCLKR	-	
INVC1	INVC1	Change function
IFSR2A	-	
S3C	S3C	Add bit4
S4C	S4C	Add bit4
U0SMR4	-	
U0SMR3	-	
U0SMR2	-	
U0SMR	-	
U1SMR4	-	
U1SMR3	-	
U1SMR2	-	
U1SMR	-	
U2SMR4	-	
U2SMR3	U2SMR3	Change function
U2SMR2	U2SMR2	Change function
U2SMR	U2SMR	Change function
ONSF	ONSF	Add bit5
TB2SC	-	
U0MR	U0MR	Change function
U0C0	U0C0	Change function
U0C1	U0C1	Add Bits6, 7
U1MR	U1MR	Change function
U1C0	U1C0	Change function

Table 3.3.2 SFR differences-2

M16C/62P	M16C/62N	Remarks
U1C1	U1C1	Add bits6, 7
UCON	UCON	Add bit6
FIDR	FIDR	Address change from 03B4h to 01B4h. Change function.
FMR1	-	
FMR0	FMR0	Address change from 03B7h to 01B7h. Change function.
ADCON2	ADCON2	Change function

3.4 Interrupt vector differences

Table 3.4.1 shows the fixed vector table differences. Table 3.4.2 shows the relocatable vector table differences.

Table 3.4.1 Fixed vector table differences

M16C/62P interrupt source	M16C/62N interrupt source
Watchdog timer Oscillation stop and re-oscillation detection Voltage down detection	Watchdog timer

Table 3.4.2 Relocatable vector table differences

M16C/62P interrupt source	M16C/62N interrupt source	Software interrupt number
Timer B4, UART1 bus collision detect	Timer B4	6
Timer B3, UART0 bus collision detect	Timer B3	7
UART0 transmit, NACK0	UART0 transmit	17
UART0 receive, ACK0	UART0 receive	18
UART1 transmit, NACK1	UART1 transmit	19
UART1 receive, ACK1	UART1 receive	20

3.5 Support tool differences

Table 3.5.1 shows the support tool differences.

Table 3.5.1 support tool differences

Tool information	M16C/62P tool product (Max.24MHz)	M16C/62P tool product (Max.16MHz)	M16C/62N tool product	Change
C Compiler	M3T-NC30WA	M3T-NC30WA	M3T-NC30WA	
Real-time OS	M3T-MR30	M3T-MR30	M3T-MR30	
Simulator Debugger	M3T-PD30SIM	M3T-PD30SIM	M3T-PD30SIM	
Emulator Debugger	M3T-PD30F	M3T-PD30	M3T-PD30	√
Emulator	PC7501	PC4701U	PC4701U	√
Emulation Pod, Emulation Probe	M3062PT-EPB	M3062PT3-RPD-E	M3062NT3-RPD-E	√

4. Reference

DATA SHEET
M16C/62N Group data sheet Rev.1.1
(Acquire the most current version from Renesas web-site)

HARDWARE MANUAL
M16C/62P Group Hardware manual Rev.2.30
(Acquire the most current version from Renesas web-site)

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REVISION HISTORY

Rev.	Date	Description	
		Page	
1.10	Aug 05, 2003	2 4	4V detect interrupt ->Voltage down detect interrupt Block status after program function delete M16C/62P None, M16C/62N None
2.00	Feb 02, 2004	2 4-8	Add UART0 to UART2 Overrun error occur timing Add pin function differences, SFR differences, Interrupt vector differences, support tool differences
2.01	Aug 02,2004	-	Words standardized: On-chip oscillator, and A/D converter

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