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April 1st, 2010
Renesas Electronics Corporation

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M16C/62P, M16C/26 Group

Differences between M16C/62P and M16C/26

1. Abstract

This issue is the reference matelials ot function differences between M16C/62P and M16C/26(M30262FXGP).

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P, M16C/26

3. Contents

3.1 Function differences

Table 3.1.1 to table 3.1.3 show the function differences

Table 3.1.1 Function differences (1)(Note1)

Item	M16C/62P	M16C/26
Shortest instruction execution time	41.7ns(f(BCLK)=24MHz, VCC1=3.0 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	50.0ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
Supply voltage	VCC1=3.0 to 5.5V, VCC2=3.0V to VCC1 (f(BCLK)=24MHz) VCC1=VCC2=2.7 to 5.5V (f(BCLK)=10MHz)	VCC=3.0 to 5.5V(f(XIN)=20MHz, without software wait) VCC=2.7 to 5.5V(f(XIN)=10MHz, without software wait)
I/O power supply	Double (VCC1, VCC2)	Single (VCC)
Package	80-pin, 100-pin, 128-pin plastic mold QFP	48-pin plastic mold QFP
Memory	Mask ROM Flash memory External ROM	Flash memory
Clock generating circuit	PLL, XIN, XCIN, on-chip oscillator	XIN, XCIN, on-chip oscillator
Processor mode	Single-chip mode, memory expansion mode, microprocessor mode	Single-chip mode
Low power consumption	18mA(VCC1=VCC2=5V, f(BCLK)=24MHz) 8mA(VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8uA(VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode)	16mA(VCC=5V, f(XIN)=20MHz) 8mA(VCC=3V, f(XIN)=10MHz) 1.8uA(VCC=3V, f(XCIN)=32kHz, wait mode)

Note 1: About the details and the characteristics, refer to hardware manual.

Table 3.1.2 Function differences (2)(Note1)

Item	M16C/62P	M16C/26
Access to SFR	Variable (1 to 2 waits)	1 wait fixed
$\overline{\text{NMI}}$ pin	Input only. Can not use I/O port.	Shared with I/O port. $\overline{\text{NMI}}$ function is enabled when the PM24 bit is “1” (enabled).
Protect	Can be set for PM0, PM1, PM2, CM0, CM1, CM2, PLC0, INVC0, INVC1, PD9, S3C, S4C, TB2SC, PCLKR, VCR2, D4INT registers	Can be set for PM0, PM1, PM2, CM0, CM1, CM2, INVC0, INVC1, PD9, TB2SC, PCLKR, VCR2, D4INT registers
I/O port	87(100-pin version)	38
Address match interrupt	4	2
Timer	Timer A X 5, Timer B X 6: total 11	Timer A X 5, Timer B X 3: total 8
Timer A two-phase pulse signal processing	Function Z-phase (counter reset) input	No function Z-phase (counter reset) input
Timer functions for three-phase motor control	If “L” is input to $\overline{\text{NMI}}$ pin, three-phase output pins do not change when INPCR1 bit is “0” (three-phase output forcible cutoff by $\overline{\text{NMI}}$ pin input disabled).	If “L” is input to $\overline{\text{SD}}$ pin, three-phase output pins change to programmable I/O port when INPCR1 bit is “0” (three-phase output forcible cutoff by $\overline{\text{SD}}$ pin input disabled).
Serial I/O (UART0 to UART2)	(UART, Clock synchronous, I^2C-bus™ (Note 2), IEBus™ (Note 3)) X 3	(UART, Clock synchronous) X 2 (UART, Clock synchronous, I^2C-bus™ (Note 2), IEBus™ (Note 3)) X 1
Clock synchronous serial I/O (SI/O3, SI/O4)	2 channel	None
A/D converter	10 bits x 8 channels Expandable up to 26 channels	10 bits x 8 channels
D/A converter	8 bits x 2	None
CRC	1	None

Note 1: About the details and the characteristics, refer to hardware manual.

Note 2: I^2C is a trademark of Philips Semiconductors Corporation.

Note 3: IEBus is a trademark of NEC Electronics Corporation.

Table 3.1.3 Function differences (3)(flash memory)(Note1)

Item	M16C/62P	M16C/26
User ROM blocks (Program area)	14 blocks: 4 Kbytes X 3, 8 Kbytes X 3, 32 Kbytes X 1, 64 Kbytes X 7 (Flash memory: max. 512 Kbytes)	4 blocks: 8 Kbytes X 2, 16 Kbytes X 1, 32 Kbytes X 1 (Flash memory: max. 64 Kbytes)
User ROM blocks (Data area)	4 Kbytes X 1 (block A)	2 Kbytes X 2 (block A, block B)
Erase-suspend	Un-corresponding	Correspondence
Boot ROM area	Can be rewritten	Can not be rewritten
Program manner	Protected for each block by lock bit	Protected for block 0 and block 1 by FMR02 bit
Program command (Software command)	8 command Read array command Read status register command Clear status register command Program command Block erase command Erase all unblocked block command Lock bit program command Read lock bit status command	5 command Read array command Read status register command Clear status register command Program command Block erase command

Note 1: About the details and the characteristics, refer to hardware manual.

3.2 Pin function differences

Table 3.2.1 and table 3.2.2 show the pin function differences.

Table 3.2.1 Pin function differences (1)

M16C/62P	M16C/26	Remarks
P9_6/ANEX1/SOUT4	-	
P9_5/ANEX0/CLK4	-	
P9_4/DA1/TB4IN	-	
P9_3/DA0/TB3IN	P9_3	
P9_2/TB2IN/SOUT3	P9_2/TB2IN	
P9_1/TB1IN/SIN3	P9_1/TB1IN	
P9_0/TB0IN/CLK3	P9_0/TB0IN	
BYTE	-	
CNVSS	CNVSS	Same
P8_7/XCIN	P8_7/XCIN	Same
P8_6/XCOUT	P8_6/XCOUT	Same
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Same
XOUT	XOUT	Same
VSS	VSS	Same
XIN	XIN	Same
VCC1	VCC	
P8_5/$\overline{\text{NMI}}$	P8_5/$\overline{\text{NMI}}$/$\overline{\text{SD}}$	
P8_4/$\overline{\text{INT2}}$/ZP	IVCC	
P8_3/$\overline{\text{INT1}}$	P8_3/$\overline{\text{INT1}}$	Same
P8_2/$\overline{\text{INT0}}$	P8_2/$\overline{\text{INT0}}$	Same
P8_1/TA4IN/$\overline{\text{U}}$	P8_1/TA4IN/$\overline{\text{U}}$	Same
P8_0/TA4OUT/U	P8_0/TA4OUT/U	Same
P7_7/TA3IN	P7_7/TA3IN	Same
P7_6/TA3OUT	P7_6/TA3OUT	Same
P7_5/TA2IN/$\overline{\text{W}}$	P7_5/TA2IN/$\overline{\text{W}}$	Same
P7_4/TA2OUT/W	P7_4/TA2OUT/W	Same
P7_3/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TA1IN/$\overline{\text{V}}$	P7_3/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TA1IN/$\overline{\text{V}}$	Same
P7_2/CLK2/TA1OUT/V	P7_2/CLK2/TA1OUT/V	Same
P7_1/RXD2/SCL2/TA0IN/TB5IN	P7_1/RXD2/SCL/TA0IN	
P7_0/TXD2/SDA2/TA0OUT	P7_0/TXD2/TA0OUT/SDA	Same
P6_7/TXD1/SDA1	P6_7/TXD1	
P6_6/RXD1/SCL1	P6_6/RXD1	
P6_5/CLK1	P6_5/CLK1	Same
P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	Same
P6_3/TXD0/SDA0	P6_3/TXD0	
P6_2/RXD0/SCL0	P6_2/RXD0	
P6_1/CLK0	P6_1/CLK0	Same
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	Same
P5_7/$\overline{\text{RDY}}$/CLKOUT	-	
P5_6/ALE	-	
P5_5/$\overline{\text{HOLD}}$	-	
P5_4/$\overline{\text{HLDA}}$	-	
P5_3/BCLK	-	
P5_2/$\overline{\text{RD}}$	-	
P5_1/$\overline{\text{WRH}}$/$\overline{\text{BHE}}$	-	
P5_0/$\overline{\text{WRL}}$/$\overline{\text{WR}}$	-	
P4_7/$\overline{\text{CS3}}$	-	
P4_6/$\overline{\text{CS2}}$	-	
P4_5/$\overline{\text{CS1}}$	-	
P4_4/$\overline{\text{CS0}}$	-	
P4_3/A19	-	
P4_2/A18	-	
P4_1/A17	-	

Table 3.2.2 Pin function differences (2)

M16C/62P	M16C/26	Remarks
P4_0/A16	-	
P3_7/A15	-	
P3_6/A14	-	
P3_5/A13	-	
P3_4/A12	-	
P3_3/A11	-	
P3_2/A10	-	
P3_1/A9	-	
VCC2	VCC	
P3_0/A8(/-/D7)	-	
P2_7/AN2_7/A7(/D7/D6)	-	
P2_6/AN2_6/A6(/D6/D5)	-	
P2_5/AN2_5/A5(/D5/D4)	-	
P2_4/AN2_4/A4(/D4/D3)	-	
P2_3/AN2_3/A3(/D3/D2)	-	
P2_2/AN2_2/A2 (/D2/D1)	-	
P2_1/AN2_1/A1(/D1/D0)	-	
P2_0/AN2_0/A0(/D0/-)	-	
P1_7/D15/$\overline{\text{INT5}}$	P1_7/$\overline{\text{INT5}}$	
P1_6/D14/$\overline{\text{INT4}}$	P1_6/$\overline{\text{INT4}}$	
P1_5/D13/$\overline{\text{INT3}}$	P1_5/$\overline{\text{INT3}}$/$\overline{\text{ADTRG}}$	
P1_4/D12	-	
P1_3/D11	-	
P1_2/D10	-	
P1_1/D9	-	
P1_0/D8	-	
P0_7/AN0_7/D7	-	
P0_6/AN0_6/D6	-	
P0_5/AN0_5/D5	-	
P0_4/AN0_4/D4	-	
P0_3/AN0_3/D3	-	
P0_2/AN0_2/D2	-	
P0_1/AN0_1/D1	-	
P0_0/AN0_0/D0	-	
P10_7/AN7/$\overline{\text{KI3}}$	P10_7/AN7/$\overline{\text{KI3}}$	Same
P10_6/AN6/$\overline{\text{KI2}}$	P10_6/AN6/$\overline{\text{KI2}}$	Same
P10_5/AN5/$\overline{\text{KI1}}$	P10_5/AN5/$\overline{\text{KI1}}$	Same
P10_4/AN4/$\overline{\text{KI0}}$	P10_4/AN4/$\overline{\text{KI0}}$	Same
P10_3/AN3	P10_3/AN3	Same
P10_2/AN2	P10_2/AN2	Same
P10_1/AN1	P10_1/AN1	Same
AVSS	AVSS	Same
P10_0/AN0	P10_0/AN0	Same
VREF	VREF	Same
AVCC	AVCC	Same
P9_7/$\overline{\text{ADTRG}}$/SIN4	-	

3.3 SFR differences

Table 3.3.1 to table 3.3.3 show the SFR differences

Table 3.3.1 SFR differences (1)

M16C/62P	M16C/26	Remarks
PM0	PM0	Change function
PM1	PM1	Change function
CM0	CM0	Change function
CM1	CM1	Change function
CSR	-	
AIER	AIER	Same
PRCR	PRCR	Change function
DBR	-	
CM2	CM2	Change function
WDTS	WDTS	Same
WDT	WDT	Same
RMAD0, RMAD1	RMAD0, RMAD1	Same
VCR1	VCR1	Same
VCR2	VCR2	Change function
CSE	-	
PLC0	-	
PM2	PM2	Change function
D4INT	D4INT	Same
SAR0, SAR1	SAR0, SAR1	Same
DAR0, DAR1	DAR0, DAR1	Same
TCR0, TCR1	TCR0, TCR1	Same
DM0CON, DM1CON	DM0CON, DM1CON	Same
INT3IC	INT3IC	Same
TB5IC	-	
TB4IC,U1BCNIC	-	
TB3IC,U0BCNIC	-	
S4IC,INT5IC	INT5IC	Change function
S3IC,INT4IC	INT4IC	Change function
BCNIC	BCNIN	Same
DM0IC, DM1IC	DM0IC, DM1IC	Same
KUPIC	KUPIC	Same
ADIC	ADIC	Same
S0TIC to S2TIC	S0TIC to S2TIC	Same
S0RIC to S2RIC	S0RIC to S2RIC	Same
TA0IC to TA4IC	TA0IC to TA4IC	Same
TB0CI to TB2IC	TB0CI to TB2IC	Same
INT0IC, INT1IC	INT0IC, INT1IC	Same
INT2IC	-	
-	FMR4	Change function
FIDR	-	
FMR1	FMR1	Change function
FMR0	FMR0	Change function
RMAD2	-	
AIER2	-	

Table 3.3.2 SFR differences (2)

M16C/62P	M16C/26	Remarks
RMAD3	-	
PCLKR	PCLKR	Same
TBSR	-	
TA11, TA21, TA41	TA11, TA21, TA41	Same
INVC0	INVC0	Change function
INVC1	INVC1	Change function
IDB0, IDB1	IDB0, IDB1	Same
DTT	DTT	Same
ICTB2	ICTB2	Same
TB3, TB4, TB5	-	
TB3MR, TB4MR, TB5MR	-	
IFSR2A	-	
IFSR	IFSR	Change function
S3TRR	-	
S3C	-	
S3BRG	-	
S4TRR	-	
S4C	-	
S4BRG	-	
U0SMR4	-	
U0SMR3	-	
U0SMR2	-	
U0SMR	-	
U1SMR4	-	
U1SMR3	-	
U1SMR2	-	
U1SMR	-	
U2SMR4	U2SMR4	Same
U2SMR3	U2SMR3	Same
U2SMR2	U2SMR2	Same
U2SMR	U2SMR	Same
U2MR	U2MR	Same
U2BRG	U2BRG	Same
U2TB	U2TB	Same
U2C0	U2C0	Same
U2C1	U2C1	Same
U2RB	U2RB	Same
TABSR	TABSR	Same
CPSRF	CPSRF	Same
ONSF	ONSF	Change function
TRGSR	TRGSR	Same
UDF	UDF	Same
TA0, TA1, TA2, TA3, TA4	TA0, TA1, TA2, TA3, TA4	Same
TB0, TB1, TB2	TB0, TB1, TB2	Same
TA0MR to TA4MR	TA0MR to TA4MR	Same
TB0MR to TB2MR	TB0MR to TB2MR	Same
TB2SC	TB2SC	Change function

Table 3.3.3 SFR differences (3)

M16C/62P	M16C/26	Remarks
U0MR	U0MR	Change function
U0BRG	U0BRG	Same
U0TB	U0TB	Same
U0C0	U0C0	Change function
U0C1	U0C1	Change function
U0RB	U0RB	Same
U1MR	U1MR	Change function
U1BRG	U1BRG	Same
U1TB	U1TB	Same
U1C0	U1C0	Change function
U1C1	U1C1	Change function
U1RB	U1RB	Same
UCON	UCON	Same
DM0SL	DM0SL	Change function
DM1SL;	DM1SL;	Change function
CRCD	-	
CRCIN	-	
AD0 to AD7	AD0 to AD7	Same
ADCON2	ADCON2	Change function
ADCON0	ADCON0	Same
ADCON1	ADCON1	Change function
DA0, DA1	-	
DACON	-	
PC14	-	
PUR3	-	
P0	-	
P1	P1	Change function
PD0	-	
PD1	PD1	Change function
P2, P3, P4, P5	-	
PD2, PD3, PD4, PD5	-	
P6, P7	P6, P7	Same
PD6, PD7	PD6, PD7	Same
P8	P8	Change function
P9	P9	Change function
PD8	PD8	Change function
PD9	PD9	Change function
P10	P10	Same
PD10	PD10	Same
P11, P12, P13	-	
PD11, PD12, PD13	-	
PUR0	PUR0	Change function
PUR1	PUR1	Change function
PUR2	PUR2	Change function
PCR	PCR	Same

3.4 Interrupt vector differences

Table 3.4.1 shows the relocatable vector table differences.

Table 3.4.1 Relocatable vector table differences

M16C/62P interrupt source	M16C/26 interrupt source	Software interrupt number
Timer B5	-	5
Timer B4, UART1 bus collision detect	-	6
Timer B3, UART0 bus collision detect	-	7
SI/O4, $\overline{\text{INT5}}$	$\overline{\text{INT5}}$	8
SI/O3, $\overline{\text{INT4}}$	$\overline{\text{INT4}}$	9
UART0 transmit, NACK0	UART0 transmit	17
UART0 receive, ACK0	UART0 receive	18
UART1 transmit, NACK1	UART1 transmit	19
UART1 receive, ACK1	UART1 receive	20
$\overline{\text{INT2}}$	-	31

3.5 Support tool differences

Table 3.5.1 shows the support tool differences.

Table 3.5.1 support tool differences

Tool information	M16C/62P tool product		M16C/26 tool product	
Maximum operation frequency	24MHz	16MHz	20MHz	16MHz
C Compiler	M3T-NC30WA			
Real-time OS	M3T-MR30			
Simulator Debugger	M3T-PD30SIM			
Emulator Debugger	M3T-PD30F	M3T-PD30	M3T-PD30F	M3T-PD30
Emulator	PC7501	PC4701U	PC7501	PC4701U
Emulation Pod, Emulation Probe	M3062PT-EPB	M3062PT3-RPD-E	M3062PT-EPB+M30262T-PTC	M30620T2-RPD-E+M30262T-PTC

4. Reference

HARDWARE MANUAL

M16C/26 Hardware manual Rev.0.90
(Acquire the most current version from Renesas web-site)

M16C/62P Group Hardware manual Rev.2.30
(Acquire the most current version from Renesas web-site)

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REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Mar 03, 2004	-	First edition
1.01	Aug 02, 2004	-	Words standardized: On-chip oscillator, A/D converter, and D/A converter

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