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M16C/30P Group, M16C/64A Group

Differences between M16C/30P and M16C/64A

1. Abstract

This document describes differences between M16C/30P (Flash memory version) and M16C/64A. Refer to each device's hardware manual for details.

2. Introduction

The explanation of this application note is applied to the following MCUs:

Applicable MCUs: M16C/30P (Flash memory version), M16C/64A

3. Differences

3.1 Differences in Functions

Table 3.1 and Table 3.2 list Differences in Functions.

Table 3.1 Differences in Functions (1/2) (1)

Item		M16C/30P	M16C/64A
Minimum Instruction Execution Time		62.5 ns (f(XIN) = 16 MHz, VCC1 =VCC2 = 3.0 to 5.5 V, no wait) 100 ns (f(XIN) = 10 MHz, VCC1 = VCC2 = 2.7 to 5.5 V, no wait)	40 ns (f(BCLK) = 25 MHz, VCC1 = VCC2 = 2.7 to 5.5 V)
Clock Generator		2 circuits Main clock, sub clock	4 circuits Main clock, sub clock, 125 kHz on-chip oscillator, PLL frequency synthesizer
Power Consumption		10 mA (VCC1 = VCC2 = 5 V, f(XIN) = 16 MHz) 8 mA (VCC1 = VCC2 = 3 V, f(XIN) = 10 MHz) 1.8 uA (VCC1 = VCC2 = 3 V, f(XCIN) = 32 kHz, wait mode) 0.7 uA (VCC1 = VCC2 = 3V, stop mode)	TBD (25 MHz/VCC1 = VCC2 = 3 V) TBD (VCC1 = VCC2 = 3 V, stop mode)
CPU Clock After Reset		Main clock divided by 8	125 kHz on-chip oscillator clock divided by 8
System Clock Protection Function		No (protected by the Protect Register)	Yes
Oscillator Stop/Restart Detect Function		No	Yes
Voltage Detection	Voltage detector	No	3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
	Power-on reset	No	Yes
Power Control	Slow read mode	No	Yes
	Low current consumption read mode	No	Yes
External Bus	Expanded area	04000h to 07FFFh 08000h to 0FFFFh (when PM10 is 0) 10000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (when PM13 is 0 or a product type does not have PM13) D0000h to FFFFFh (in microprocessor mode)	04000h to 07FFFh (when PM13 is 0) 08000h to 0CFFFh 0D800h to 0DFFFh 0E000h to 0FFFFh (when PM10 is 0) 10000h to 13FFFh (when PRG2C0 is 1) 14000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (when PM13 is 0) D0000h to FFFFFh (in microprocessor mode)
	External bus mode	Separate bus	Separate bus, multiplexed bus
Memory Space Expansion Function		1-MB mode	1-MB mode, 4-MB mode
Interrupts		External interrupts: 10	External interrupts: 13
Address Match Interrupt		2 addresses	4 addresses
$\overline{\text{NMI}}$ Pin		Cannot be used as an input port	• I/O port (N-channel open drain output) when PM24 bit in the PM2 register is 0 ($\overline{\text{NMI}}$ interrupt disabled) • Input port when PM24 bit in the PM2 register is 1 ($\overline{\text{NMI}}$ interrupt enabled)

PM10, PM13: Bits in the PM1 register, PRG2C0: Bit in the PRG2C register

Note:
1. Refer to the hardware manual for electrical characteristics and more details.

Table 3.2 Differences in Function (2/2) (1)

Item		M16C/30P	M16C/64A
Watchdog Timer	Count source	CPU clock	CPU clock, 125 kHz on-chip oscillator
	Count source protection mode	No	Yes
	Reset start function	No	Selectable from start and stop
	Operation when timer underflows	Watchdog timer interrupt	Selectable from watchdog timer interrupt and watchdog timer reset
DMAC		2 channels Trigger sources: 18	4 channels Trigger sources: 43
Timer	Number of channels	Timer A x 3 Timer B x 3	Timer A x 5 Timer B x 6
	Timer A operating mode	Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode	Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, programmable output mode
	Three-phase motor control timer function	No	Yes
	Real-time clock	No	Count: second, minute, hour, day of the week
	PWM function	No	8 bits x 2
	Remote control signal receiver	No	2 circuits
Serial Interface	Number of channels	Clock synchronous/asynchronous x 3	Clock synchronous/asynchronous x 6 Clock-synchronous only x 2
	Multi-master I^2C-bus interface	No	1 channel
	CEC	No	Yes
A/D Converter	Operation mode	One-shot mode, repeat mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1
	A/D converter input pins	Selectable from port P0 and port P10	Selectable from port P0, port P2 and port P10
	Resolution	8-bit/10-bit (selectable)	10-bit only
	Open-circuit detection assist function	No	Yes
D/A converter		No	8 bits x 2 channels
CRC Calculator	Generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	Selectable form CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) and CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
	CRC snoop	No	Yes
Flash Memory	Memory map	User ROM (ROM size: 192 KB) Program ROM 0D0000h to 0FFFFFh Data flash Block A 00F000h to 00FFFFh	User ROM (ROM size: 512 KB) • Program ROM1 080000h to 0FFFFFh • Program ROM2 010000h to 013FFFh Data flash • Block A 00E000h to 00EFFFh • Block B 00F000h to 00FFFFh
	Data flash	4 KB x 1 (block A)	4 KB x 2 (block A, block B)
	Program method	1-word (2-byte) unit	2-word (4-byte) units
	User boot mode	No	Yes

Note:
1. Refer to the hardware manual for electrical characteristics and more details.

3.2 Pin Characteristics

Table 3.3 and Table 3.4 list Differences in Pin Characteristics.

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Table 3.3 Differences in Pin Characteristics (1/2)

M16C/30P	M16C/64A	Changes from M16C/30P
P9_6/ANEX1	P9_6/SOUT4/ANEX1	Added: SOUT4
P9_5/ANEX0	P9_5/CLK4/ANEX0	Added: CLK4
P9_4	P9_4/TB4IN/PWM1/DA1	Added: TB4IN/PWM1/DA1
P9_3	P9_3/TB3IN/PWM0/DA0	Added: TB3IN/PWM0/DA0
P9_2/TB2IN	P9_2/TB2IN/PMC0/SOUT3	Added: PMC0/SOUT3
P9_1/TB1IN	P9_1/TB1IN/PMC1/SIN3	Added: PMC1/SIN3
P9_0/TB0IN	P9_0/TB0IN/CLK3	Added: CLK3
P8_5/$\overline{\text{NMI}}$	P8_5/$\overline{\text{NMI}}$/$\overline{\text{SD}}$/CEC	Added: $\overline{\text{SD}}$/CEC
P8_4/$\overline{\text{INT2}}$	P8_4/$\overline{\text{INT2}}$/ZP	Added: ZP
P8_1	P8_1/TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	Added: TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$
P8_0	P8_0/TA4OUT/U/RXD5/SCL5	Added: TA4OUT/U/RXD5/SCL5
P7_7	P7_7/TA3IN/CLK5	Added: TA3IN/CLK5
P7_6	P7_6/TA3OUT/TXD5/SDA5	Added: TA3OUT/TXD5/SDA5
P7_5/TA2IN	P7_5/TA2IN/$\overline{\text{W}}$	Added: $\overline{\text{W}}$
P7_4/TA2OUT	P7_4/TA2OUT/W	Added: W
P7_3/TA1IN/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$	Added: $\overline{\text{V}}$
P7_2/TA1OUT/CLK2	P7_2/TA1OUT/V/CLK2	Added: V
P7_1/TA0IN/RXD2/SCL2	P7_1/TA0IN/TB5IN/RXD2/SCL2/SCLMM	Added: TB5IN/SCLMM
P7_0/TA0OUT/TXD2/SDA2	P7_0/TA0OUT/TXD2/SDA2/SDAMM	Added: SDAMM
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/RTCOUT	Added: RTCOUT
P4_7/$\overline{\text{CS3}}$	P4_7/PWM1/TXD7/SDA7/$\overline{\text{CS3}}$	Added: PWM1/TXD7/SDA7
P4_6/$\overline{\text{CS2}}$	P4_6/PWM0/RXD7/SCL7/$\overline{\text{CS2}}$	Added: PWM0/RXD7/SCL7
P4_5/$\overline{\text{CS1}}$	P4_5/CLK7/$\overline{\text{CS1}}$	Added: CLK7
P4_4/$\overline{\text{CS0}}$	P4_4/$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$/$\overline{\text{CS0}}$	Added: $\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$
P3_0/A8	P3_0/ A8, [A8/D7]	Added: [A8/D7]
P2_7/A7	P2_7/AN2_7/A7, [A7/D7], [A7/D6]	Added: AN2_7/[A7/D7], [A7/D6]
P2_6/A6	P2_6/AN2_6/A6, [A6/D6], [A6/D5]	Added: AN2_6/[A6/D6], [A6/D5]
P2_5/A5	P2_5/$\overline{\text{INT7}}$/AN2_5/A5, [A5/D5], [A5/D4]	Added: $\overline{\text{INT7}}$/AN2_5/ [A5/D5], [A5/D4]
P2_4/A4	P2_4/$\overline{\text{INT6}}$/AN2_4/A4, [A4/D4], [A4/D3]	Added: $\overline{\text{INT6}}$/ AN2_4/ [A4/D4], [A4/D3]
P2_3/A3	P2_3/AN2_3/A3, [A3/D3], [A3/D2]	Added: AN2_3/[A3/D3], [A3/ D2]
P2_2/A2	P2_2/AN2_2/A2, [A2/D2], [A2/D1]	Added: AN2_2/[A2/D2], [A2/D1]
P2_1/A1	P2_1/AN2_1/A1, [A1/D1], [A1/D0]	Added: AN2_1/[A1/D1], [A1/D0]
P2_0/A0	P2_0/AN2_0/A0, [A0/D0], A0	Added: AN2_0/[A0/D0], A0

Table 3.4 Differences in Pin Characteristics (2/2)

M16C/30P	M16C/64A	Changes from M16C/30P
P1_7/D15	P1_7/$\overline{\text{INT5}}$/IDU/D15	Added: $\overline{\text{INT5}}$/IDU
P1_6/$\overline{\text{INT4}}$/D14	P1_6/$\overline{\text{INT4}}$/IDW/D14	Added: IDW
P1_5/$\overline{\text{INT3}}$/D13	P1_5/$\overline{\text{INT3}}$/IDV/D13	Added: IDV
P1_3/D11	P1_3/TXD6/SDA6/D11	Added: TXD6/SDA6
P1_2/D10	P1_2/RXD6/SCL6/D10	Added: RXD6/SCL6
P1_1/D9	P1_1/CLK6/D9	Added: CLK6
P1_0/D8	P1_0/$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/D8	Added: $\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$
P9_7/$\overline{\text{ADTRG}}$	P9_7/SIN4/$\overline{\text{ADTRG}}$	Added: SIN4

4. Detailed Comparison

4.1 Differences in Protections

Table 4.1 lists Differences in Registers Associated with Protect Function.

Table 4.1 Differences in Registers Associated with Protect Function

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PRCR	000Ah	000Ah	0	Protect bit 0 Enable write to registers CM0, CM1, and PCLKR	Protect bit 0 Enable write to registers CM0, CM1, CM2, PLC0, and PCLKR
			1	Protect bit 1 Enable write to registers PM0, and PM1	Protect bit 1 Enable write to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1
			2	Protect bit 2 Enable write to the PD9 register	Protect bit 2 Enable write to registers PD9, S3C, and S4C
			3	Reserved bit	Protect bit 3 Enable write to registers VCR2, VWCE, VD1LS, VW0C, VW1C, and VW2C
			6	No register bit	Protect bit 6 Enable write to the PRG2C register

4.2 Differences in Resets

Table 4.2 lists Differences in Resets and Table 4.3 lists Difference in Registers Associated with Resets.

Table 4.2 Differences in Resets

Item	M16C/30P	M16C/64A
Types of resets	Hardware reset Software reset	Hardware reset Software reset Voltage monitor 0 reset Voltage monitor 1 reset Voltage monitor 2 reset Power-on reset Oscillation stop detect reset Watchdog timer reset
Cold start, warm start discrimination method	WDC5 bit in the WDC register	CWR bit in the RSTFR register (operates at the same time as voltage monitor 0 reset)

Table 4.3 Difference in Registers Associated with Resets

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
RSTFR	—	0018h	—	—	M16C/64A only

4.3 Difference in Clock Generator

Table 4.4 lists Differences in Clock Generators and Table 4.5 lists Differences in Registers Associated with Clock Generation.

Table 4.4 Differences in Clock Generators

Item	M16C/30P	M16C/64A
Types of clocks	Main clock oscillation circuit (0 to 16 MHz), Sub clock oscillation circuit (32.768 kHz)	Main clock oscillation circuit (0 to 20 MHz), Sub clock oscillation circuit (32.768 kMz), PLL frequency synthesizer (10 to 25 MHz), 125 kHz on-chip oscillator (125 kHz)
Clock output function	Selectable from fC, f8, and f32	Selectable from fC, f8, f32, and f1
CPU clock after reset	Main clock (default setting of the CM07 bit: 0)	125 kHz on-chip oscillator clock (default setting of CM21 bit: 1)
Peripheral clock (fC)	Supply constantly	Provided/not provided selected using the PM25 bit
System clock protection function	No (protected by the Protect Register)	Yes
Oscillator stop/restart detect function	No	Yes

CM07: Bit in the CM0 register
CM21: Bit in the CM2 register
PM25: Bit in the PM2 register

Table 4.5 Differences in Registers Associated with Clock Generation

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
CM0	0006h	0006h	7	System clock select bit 0: Main clock 1: Sub clock	System clock select bit 0: Main clock, PLL clock or on-chip oscillator clock 1: Sub clock
CM1	0007h	0007h	1	Reserved bits	System clock select bit 1 0: Main clock 1: PLL clock
			3		XIN-XOUT feedback resistor select bit 0: Internal feedback resistor connected 1: Internal feedback resistor not connected
			4		125 kHz on-chip oscillator oscillation stop bit 0: 125 kHz on-chip oscillator on 1: 125 kHz on-chip oscillator off
PCLKR	025Eh	0012h	—	Different address	
			0	Timers A, B clock select Bit (Clock source for the timers A and B) 0: f2 1: f1	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and multi-master I^2C-bus interface) 0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC
			5	Reserved bit	Clock output function expansion bit (enabled in single-chip mode) 0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1
CM2	—	000Ch	—	—	M16C/64A only
PLC0	—	001Ch	—	—	M16C/64A only
PM2	—	001Eh	—	—	M16C/64A only

4.4 Differences in Power Controls

Table 4.6 lists Differences in Power Controls and Table 4.7 lists Differences in Registers Associated with Power Control.

Table 4.6 Differences in Power Controls

Item	M16C/30P	M16C/64A
Slow read mode	No	Yes
Low current consumption read mode	No	Yes

Table 4.7 Differences in Registers Associated with Power Control

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
FMR2	—	0222h	—	—	M16C/64A only

4.5 Differences in Processor Modes

Table 4.8 lists Differences in Registers Associated with Processor Mode.

Table 4.8 Differences in Registers Associated with Processor Mode

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PM1	0005h	0005h	0	$\overline{CS2}$ area switch bit 0: 08000h to 26FFFh (block A disabled) 1: 10000h to 26FFFh (block A enabled)	$\overline{CS2}$ area switch bit 0: $\overline{CS2}$ area (0E000h to 0FFFFh) 1: Data flash (0E000h to 0FFFFh)
			3	No register bit	Internal area expansion bit 0
PRG2C	—	0010h	—	—	M16C/64A only

4.6 Differences in Buses

Table 4.9 lists Differences in Buses and Table 4.10 lists Differences in Registers Associated with Bus.

Table 4.9 Differences in Buses

Item	M16C/30P	M16C/64A
Bus mode	Separate bus	Selectable from separate bus and multiplexed bus
Upper address in memory extension mode or microprocessor mode	P4_0 to P4_3 (A16 to A19): selectable from address bus and I/O port P3_4 to P3_7 (A12 to A15): address bus	P4_0 to P4_3 (A16 to A19) P3_4 to P3_7 (A12 to A15): selectable from address bus and I/O port

Table 4.10 Differences in Registers Associated with Bus

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PM0	0004h	0004h	5-4	Reserved bits	Multiplexed bus space select bit 00: Multiplexed bus is unused (separate bus in the entire $\overline{CS}$ space) 01: Allocated to $\overline{CS2}$ space 10: Allocated to $\overline{CS1}$ space 11: Allocated to the entire $\overline{CS}$ space
PM1	0005h	0005h	1	No register bit	Port P3_7 to P3_4 function select bit 0: Address output 1: Port function
CSE	—	001Bh	—	—	M16C/64A only

4.7 Differences in Memory Space Expansion Functions

Table 4.11 lists Differences in Memory Space Expansion Functions and Table 4.12 lists Differences in Registers Associated with Memory Space Expansion Function.

Table 4.11 Differences in Memory Space Expansion Functions

Item	M16C/30P	M16C/64A
Memory space	1-MB mode	1-MB mode, 4-MB mode

Table 4.12 Differences in Registers Associated with Memory Space Expansion Function

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PM1	0005h	0005h	5-4	No register bits	Memory area expansion bit 00: 1-Mbyte mode (no expansion) 01: Do not set 10: Do not set 11: 4-Mbyte mode
DBR	—	000Bh	—	—	M16C/64A only

4.8 Differences in Programmable I/O Ports

Table 4.13 lists Differences in Programmable I/O Ports and Table 4.14 lists Differences in Registers Associated with Programmable I/O Ports.

Table 4.13 Differences in Programmable I/O Ports

Item	M16C/30P	M16C/64A
$\overline{\text{NMI}}$/$\overline{\text{SD}}$ digital filter	No	The digital filter can be enabled/disabled by setting the NMIDF register

Table 4.14 Differences in Registers Associated with Programmable I/O Ports

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PD8	03F2h	03F2h	5	No register bit	Port P8_5 direction bit 0: Input mode (Functions as an input port) 1: Output mode (Functions as an output port)
PUR0	03FCh	0360h	—	Different address	
PUR1	03FDh	0361h	—	Different address	
PUR2	03FEh	0362h	—	Different address	
PCR	03FFh	0366h	—	Different address	
NMIDF	—	0369h	—	—	M16C/64A only

4.9 Differences in Interrupts

Table 4.15 lists Differences in Interrupts and Table 4.16 to Table 4.17 list Differences in Interrupt Vectors, and Table 4.18 to Table 4.19 list Difference in Registers Associated with Interrupts (2/2).

Table 4.15 Differences in Interrupts

Item	M16C/30P	M16C/64A
$\overline{\text{NMI}}$ enable function	Enable only	Enable/disable selectable using the PM24 bit in the PM2 register
Address match interrupt	2 addresses	4 addresses

Table 4.16 Differences in Interrupt Vectors - (1/2)

Software Interrupt Number	Vector Address	M16C/30P	M16C/64A
0	+0 to +3 (0000h to 0003h)	BRK instruction	BRK instruction
1	+4 to +7 (0004h to 0007h)	— (Reserved)	INT instruction interrupt
2	+8 to +11 (0008h to 000Bh)		$\overline{\text{INT7}}$
3	+12 to +15 (000Ch to 000Fh)		$\overline{\text{INT6}}$
4	+16 to +19 (0010h to 0013h)	$\overline{\text{INT3}}$	$\overline{\text{INT3}}$
5	+20 to +23 (0014h to 0017h)	— (Reserved)	Timer B5
6	+24 to +27 (0018h to 001Bh)	UART1 start/stop condition detection, bus collision detection	Timer B4, UART1 start/stop condition detection, bus collision detection
7	+28 to +31 (001Ch to 001Fh)	UART0 start/stop condition detection, bus collision detection	Timer B3, UART0 start/stop condition detection, bus collision detection
8	+32 to +35 (0020h to 0023h)	— (Reserved)	SI/O4, $\overline{\text{INT5}}$
9	+36 to +39 (0024h to 0027h)	$\overline{\text{INT4}}$	SI/O3, $\overline{\text{INT4}}$
10	+40 to +43 (0028h to 002Bh)	UART2 start/stop condition detection, bus collision detection	UART2 start/stop condition detection, bus collision detection
11	+44 to +47 (002Ch to 002Fh)	DMA0	DMA0
12	+48 to +51 (0030h to 0033h)	DMA1	DMA1
13	+52 to +55 (0034h to 0037h)	Key input interrupt	Key input interrupt
14	+56 to +59 (0038h to 003Bh)	A/D converter	A/D converter
15	+60 to +63 (003Ch to 003Fh)	UART2 transmit, NACK2	UART2 transmit, NACK2
16	+64 to +67 (0040h to 0043h)	UART2 receive, ACK2	UART2 receive, ACK2
17	+68 to +71 (0044h to 0047h)	UART0 transmit, NACK0	UART0 transmit, NACK0
18	+72 to +75 (0048h to 004Bh)	UART0 receive, ACK0	UART0 receive, ACK0
19	+76 to +79 (004Ch to 004Fh)	UART1 transmit, NACK1	UART1 transmit, NACK1
20	+80 to +83 (0050h to 0053h)	UART1 receive, ACK1	UART1 receive, ACK1
21	+84 to +87 (0054h to 0057h)	Timer A0	Timer A0
22	+88 to +91 (0058h to 005Bh)	Timer A1	Timer A1
23	+92 to +95 (005Ch to 005Fh)	Timer A2	Timer A2
24	+96 to +99 (0060h to 0063h)	— (Reserved)	Timer A3
25	+100 to +103 (0064h to 0067h)	— (Reserved)	Timer A4
26	+104 to +107 (0068h to 006Bh)	Timer B0	Timer B0
27	+108 to +111 (006Ch to 006Fh)	Timer B1	Timer B1
28	+112 to +115 (0070h to 0073h)	Timer B2	Timer B2

Table 4.17 Differences in Interrupt Vectors - (2/2)

Software Interrupt Number	Vector Address	M16C/30P	M16C/64A
29	+116 to +119 (0074h to 0077h)	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$
30	+120 to +123 (0078h to 007Bh)	$\overline{\text{INT1}}$	$\overline{\text{INT1}}$
31	+124 to +127 (007Ch to 007Fh)	$\overline{\text{INT2}}$	$\overline{\text{INT2}}$
32 to 40	+128 to +131 (0080h to 0083h) to +160 to +163 (00A0h to 00A3h)	INT instruction interrupt	INT instruction interrupt
41	+164 to +167 (00A4h to 00A7h)		DMA2
42	+168 to +171 (00A8h to 00ABh)		DMA3
43	+172 to +175 (00ACh to 00AFh)		UART5 start/stop condition detection, bus collision detection, CEC1
44	+176 to +179 (00B0h to 00B3h)		UART5 transmit, NACK5, CEC2
45	+180 to +183 (00B4h to 00B7h)		UART5 receive, ACK5
46	+184 to +187 (00B8h to 00BBh)		UART6 start/stop condition detection, bus collision detection, real-time clock period
47	+188 to +191 (00BCh to 00BFh)		UART6 transmit, NACK6, real-time clock compare
48	+192 to +195 (00C0h to 00C3h)		UART6 receive, ACK6
49	+196 to +199 (00C4h to 00C7h)		UART7 start/stop condition detection, bus collision detection, remote control 0
50	+200 to +203 (00C8h to 00CBh)		UART7 transmit, NACK7, remote control 1
51	+204 to +207 (00CCh to 00CFh)		UART7 receive, ACK7
52 to 58	+208 to +211 (00D0h to 00D3h) to +232 to +235 (00E8h to 00EBh)		INT instruction interrupt
59	+236 to +239 (00ECh to 00EFh)		I^2C-bus interface interrupt
60	+240 to +243 (00F0h to 00F3h)		SCL/SDA interrupt
61 to 63	+244 to +247 (00F4h to 00F7h) to +252 to +255 (00FCh to 00FFh)		INT instruction interrupt

Table 4.18 Differences in Registers Associated with Interrupts (1/2)

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PCR	03FFh	0366h	—	Different address	
			5	No register bits	$\overline{\text{INT6}}$ input enable bit 0: Enabled 1: Disabled
			6		$\overline{\text{INT7}}$ input enable bit 0: Enabled 1: Disabled
			7		Key input enable bit 0: Enabled 1: Disabled

Table 4.19 Difference in Registers Associated with Interrupts (2/2)

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PM2	—	001Eh	4	No register bit	$\overline{\text{NMI}}$ interrupt enable bit 0: $\overline{\text{NMI}}$ interrupt disabled 1: $\overline{\text{NMI}}$ interrupt enabled
IFSR3A	—	0205h	—	—	M16C/64A only
IFSR2A	035Eh	0206h	—	Different address	
			2	No register bits	Interrupt request source select bit 0: Not used 1: I^2C-bus interface
			3		Interrupt request source select bit 0: Not used 1: SCL/SDA
			4		Interrupt request source select bit 0: UART7 start/stop condition detection, bus collision detection 1: Remote control 0
			5		Interrupt request source select bit 0: UART7 transmission, NACK 1: Remote control 1
			6	Interrupt request factor select bit 0: Do not set 1: UART0 bus collision detection	Interrupt request source select bit 0: Timer B3 1: UART0 start/stop condition detection, bus collision detection
			7	Interrupt request factor select bit 0: Do not set 1: UART1 bus collision detection	Interrupt request source select bit 0: Timer B4 1: UART1 start/stop condition detection, bus collision detection
IFSR	035Fh	0207h	—	Different address	
			5	Reserved bit	$\overline{\text{INT5}}$ interrupt polarity select bit 0: One edge 1: Both edges
			6	Interrupt request factor select bit 0: $\overline{\text{Do}}$ not set 1: $\overline{\text{INT4}}$	Interrupt request source select bit 0: $\overline{\text{SI/O3}}$ 1: $\overline{\text{INT4}}$
			7	Reserved bit	Interrupt request source select bit 0: $\overline{\text{SI/O4}}$ 1: $\overline{\text{INT5}}$
AIER	0009h	020Eh	—	Different address	
AIER2	—	020Fh	—	—	M16C/64A only
RMAD0	0010h to 0012h	0210h to 0212h	—	Different address	
RMAD1	0014h to 0016h	0214h to 0216h	—	Different address	
RMAD2	—	0218h to 021Ah	—	—	M16C/64A only
RMAD3	—	021Ch to 021Eh	—	—	M16C/64A only

4.10 Differences in Watchdog Timers

Table 4.20 lists Differences in Watchdog Timers and Table 4.21 lists Differences in Registers Associated with Watchdog Timer.

Table 4.20 Differences in Watchdog Timers

Item	M16C/30P	M16C/64A
Count source protection mode	No	Yes
Operation when the timer underflows	Watchdog timer interrupt	Selectable from watchdog timer interrupt and watchdog timer reset
Watchdog timer counter initialization	Watchdog timer counter is initialized and starts counting by writing to the WDTS register.	Write 00h, and then FFh to the WDTR register
Count start condition		• Count starts automatically after reset when the WDTON bit in the OFS1 address to 0. • Count starts by writing to the WDTS register.

Table 4.21 Differences in Registers Associated with Watchdog Timer

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PM1	0005h	0005h	2	Reserved bit	Watchdog timer function select bit 0: Watchdog timer interrupt 1: Watchdog timer reset
WDTS	000Eh	037Eh	—	Different address	
WDC	000Fh	037Fh	—	Different address	
			5	Cold start/warm start discrimination flag 0: Cold Start 1: Warm Start	No register bit
VW2C	—	002Ch	—	—	M16C/64A only
CSPR	—	037Ch	—	—	M16C/64A only
WDTR	—	037Dh	—	—	M16C/64A only
30P: ROMCP 64A: OFS1	FFFFFh	FFFFFh	0	Reserved bit Set to 1	Watchdog timer start select bit 0: Watchdog timer starts automatically after reset 1: Watchdog timer is stopped after reset
			7	ROM code protect level 1 set bit	After-reset count source protection mode select bit 0: Count source protection mode enabled after reset. 1: Count source protection mode disabled after reset.

4.11 Differences in DMACs

Table 4.22 lists Differences in DMACs, Table 4.23 to 4.24 list Differences in DMA Request Sources, and Table 4.25 lists Differences in Registers Associated with DMAC.

Table 4.22 Differences in DMACs

Item	M16C/30P	M16C/64A
Number of channels	2 channels	4 channels

Table 4.23 Differences in DMAi Request Sources (i=0 and 1 in M16C/30P; i=0 to 3 in M16C/64A)(1/2)

DSEL4 to DSEL0	M16C/30P		M16C/64A	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b	Falling edge of $\overline{\text{INTi}}$ pin	—	Falling edge of $\overline{\text{INTi}}$ pin	—
00001b	Software trigger	—	Software trigger	—
00010b	Timer A0	—	Timer A0	—
00011b	Timer A1	—	Timer A1	—
00100b	Timer A2	—	Timer A2	—
00101b	—	—	Timer A3	SI/O3 (DMA1, DMA3 only)
00110b	—	DMA0: Both edges of $\overline{\text{INTi}}$ pin DMA1: —	Timer A4	DMA0, DMA2: Both edges of $\overline{\text{INTi}}$ pin DMA1, DMA3: SI/O4
00111b	Timer B0	DMA0, DMA2: — DMA1, DMA3: Both edges of $\overline{\text{INTi}}$ pin	Timer B0	DMA0, DMA2: Timer B3 DMA1,DMA3: Both edges of $\overline{\text{INTi}}$ pin
01000b	Timer B1	—	Timer B1	Timer B4 (DMA0, DMA2 only)
01001b	Timer B2	—	Timer B2	Timer B5 (DMA0, DMA2 only)
01010b	UART0 transmission	—	UART0 transmission	—
01011b	DMA0: UART0 reception DMA1: UART0 reception/ACK0	—	DMA0, DMA2: UART0 reception DMA1, DMA3: UART0 reception/ACK0	—
01100b	UART2 transmission	—	UART2 transmission	—
01101b	DMA0: UART2 reception DMA1: UART2 reception/ACK2	—	DMA0, DMA2: UART2 reception DMA1, DMA3: UART2 reception/ACK2	—
01110b	A/D converter	—	A/D converter	—
01111b	DMA0: UART1 transmission DMA1: UART1 reception/ACK1	—	DMA0, DMA2: UART1 transmission DMA1, DMA3: UART1 reception/ACK1	—

Table 4.24 Differences in DMAi Request Sources (i=0 and 1 in M16C/30P; i=0 to 3 in M16C/64A)(2/2)

DSEL4 to DSEL0	M16C/30P		M16C/64A	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
10000b			DMA0, DMA2: UART1 reception DMA1, DMA3: UART1 transmission	Falling edge of $\overline{\text{INTj}}$ pin (j = 4 to 7)
10001b			UART5 transmission	Both edges of $\overline{\text{INTj}}$ pin
10010b			DMA0, DMA2: UART5 reception DMA1, DMA3: UART5 reception/ACK5	—
10011b			UART6 transmission	—
10100b			DMA0, DMA2: UART6 reception DMA1, DMA3: UART6 reception/ACK6	—
10101b			UART7 transmission	—
10110b			DMA0, DMA2: UART7 reception DMA1, DMA3 UART7 reception/ACK7	—

Table 4.25 Differences in Registers Associated with DMAC

Symbol	Address		Bits	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
SAR0	0020h to 0022h	0180h to 0182h	—	Different address	
SAR1	0030h to 0032h	0190h to 0192h	—	Different address	
SAR2	—	01A0h to 01A2h	—	—	M16C/64A only
SAR3	—	01B0h to 01B2h	—	—	M16C/64A only
DAR0	0024h to 0026h	0184h to 0186h	—	Different address	
DAR1	0034h to 0036h	0194h to 0196h	—	Different address	
DAR2	—	01A4h to 01A6h	—	—	M16C/64A only
DAR3	—	01B4h to 01B6h	—	—	M16C/64A only
TCR0	0028h to 0029h	0188h to 0189h	—	Different address	
TCR1	0038h to 0039h	0198h to 0199h	—	Different address	
TCR2	—	01A8h to 01A9h	—	—	M16C/64A only
TCR3	—	01B8h to 01B9h	—	—	M16C/64A only
DM0CON	002Ch	018Ch	—	Different address	
DM1CON	003Ch	019Ch	—	Different address	
DM2CON	—	01ACh	—	—	M16C/64A only
DM3CON	—	01BCh	—	—	M16C/64A only
DM0SL	03B8h	0398h	—	Different address	
DM1SL	03BAh	039Ah	—	Different address	
DM2SL	—	0390h	—	—	M16C/64A only
DM3SL	—	0392h	—	—	M16C/64A only

4.12 Differences in Timers

Table 4.26 lists Differences in Timers, and Table 4.27 to Table 4.29 list Differences in Registers Associated with Timer.

Table 4.26 Differences in Timers

Item	M16C/30P	M16C/64A
Count source	f1, f2, f8, f32, fC32	f1, f2, f8, f32, f64, fOCO-S, fC32
Output polarity inversion function	No	Yes
Programmable output mode	No	Yes
Multiply-by-4 processing operation in event counter mode (when processing two-phase pulse signal)	No	Timer A3: Selectable from normal and multiply-by-4 processing operation Timer A4: Multiply-by-4 processing operation (fixed)
Counter reset by Z-phase input	No	Timer A3
Count direction (up/down) selected by the TAiOUT pin (i = 0 to 2)	Yes	No
Default value in pulse period/pulse width measurement modes	Undefined	Programmable
Read from timer register in pulse period/pulse width measurement modes	Contents of the reload register (measurement result) can be read by reading the TBi register.	When bits PPWFSk2 to PPWFSk0 in the PPWFSk register (k = 1 and 2) are 0: • Contents of the reload register (measurement result) can be read by reading the TBj register (j = 0 to 5). When bits PPWFSk2 to PPWFSk0 in the PPWFSk register are 1: • Contents of the counter (counter value) can be read by reading the TBj register • Contents of the reload register (measurement result) can be read by reading the TBj1 register
Overflow flag clear method	When the TBiS bit is 1 (start counting), write to the TBiMR register at the next count timing or later after the MR3 bit is set to 1 (overflowed).	Write a value to the TBjMR register

Table 4.27 Differences in Registers Associated with Timer (1/3)

Symbol	Address		Bits	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PCLKR	025Eh	0012h	—	Different address	
CPSRF	0381h	0015h	—	Different address	
TACS0 to TACS2	—	01D0h to 01D2h	2 - 0	—	TAi count source select bit (i = 0, 2, and 4) Select the TAi count source
			3	—	TAi count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4	—	TAj count source select bit (j = 1 and 3) Select the TAj count source
			7	—	TAj count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TA0MR to TA2MR	0396h to 0398h	0336h to 0338h	—	Different address	
			4 (1)	Up/Down switching factor select bit 0: UDF register 1: Input signal to TAiOUT pin	Set to 0 in event counter mode
TA3MR	—	0339h	—	—	M16C/64A only
TA4MR	—	033Ah	—	—	M16C/64A only
TA0	0386h to 0387h	0326h to 0327h	—	Different address	
TA1	0388h to 0389h	0328h to 0329h	—	Different address	
TA2	038Ah to 038Bh	032Ah to 032Bh	—	Different address	
TA3	—	032Ch to 032Dh	—	—	M16C/64A only
TA4	—	032Eh to 032Fh	—	—	M16C/64A only
TABSR	0380h	0320h	—	Different address	
			3	No register bits	Timer A3 count start flag 0: Stop counting 1: Start counting
			4		Timer A4 count start flag 0: Stop counting 1: Start counting

Note:
1. Bit 4 is difference in the event counter mode (when not processing two-phase pulse signal).

Table 4.28 Differences in Registers Associated with Timer (2/3)

Symbol	Address		Bits	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
UDF	0384h	0324h	—	Different address	
			3	No register bits	Timer A3 up/down flag 0: Decrement 1: Increment
			4		Timer A4 up/down flag 0: Decrement 1: Increment
			6		Timer A3 two-phase pulse signal processing select bit 0: Two-phase pulse signal processing disabled 1: Two-phase pulse signal processing enabled
			7		Timer A4 two-phase pulse signal processing select bit 0: Two-phase pulse signal processing disabled 1: Two-phase pulse signal processing enabled
ONSF	0382h	0322h	—	Different address	
			3	No register bits	Timer A3 one-shot start flag The timer starts counting by setting this bit to 1. Read as 0
			4		Timer A4 one-shot start flag The timer starts counting by setting this bit to 1. Read as 0
			5		Z-phase input enable bit 0: Z-phase input disabled 1: Z-phase input enabled
			7-6	Timer A0 event/trigger select bit 00: Input on TA0IN is selected 01: TB2 is selected 10: Do not set 11: TA1 is selected	Timer A0 event/trigger select bit 00: Input on TA0IN pin selected 01: Timer B2 selected 10: Timer A4 selected 11: Timer A1 selected
TRGSR	0383h	0323h	—	Different address	
			3-2	Timer A2 event/trigger select bit 00: Input on TA2IN is selected 01: TB2 is selected 10: TA1 is selected 11: Do not set	Timer A2 event/trigger select bit 00: Input on TA2IN selected 01: TB2 selected 10: TA1 selected 11: TA3 selected
			5-4	No register bits	Timer A3 event/trigger select bit 00: Input on TA3IN selected 01: TB2 selected 10: TA2 selected 11: TA4 selected
			7-6		Timer A4 event/trigger select bit 00: Input on TA4IN selected 01: TB2 selected 10: TA3 selected 11: TA0 selected

Table 4.29 Differences in Registers Associated with Timer (3/3)

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PWMFS	—	01D4h	—	—	M16C/64A only
TAPOFS	—	01D5h	—	—	M16C/64A only
TAOW	—	01D8h	—	—	M16C/64A only
TA11	—	0302h to 0303h	—	—	M16C/64A only
TA21	—	0304h to 0305h	—	—	M16C/64A only
TA41	—	0306h to 0307h	—	—	M16C/64A only
TBCS0 TBCS1 TBCS2 TBCS3	—	01C8h 01C9h 01E8h 01E9h	2 - 0	—	TBi count source select bit (i = 0, 2, 3, and 5) Select the TBi count source
			3	—	TBi count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4	—	TBj count source select bit (j = 1 and 4) Select the TBj count source
			7	—	TBj count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TB0MR to TB2MR	039Bh to 039Dh	033Bh to 033Dh	—	Different address	
TB3MR to TB5MR	—	031Bh to 031Dh	—	—	M16C/64A only
TB0	0390h to 0391h	0330h to 0331h	—	Different address	
TB1	0392h to 0393h	0332h to 0333h	—	Different address	
TB2	0394h to 0395h	0334h to 0335h	—	Different address	
TB3	—	0310h to 0311h	—	—	M16C/64A only
TB4	—	0312h to 0313h	—	—	M16C/64A only
TB5	—	0314h to 0315h	—	—	M16C/64A only
TBSR	—	0300h	—	—	M16C/64A only
PPWFS1	—	01C6h	—	—	M16C/64A only
PPWFS2	—	01E6h	—	—	M16C/64A only
TB01	—	01C0h to 01C1h	—	—	M16C/64A only
TB11	—	01C2h to 01C3h	—	—	M16C/64A only
TB21	—	01C4h to 01C5h	—	—	M16C/64A only
TB31	—	01E0h to 01E1h	—	—	M16C/64A only
TB41	—	01E2h to 01E3h	—	—	M16C/64A only
TB51	—	01E4h to 01E5h	—	—	M16C/64A only

4.13 Differences in Serial Interfaces

Table 4.30 lists Differences in Serial Interfaces, and Table 4.31 to Table 4.32 list Differences in Registers Associated with Serial Interface.

Table 4.30 Differences in Serial Interfaces

Item	M16C/30P	M16C/64A
Clock synchronous/asynchronous	3 channels (UART0 to UART2)	6 channels (UART0 to 2, UART5 to 7)
Clock-synchronous only	No	2 channels (SI/O3, SI/O4)
Special mode 3 (IE mode)	1 channel (UART2 only)	6 channels (UART0 to 2, UART5 to 7)

Table 4.31 Differences in Registers Associated with Serial Interface (1/2)

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PCLKR	025Eh	0012h	—	Different address	
U0TB	03A2h to 03A3h	024Ah to 024Bh	—	Different address	
U1TB	03AAh to 03ABh	025Ah to 025Bh	—	Different address	
U2TB	037Ah to 037Bh	026Ah to 026Bh	—	Different address	
U5TB	—	028Ah to 028Bh	—	—	M16C/64A only
U6TB	—	029Ah to 029Bh	—	—	M16C/64A only
U7TB	—	02AAh to 02ABh	—	—	M16C/64A only
U0RB	03A6h to 03A7h	024Eh to 024Fh	—	Different address	
U1RB	03AEh to 03AFh	025Eh to 025Fh	—	Different address	
U2RB	037Eh to 037Fh	026Eh to 026Fh	—	Different address	
U5RB	—	028Eh to 028Fh	—	—	M16C/64A only
U6RB	—	029Eh to 029Fh	—	—	M16C/64A only
U7RB	—	02AEh to 02AFh	—	—	M16C/64A only
U0BRG	03A1h	0249h	—	Different address	
U1BRG	03A9h	0259h	—	Different address	
U2BRG	0379h	0269h	—	Different address	
U5BRG	—	0289h	—	—	M16C/64A only
U6BRG	—	0299h	—	—	M16C/64A only
U7BRG	—	02A9h	—	—	M16C/64A only
U0MR	03A0h	0248h	—	Different address	
U1MR	03A8h	0258h	—	Different address	
U2MR	0378h	0268h	—	Different address	
U5MR	—	0288h	—	—	M16C/64A only
U6MR	—	0298h	—	—	M16C/64A only
U7MR	—	02A8h	—	—	M16C/64A only
U0C0	03A4h	024Ch	—	Different address	
U1C0	03ACh	025Ch	—	Different address	
U2C0	037Ch	026Ch	—	Different address	
U5C0	—	028Ch	—	—	M16C/64A only
U6C0	—	029Ch	—	—	M16C/64A only
U7C0	—	02ACh	—	—	M16C/64A only
U0C1	03A5h	024Dh	—	Different address	
U1C1	03ADh	025Dh	—	Different address	
U2C1	037Dh	026Dh	—	Different address	
U5C1	—	028Dh	—	—	M16C/64A only
U6C1	—	029Dh	—	—	M16C/64A only
U7C1	—	02ADh	—	—	M16C/64A only
UCON	03B0h	0250h	—	Different address	

Table 4.32 Differences in Registers Associated with Serial Interface (2/2)

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
U0SMR	036Fh	0247h	—	Different address	
U1SMR	0373h	0257h	—	Different address	
U2SMR	0377h	0267h	—	Different address	
U5SMR	—	0287h	—	—	M16C/64A only
U6SMR	—	0297h	—	—	M16C/64A only
U7SMR	—	02A7h	—	—	M16C/64A only
U0SMR2	036Eh	0246h	—	Different address	
U1SMR2	0372h	0256h	—	Different address	
U2SMR2	0376h	0266h	—	Different address	
U5SMR2	—	0286h	—	—	M16C/64A only
U6SMR2	—	0296h	—	—	M16C/64A only
U7SMR2	—	02A6h	—	—	M16C/64A only
U0SMR3	036Dh	0245h	—	Different address	
U1SMR3	0371h	0255h	—	Different address	
U2SMR3	0375h	0265h	—	Different address	
U5SMR3	—	0285h	—	—	M16C/64A only
U6SMR3	—	0295h	—	—	M16C/64A only
U7SMR3	—	02A5h	—	—	M16C/64A only
U0SMR4	036Ch	0244h	—	Different address	
U1SMR4	0370h	0254h	—	Different address	
U2SMR4	0374h	0264h	—	Different address	
U5SMR4	—	0284h	—	—	M16C/64A only
U6SMR4	—	0294h	—	—	M16C/64A only
U7SMR4	—	02A4h	—	—	M16C/64A only
S3TRR	—	0270h	—	—	M16C/64A only
S3C	—	0272h	—	—	M16C/64A only
S3BRG	—	0273h	—	—	M16C/64A only
S4TRR	—	0274h	—	—	M16C/64A only
S4C	—	0276h	—	—	M16C/64A only
S4BRG	—	0277h	—	—	M16C/64A only
S34C2	—	0278h	—	—	M16C/64A only

4.14 Differences in A/D Converters

Table 4.33 lists Differences in A/D Converters and Table 4.34 lists Differences in Registers Associated with A/D Converter.

Table 4.33 Differences in A/D Converters

Item	M16C/30P	M16C/64A
Operation modes	One-shot mode, repeat mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1
Conversion rate per pin	Without sample and hold 8-bit resolution: 49 ϕAD cycles 10-bit resolution: 59 ϕAD cycles With sample and hold 8-bit resolution: 28 ϕAD cycles 10-bit resolution: 33 ϕAD cycles	Minimum 43 ϕAD cycles
Resolution	Selectable from 8 bits or 10 bits	10 bits
Analog input pins	Total 18 pins 8 pins (AN0 to AN7) 2 pins (ANEX0 and ANEX1) 8 pins (AN0_0 to AN0_7)	Total 26 pins 8 pins (AN0 to AN7) 2 pins (ANEX0 and ANEX1) 8 pins (AN0_0 to AN0_7) 8 pins (AN2_0 to AN2_7)
Sample and hold	Yes/No (selectable)	Yes
Open-circuit detection assist function	No	Yes

Table 4.34 Differences in Registers Associated with A/D Converter

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
PCR	03FFh	0366h	—	Different address	
			5	No register bits	$\overline{\text{INT6}}$ input enable bit 0: Enabled 1: Disabled
			6		$\overline{\text{INT7}}$ input enable bit 0: Enabled 1: Disabled
			7		Key input enable bit 0: Enabled 1: Disabled
ADCON0	03D6h	03D6h	3	A/D operation mode select bit 0 0: One-shot mode 1: Repeat mode	A/D operation mode select bit 0 00: One-shot mode 01: Repeat mode 10: Single sweep mode 11: Repeat sweep mode 0 or repeat sweep mode 1
			4	No register bit	
ADCON1	03D7h	03D7h	1-0	No register bits	A/D sweep pin select bit In single sweep mode or repeat sweep mode 0 00: AN0 to AN1 (2 pins) 01: AN0 to AN3 (4 pins) 10: AN0 to AN5 (6 pins) 11: AN0 to AN7 (8 pins) In repeat sweep mode 1 0 0: AN0 (1 pin) 0 1: AN0 to AN1 (2 pins) 1 0: AN0 to AN2 (3 pins) 1 1: AN0 to AN3 (4 pins)
			2		A/D operation mode select bit 1 0: Any mode other than repeat sweep mode 1 1: Repeat sweep mode 1
			3	8/10-bit mode select bit 0: 8-bit mode 1: 10-bit mode	No register bit
			5	Vref connect bit 0: Vref not connected 1: Vref connected	A/D standby bit 0: A/D operation stopped (standby) 1: A/D operation enabled
ADCON2	03D4h	03D4h	0	A/D conversion method select bit 0: Without sample and hold 1: With sample and hold	No register bit
			1	No register bit	A/D input group select bit 00: AN0 to AN7 01: Do not set 10: AN0_0 to AN0_7 11: AN2_0 to AN2_7
			2	A/D input group select bit 0: Port P10 group is selected 1: Port P0 group is selected	
AINRST	—	03A2h	—	—	M16C/64A only

4.15 Differences in CRC Calculators

Table 4.35 lists Differences in CRC Calculators and Table 4.36 lists Differences in Registers Associated with CRC Calculator.

Table 4.35 Differences in CRC Calculators

Item	M16C/30P	M16C/64A
CRC generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
MSB/LSB selection	No	MSB/LSB selectable
CRC snoop	No	Yes

Table 4.36 Differences in Registers Associated with CRC Calculator

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
CRCSAR	—	03B4h to 03B5h	—	—	M16C/64A only
CRCMR	—	03B6h	—	—	M16C/64A only

4.16 Differences in Flash Memories

Table 4.37 lists Differences in Flash Memories and Table 4.38 lists Differences in Software Commands, and 4.39 lists Differences in Registers Associated with Flash Memory.

Table 4.37 Differences in Flash Memories

Item	M16C/30P	M16C/64A
Program method	1-word (16-bit) units	2-word (32-bit) units
Number of program and erase cycles	100 times	• 1,000 times (program ROM 1, program ROM 2) • 10,000 times (data flash)
User boot function	No	Yes

Table 4.38 Differences in Software Commands

Software Commands	M16C/30P				M16C/64A					
	First bus cycle		Second bus cycle		First bus cycle		Second bus cycle		Third bus cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Program	WA	XX40h	WA	WD	WA	XX41h	WA	WD0	WA	WD1
Block blank check	—	—	—	—	X	XX25h	BA	XXD0h	—	—

WA: Write address (Even number. For M16C/64A, set the address which ends with 0h, 4h, 8h, or Ch.)
WD: Write data (16 bits)
WD0: Write data low-order word (16 bits)
WD1: Write data high-order word (16 bits)
BA: Highest-order block address (even address)
X: Any even address in user ROM area
XX: Eight high-order bits of command code (ignored)

Table 4.39 Differences in Registers Associated with Flash Memory

Symbol	Address		Bit	Differences	
	M16C/30P	M16C/64A		M16C/30P	M16C/64A
FMR0	01B7h	0220h	—	Different address	
			5	User ROM area select bit (Effective in only boot mode) 0: Boot ROM area is accessed 1: User ROM area is accessed	Reserved bit Set to 0 in other than user boot mode Set to 1 in user boot mode
FMR1	01B5h	0221h	—	Different address	
			1	EW1 mode select bit 0: EW0 mode 1: EW1 mode	Write to FMR6 register enable bit 0: Disabled 1: Enabled
			7	Reserved bit	Data flash wait bit 0: 1 wait 1: Follow the setting of the PM17 bit
FMR2	—	0222h	—	—	M16C/64A only
FMR6	—	0230h	—	—	M16C/64A only
30P: ROMCP 64A: OFS1	FFFFFh	FFFFFh	2	Reserved bits	ROM code protect cancel bit 0: ROM code protection cancelled 1: ROMCP1 bit enabled
			3		ROM code protect bit 0: ROM code protection enabled 1: ROM code protection disabled
			6	ROM code protect level 1 set bit 00:] 01:] ROM code protection active 10:] 11: ROM code protection inactive	Voltage detector 0 start bit 0: Voltage monitor 0 reset enabled after hardware reset. 1: Voltage monitor 0 reset disabled after hardware reset.
			7		After-reset count source protection mode select bit 0: Count source protection mode enabled after reset. 1: Count source protection mode disabled after reset.

4.17 Differences in Flash Memory Block Structures

The flash memory block structure differs between M16C/30P and M16C/64A Groups. Figure 4.1 shows Differences in Flash Memory Block Structures between M16C/30P 192 KB version and M16C/64A 512 KB version.

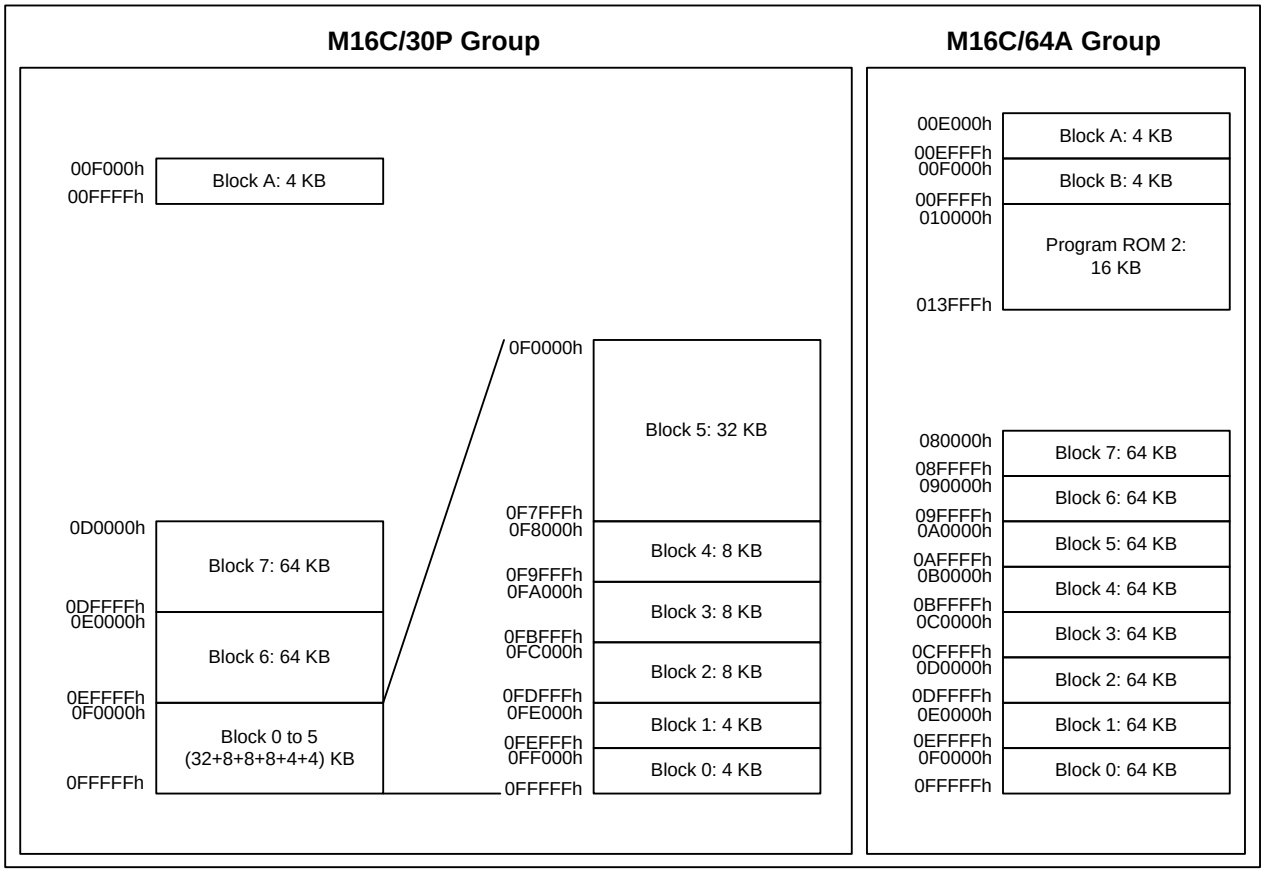

Figure 4.1 Differences in Flash Memory Block Structures

4.18 New Functions Added in M16C/64A

The following functions have been added in the M16C/64A Group MCU:

- Voltage detector
- Three-phase motor control timer function
- Real-time clock
- Pulse width modulator (PWM)
- Remote control signal receiver
- Multi-master I^2C-bus interface
- Consumer electronics control (CEC) function
- D/A converter

4.19 Differences in Development Tools

Table 4.40 lists Differences in Development Tools.

Table 4.40 Differences in Development Tools

Types of Tool	M16C/30P	M16C/64A
C compiler	M3T-NC30WA	M3T-NC30WA
Real-time OS	M3T-MR30	M3T-MR30
Emulator debugger	PC7501	E100 (R0E001000EMU00)
Emulation probe	M3062PT2-EPB	—
MCU unit	—	R0E530650MCU00
Compact emulator	M3062PT3-CPE	—
On-chip debugging emulator	E8 E8a (7-wire system)	E8a (single-wire system)

5. Reference Documents

Hardware Manual
M16C/30P Group Hardware Manual
M16C/64A Group Hardware Manual
(The latest version of these documents can be downloaded from the Renesas Technology website.)

Technical News/Technical Update
(The latest version of these documents can be downloaded from the Renesas Technology website.)

Website and Support

Renesas Technology Website
http://www.renesas.com/

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http://www.renesas.com/inquiry
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REVISION HISTORY	M16C/30P Group, M16C/64A Group Differences between M16C/30P and M16C/64A

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		Page	Summary
1.00	Sep 1, 2009	–	First edition issued

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