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M16C/29 Group, M16C/5LD Group

Differences between M16C/29 and M16C/5LD

1. Abstract

This following document describes differences between the M16C/29 80-pin package and the M16C/5LD 80-pin package Renesas microcomputers (MCUs). Refer to each device's hardware manual for details.

2. Introduction

The application examples in this document refer to the following MCUs:

- M16C/29 80-pin package
- M16C/5LD 80-pin package

Refer to the latest hardware manuals and technical updates when using this application note.

3. Differences

3.1 Differences in Functions

Table 3.1.1 and Table 3.1.2 list Differences in Functions.

Table 3.1.1 Differences in Functions (1/2) (1)

Item		M16C/29	M16C/5LD
Minimum Instruction Execution Time		50 ns (f(BCLK) = 20 MHz, VCC = 3.0 to 5.5 V) (Normal-ver./T-ver.) 100 ns (f(BCLK) = 10 MHz, VCC = 2.7 to 5.5 V) (Normal-ver.) 50 ns (f(BCLK) = 20 MHz, VCC = 4.2 to 5.5 V, -40°C to 105°C) (V-ver.) 62.5 ns (f(BCLK) = 16 MHz, VCC = 4.2 to 5.5 V, -40°C to 125°C) (V-ver.)	31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V) 40 ns (f(BCLK) = 25 MHz, VCC = 2.7 to 5.5 V)
Voltage Detector	Voltage detect circuits	2 circuits (Normal-ver.), No (T-ver./V-ver.)	2 circuits
	Power-on reset	No	Yes
Clock Generator		4 circuits Main clock (2), sub clock (2), on-chip oscillator, PLL frequency synthesizer	4 circuits Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator
CPU Clock after Reset		On-chip oscillator clock f2 (ROC) divided by 16	125 kHz on-chip oscillator clock (fOCO-S) divided by 8
Power Control	Slow read mode	No	Yes
	Low current consumption read mode	No	Yes
Power Supply Voltage		(Normal-ver.) VCC = 3.0 to 5.5 V (f(BCLK) = 20 MHz) VCC = 2.7 to 5.5 V (f(BCLK) = 10 MHz)	32 MHz / 3.0 to 5.5 V 25 MHz / 2.7 to 5.5 V
		(T-ver.) VCC = 3.0 to 5.5 V	
		(V-ver.) VCC = 4.2 to 5.5 V	
Current Consumption		18 mA (VCC = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 kHz on RAM) 3.0 μA (VCC = 5 V, f(XCIN) = 32 kHz, in wait mode) 0.8 μA (VCC = 5 V, in stop mode)	TBD
Watchdog Timer	Count source	CPU clock, on-chip oscillator	CPU clock, dedicated 125 kHz on-Chip oscillator for the watchdog timer
	Reset start function	No	Selectable from start and stop
	Refresh possible period	100% (can be refreshed constantly)	25%, 50%, 75%, 100% (selectable)
DMAC		2 channels Trigger sources: 23	4 channels Trigger sources: 42

Notes:
1. Refer to the hardware manual for electrical characteristics and more details.
2. These circuits contain a built-in feedback resistor.

Table 3.1.2 Differences in Functions (2/2) (1)

Item		M16C/29	M16C/5LD
Timers	Timer A, timer B count source	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32
	Timer A modes	Timer mode, event counter mode, one-shot timer mode, pulse width modulation mode (PWM mode)	Timer mode, event counter mode, one-shot timer mode, pulse width modulation mode (PWM mode), programmable output mode
	Task monitor timer	No	16 bits timer x 1 channel
	Real-time clock	No	Counts seconds, minutes, hours, and days of the week
Serial Interface	Number of channels	Clock synchronous/asynchronous x 3 channels Dedicated clock-synchronous x 2 channels	Clock synchronous/asynchronous x 5 channels
Multi-master I^2C-bus Interface	Slave address setting	1	3 (maximum)
CAN Module		16 slots	32 slots
A/D Converter		1 circuit (A/D circuit only)	2 circuits (A/D circuit, A/D1 circuit)
	Resolution	8-bit/10-bit (selectable)	10-bit only
	Sample and hold	Yes/No (selectable)	Yes
	Analog input pins	8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2)	A/D circuit: 8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2) A/D1 circuit: 4 pins (AN0 to AN3)
Flash Memory	Program/ erase power supply voltage	2.7 to 5.5 V (Normal-ver.) 3.0 to 5.5 V (T-ver.) 4.2 to 5.5 V (V-ver.)	2.7 to 5.5 V
	Program/ erase cycles	100 times (all space) or 1,000 times (blocks 0 to 5) 10,000 times (blocks A and B)	1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash)

Note:
1. Refer to the hardware manual for electrical characteristics and more details.

3.2 Pin Characteristics

Table 3.2.1 lists Differences in Pin Characteristics.

Table 3.2.1 Differences in Pin Characteristics

M16C/29	M16C/5LD	Changes from M16C/29
P9_3/CTX/AN2_4	P9_3/CTX0/AN2_4	Added: CTX0 Deleted: CTX
P9_2/TB2IN/CRX/AN3_2	P9_2/TB2IN/CRX0/AN3_2	Added: CRX0 Deleted: CRX
P7_0/TA0OUT/TXD2/SDA2/$\overline{\text{RTS1}}$/$\overline{\text{CTS1}}$ /$\overline{\text{CTS0}}$/CLKS1	P7_0/TA0OUT/TXD2/SDA2/$\overline{\text{RTS1}}$/$\overline{\text{CTS1}}$	Deleted: $\overline{\text{CTS0}}$/CLKS1
P6_4/$\overline{\text{RTS1}}$/$\overline{\text{CTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4 /$\overline{\text{RTS1}}$/$\overline{\text{CTS1}}$	Deleted: $\overline{\text{CTS0}}$/CLKS1
P3_3	P3_3/$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	Added: $\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$
P3_2/SOUT3	P3_2/TXD3	Added: TXD3 Deleted: SOUT3
P3_1/SIN3	P3_1/RXD3	Added: RXD3 Deleted: SIN3
P6_0/$\overline{\text{RTS0}}$/$\overline{\text{CTS0}}$	P6_0/RTCOUT/$\overline{\text{RTS0}}$/$\overline{\text{CTS0}}$	Added: RTCOUT
P9_7/SIN4/AN2_7	P9_7/RXD4/AN2_7	Added: RXD4 Deleted: SIN4
P9_6/SOUT4/AN2_6	P9_6/TXD4/AN2_6	Added: TXD4 Deleted: SOUT4

4. Detailed Comparison

4.1 Differences in Protection

Table 4.1.1 lists Differences in the Register Associated with Protection.

Table 4.1.1 Differences in the Register Associated with Protection

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PRCR	000Ah		0	Protect bit 0 Enable write access to registers CM0, CM1, CM2, ROCR, PLC0, PCLKR, and CCLKR	Protect bit 0 Enable write access to registers CM0, CM1, CM2, PLC0, and PCLKR
			2	Protect bit 2 Enable write access to registers PD9, PACR, S4C, and NDDR	Protect bit 2 Enable write access to registers PD9, U4MR, NDDR, and PACR
			3	Protect bit 3 Enable write access to registers VCR2 and D4INT	Protect bit 3 Enable write access to registers VCR2, VWCE, VD2LS, VW0C, and VW2C
			6	No register bit	Protect bit 6 Enable write access to PRG2C register

4.2 Differences in Resets

Table 4.2.1 lists Differences in Resets and Table 4.2.2 lists Differences in the Register Associated with Resets.

Table 4.2.1 Differences in Resets

Item	M16C/29	M16C/5LD
Types of resets	Hardware reset 1 Software reset Watchdog timer reset Oscillation stop detection reset Hardware reset 2 (brown-out detection reset) (1)	Hardware reset Software reset Watchdog timer reset Oscillation stop detection reset Voltage monitor 0 reset Voltage monitor 2 reset Power-on reset

Note:
1. T-ver. and V-ver. cannot be used.

Table 4.2.2 Differences in the Register Associated with Resets

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
RSTFR	—	0018h	1	—	Hardware reset detection flag 0: Not detected 1: Detected
			2		Software reset detection flag 0: Not detected 1: Detected
			3		Watchdog timer reset detection flag 0: Not detected 1: Detected
			5		Voltage monitor 2 reset detection flag 0: Not detected 1: Detected
			6		Oscillator stop detect reset detection flag 0: Not detected 1: Detected

4.3 Differences in Voltage Detector

Table 4.3.1 lists Differences in the Voltage Detector and Table 4.3.2 lists Differences in Registers Associated with the Voltage Detector.

Table 4.3.1 Differences in the Voltage Detector

Item	M16C/29	M16C/5LD
Voltage detection interrupt monitor level	Vdet4	Vdet2 (voltage detection circuit 2)
Voltage detection reset monitor level	Vdet3	• Vdet2 (voltage detection circuit 2) • Vdet0 (voltage detection circuit 0)
Sampling clock	CPU clock	fOCO-S

Refer to the electric characteristics in the hardware manual for detection voltage.

Table 4.3.2 Differences in Registers Associated with the Voltage Detector

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
VCR1	0019h		3	Low voltage monitor flag 0: VCC < Vdet4 1: VCC ≥ Vdet4	Low voltage monitor flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detector 2 circuit disabled
VCR2	001Ah		5	Reserved bit	Voltage detector 0 enable bit 0: Voltage detector 0 disabled 1: Voltage detector 0 enabled
			6	Reset level monitor bit 0: Disable reset level detection circuit 1: Enable reset level detection circuit	Reserved bit
			7	Low voltage monitor bit 0: Disable low voltage detection circuit 1: Enable low voltage detection circuit	Voltage detector 2 enable bit 0: Voltage detector 2 disabled 1: Voltage detector 2 enabled
VWCE	—	0026h	—	—	M16C/5LD only
VD2LS	—	0028h	—	—	M16C/5LD only
VW0C	—	002Ah	—	—	M16C/5LD only
VW2C	—	002Ch	—	—	M16C/5LD only
D4INT	001Fh	—	0	Low voltage detection interrupt enable bit 0: Disable 1: Enable	—
			1	Stop mode deactivation control bit 0: Disable (do not use the low voltage detection interrupt to exit stop mode) 1: Enable (use the low voltage detection interrupt to exit stop mode)	
			2	Voltage change detection flag 0: Not detected 1: Vdet4 passing detection	
			3	WDT overflow detect flag 0: Not detected 1: Detected	
			5 - 4	Sampling clock select bit 00: CPU clock divided by 8 01: CPU clock divided by 16 10: CPU clock divided by 32 11: CPU clock divided by 64	
OFS1	—	FFFFFh	6	—	Voltage detector 0 start bit 0: Voltage monitor 0 reset enabled after hardware reset. 1: Voltage monitor 0 reset disabled after hardware reset.

4.4 Differences in the Clock Generator

Table 4.4.1 lists Differences in the Clock Generator and Table 4.4.2 lists Differences in Registers Associated with Clock Generator.

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Table 4.4.1 Differences in the Clock Generator

Item	M16C/29	M16C/5LD
CPU clock after reset	On-chip oscillator clock f2 (ROC) divided by 16	125 kHz on-chip oscillator clock (fOCO-S) divided by 8
Peripheral clock (fC)	Supply constantly	Provided/Not provided (selectable) Selected by setting the PM25 bit in the PM2 register.
On-chip oscillator types and frequency	3 types On-chip oscillator frequency 1 (f1(ROC)): 1 MHz On-chip oscillator frequency 2 (f2(ROC)): 2 MHz On-chip oscillator frequency 3 (f3(ROC)): 16 MHz	2 types 125 kHz on-chip oscillator (fOCO-S): Approx. 125 kHz Dedicated 125 kHz on-chip oscillator for the watchdog timer (fWDT): Approx. 125 kHz
Clock frequency generated by PLL frequency synthesizer	10 to 20 MHz	10 to 32 MHz (VCC = 3.0 V to 5.5 V) 10 to 25 MHz (VCC = 2.7 V to 5.5 V)
Calculation formula for PLL clock frequency	f(XIN) x n	f(XIN) / m x n

n: Multiplication rate set by bits PLC02 to PLC00 in the PLC0 register
m: Division ratio set by bits PLC05 to PLC04 in the PLC0 register

Table 4.4.2 Differences in Registers Associated with Clock Generator

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
CM1	0007h		3	Reserved bits	XIN-XOUT feedback resistor select bit 0: Internal feedback resistor connected 1: Internal feedback resistor not connected
			4		125 kHz on-chip oscillator stop bit 0: 125 kHz on-chip oscillator oscillates 1: 125 kHz on-chip oscillator stops
PCLKR	025Eh	0012h	—	Difference in address	
PLC0	001Ch		2 - 0	PLL multiplying factor select bit 000: Do not set 001: Multiply by 2 010: Multiply by 4 011: 100: 101: 110: 111: Do not set	PLL multiplying factor select bit 000: Do not set 001: Multiply-by-2 010: Multiply-by-4 011: Multiply-by-6 100: Multiply-by-8 101: 110: 111: Do not set
			4	Reserved bit Set to 1.	Reference frequency counter set bit 00: No division 01: Divide-by-2 10: Divide-by-4 11: Do not set
			5	Reserved bit	
PM2	001Eh		0	Specifying wait when accessing SFR 0: 2 waits 1: 1 wait	Reserved bit Set to 1.
			2	WDT count source protective bit 0: CPU clock is used for the watchdog timer count source 1: On-chip oscillator clock is used for the watchdog timer count source	No register bit
			5	No register bit	Peripheral clock fC provide bit 0: fC disabled 1: fC enabled
ROCR	025Ch	—	—	M16C/29 only	—
CCLKR	025Fh	—	—	M16C/29 only	—

4.5 Differences in Power Control

Table 4.5.1 lists Differences in Power Control and Table 4.5.2 lists Difference in the Register Associated with Power Control.

Table 4.5.1 Differences in Power Control

Item	M16C/29	M16C/5LD
Slow read mode	No	Yes
Low current consumption read mode	No	Yes

Table 4.5.2 Difference in the Register Associated with Power Control

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
FMR2	—	0222h	—	—	M16C/5LD only

4.6 Difference in Processor Mode

Table 4.6.1 lists Difference in the Register Associated with Processor Mode.

Table 4.6.1 Difference in the Register Associated with Processor Mode

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PRG2C	—	0010h	—	—	M16C/5LD only

4.7 Differences in Programmable I/O Ports

Table 4.7.1 lists Differences in Registers Associated with Programmable I/O Ports.

Table 4.7.1 Differences in Registers Associated with Programmable I/O Ports

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
NDDR	033Eh	02FEh	—	Difference in address	
P17DDR	033Fh	02FFh	—	Difference in address	
PUR0	03FCh	0360h	—	Difference in address	
PUR1	03FDh	0361h	—	Difference in address	
PUR2	03FEh	0362h	—	Difference in address	
PCR	03FFh	0366h	—	Difference in address	
PACR	025Dh	0370h	—	Difference in address	

4.8 Differences in Interrupts

Table 4.8.1 to Table 4.8.2 list Differences in Interrupt Vectors, Table 4.8.3 lists Differences in SFRs Associated with Interrupts, and Table 4.8.4 Differences in Interrupt Source Select Registers.

Table 4.8.1 Differences in Interrupt Vectors (1/2)

Software Interrupt Number	Vector Address	M16C/29	M16C/5LD
0	+0 to +3 (0000h to 0003h)	BRK instruction	BRK instruction
1	+4 to +7 (0004h to 0007h)	CAN0 wake-up	— (Reserved)
2	+8 to +11 (0008h to 000Bh)	CAN0 receive completion	— (Reserved)
3	+12 to +15 (000Ch to 000Fh)	CAN0 transmit completion	— (Reserved)
4	+16 to +19 (0010h to 0013h)	$\overline{\text{INT3}}$	$\overline{\text{INT3}}$
5	+20 to +23 (0014h to 0017h)	IC/OC interrupt 0	— (Reserved)
6	+24 to +27 (0018h to 001Bh)	IC/OC interrupt 1, I^2C-bus interface	— (Reserved)
7	+28 to +31 (001Ch to 001Fh)	IC/OC base timer, SCL/SDA	— (Reserved)
8	+32 to +35 (0020h to 0023h)	SI/O4, $\overline{\text{INT5}}$	$\overline{\text{INT5}}$
9	+36 to +39 (0024h to 0027h)	SI/O3, $\overline{\text{INT4}}$	$\overline{\text{INT4}}$
10	+40 to +43 (0028h to 002Bh)	UART2 start/stop condition detection, bus collision detection	UART2 start/stop condition detection, bus collision detection, task monitor timer
11	+44 to +47 (002Ch to 002Fh)	DMA0	DMA0
12	+48 to +51 (0030h to 0033h)	DMA1	DMA1
13	+52 to +55 (0034h to 0037h)	CAN0 error	Key input interrupt, A/D1
14	+56 to +59 (0038h to 003Bh)	A/D converter, Key input interrupt	A/D
15	+60 to +63 (003Ch to 003Fh)	UART2 transmit, NACK2	UART2 transmit, NACK2
16	+64 to +67 (0040h to 0043h)	UART2 receive, ACK2	UART2 receive, ACK2
17	+68 to +71 (0044h to 0047h)	UART0 transmit	UART0 transmit
18	+72 to +75 (0048h to 004Bh)	UART0 receive	UART0 receive
19	+76 to +79 (004Ch to 004Fh)	UART1 transmit	UART1 transmit
20	+80 to +83 (0050h to 0053h)	UART1 receive	UART1 receive
21	+84 to +87 (0054h to 0057h)	Timer A0	Timer A0
22	+88 to +91 (0058h to 005Bh)	Timer A1	Timer A1
23	+92 to +95 (005Ch to 005Fh)	Timer A2	Timer A2
24	+96 to +99 (0060h to 0063h)	Timer A3	Timer A3
25	+100 to +103 (0064h to 0067h)	Timer A4	Timer A4
26	+104 to +107 (0068h to 006Bh)	Timer B0	Timer B0
27	+108 to +111 (006Ch to 006Fh)	Timer B1	Timer B1
28	+112 to +115 (0070h to 0073h)	Timer B2	Timer B2

Table 4.8.2 Differences in Interrupt Vectors (2/2)

Software Interrupt Number	Vector Address	M16C/29	M16C/5LD
29	+116 to +119 (0074h to 0077h)	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$
30	+120 to +123 (0078h to 007Bh)	$\overline{\text{INT1}}$	$\overline{\text{INT1}}$
31	+124 to +127 (007Ch to 007Fh)	$\overline{\text{INT2}}$	$\overline{\text{INT2}}$
32 to 40	+128 to +131 (0080h to 0083h) to +160 to +163 (00A0h to 00A3h)	Software interrupt	INT instruction interrupt
41	+164 to +167 (00A4h to 00A7h)		DMA2
42	+168 to +171 (00A8h to 00ABh)		DMA3
43	+172 to +175 (00ACh to 00AFh)		— (Reserved)
44	+176 to +179 (00B0h to 00B3h)		— (Reserved)
45	+180 to +183 (00B4h to 00B7h)		— (Reserved)
46	+184 to +187 (00B8h to 00BBh)		— (Reserved)
47	+188 to +191 (00BCh to 00BFh)		UART4 transmit, real-time clock compare
48	+192 to +195 (00C0h to 00C3h)		UART4 receive
49	+196 to +199 (00C4h to 00C7h)		CAN0 wake-up
50	+200 to +203 (00C8h to 00CBh)		UART3 transmit, CAN0 error
51	+204 to +207 (00CCh to 00CFh)		UART3 receive
52	+208 to +211 (00D0h to 00D3h)		Real-time clock cycle
53	+212 to +215 (00D4h to 00D7h)		CAN0 successful receive
54	+216 to +219 (00D8h to 00DBh)		CAN0 successful transmit
55	+220 to +223 (00DCh to 00DFh)		CAN0 receive FIFO
56	+224 to +227 (00E0h to 00E3h)		CAN0 transmit FIFO
57	+228 to +231 (00E4h to 00E7h)		IC/OC interrupt 0 (0 to 7)
58	+232 to +235 (00E8h to 00EBh)		IC/OC channel 0
59	+236 to +239 (00ECh to 00EFh)		IC/OC interrupt 1 (0 to 7), I^2C-bus interface interrupt
60	+240 to +243 (00F0h to 00F3h)		IC/OC channel 1, SCL/SDA interrupt
61	+244 to +247 (00F4h to 00F7h)		IC/OC channel 2
62	+248 to +251 (00F8h to 00FBh)		IC/OC channel 3
63	+252 to +255 (00FCh to 00FFh)		IC/OC base timer

Table 4.8.3 Differences in SFRs Associated with Interrupts

Symbol	Address		Differences	
	M16C/29	M16C/5LD	M16C/29	M16C/5LD
AIER	0009h	020Eh	Difference in address	
AIER2	—	020Fh	—	M16C/5LD only
RMAD0	0010h to 0012h	0210h to 0212h	Difference in address	
RMAD1	0014h to 0016h	0214h to 0216h	Difference in address	
RMAD2	—	0218h to 021Ah	—	M16C/5LD only
RMAD3	—	021Ch to 021Eh	—	M16C/5LD only
M16C/29: C01WKIC M16C/5LD: C0WIC	0041h	0071h	Difference in symbol and address	
M16C/29: C0RECIC M16C/5LD: C0RIC	0042h	0075h	Difference in symbol and address	
M16C/29: C0TRMIC M16C/5LD: C0TIC	0043h	0076h	Difference in symbol and address	
C0FRIC	—	0077h	—	M16C/5LD only
C0FTIC	—	0078h	—	M16C/5LD only
ICOC0IC	0045h	0079h	Difference in address	
ICOCH0IC	—	007Ah	—	M16C/5LD only
ICOC1IC, IICIC	0046h	007Bh	Difference in address	
BTIC	0047h	007Fh	Difference in address	
SCLDAIC	0047h	007Ch	Difference in address	
ICOCH1IC	—	007Ch	—	M16C/5LD only
ICOCH2IC	—	007Dh	—	M16C/5LD only
ICOCH3IC	—	007Eh	—	M16C/5LD only
S4IC	0048h	—	M16C/29 only	—
S4TIC	—	006Fh	—	M16C/5LD only
S4RIC	—	0070h	—	M16C/5LD only
S3IC	0049h	—	M16C/29 only	—
S3TIC	—	0072h	—	M16C/5LD only
S3RIC	—	0073h	—	M16C/5LD only
M16C/29: C01ERRIC M16C/5LD: C0EIC	004Dh	0072h	Difference in symbol and address	
KUPIC	004Eh	004Dh	Difference in address	
ADEIC	—	004Dh	—	M16C/5LD only
IFSR3A	—	0205h	—	M16C/5LD only
IFSR2A	035Eh	0206h	Difference in address and contents	
IFSR	035Fh	0207h	Difference in address and contents	
G1IR	0330h	02F0h	Difference in address	
G1IE0	0331h	02F1h	Difference in address	
G1IE1	0332h	02F2h	Difference in address	
NDDR	033Eh	02FEh	Difference in address	
TMOSIC	—	004Ah	—	M16C/5LD only
DM2IC	—	0069h	—	M16C/5LD only
DM3IC	—	006Ah	—	M16C/5LD only
RTCCIC	—	006Fh	—	M16C/5LD only
RTCTIC	—	0074h	—	M16C/5LD only
C0ICR	0216h to 0217h	—	M16C/29 only	—

Table 4.8.4 Differences in Interrupt Source Select Registers

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
IFSR3A	—	0205h	6	—	0: UART4 transmission 1: Real-time clock compare
IFSR2A	035Eh	0206h	0	Reserved bit	0: UART2 bus collision detection 1: Task monitor timer
			1	0: A/D conversion 1: Key input	0: Key input interrupt 1: A/D1 conversion interrupt
			2	0: CAN0 wake-up/error 1: Do not set	0: IC/OC interrupt 1 1: I^2C-bus interface
			3	No register bits	0: IC/OC channel 1 interrupt 1: SCL/SDA
			4		0: Reserved 1: CAN0 wake-up
			5		0: UART3 transmission 1: CAN0 error
			6	0: IC/OC base timer 1: SCL/SDA	Reserved bits
			7	0: IC/OC interrupt 1 1: I^2C-bus interface	
IFSR	035Fh	0207h	6	0: $\overline{SI/O3}$ 1: INT4	0: $\overline{Reserved}$ 1: INT4
			7	0: $\overline{SI/O4}$ 1: INT5	0: $\overline{Reserved}$ 1: INT5

4.9 Differences in the Watchdog Timer

Table 4.9.1 lists Differences in the Watchdog Timer and Table 4.9.2 lists Differences in Registers Associated with the Watchdog Timer.

Table 4.9.1 Differences in the Watchdog Timer

Item	M16C/29	M16C/5LD
Count source in count source protect mode	On-chip oscillator clock	Watchdog timer with dedicated 125 kHz on-chip oscillator
Count source protect mode enable setting	Set the PM22 bit to 1.	Set the CSPRO bit to 1. (1)
Watchdog timer cycle in count source protect mode	$\frac{\text{Watchdog timer count (32768)}}{\text{On-chip oscillator clock}}$ On-chip oscillator clock can be set in the ROCR register.	$\frac{\text{Watchdog timer count (m)}}{\text{fWDT (Approx. 125 kHz)}}$ m: Value set by bits WDTUFS1 to WDTUFS0 in the OFS2 address
Set value can be for watchdog timer	7FFFh	03FFh, 0FFFh, 1FFFh, 3FFFh
A value of watchdog timer read in the WDC register	Watchdog timer high-order bits	•Bits b10 to b5 can be read when the count source protect mode is disabled. •When the count source protect mode is enabled, while bits WDTUFS1 and WDTUFS0 in the OFS2 address are: 00b (03FFh), bits b5 to b0 can be read 01b (0FFFh), bits b8 to b3 can be read 10b (1FFFh), bits b9 to b4 can be read 11b (3FFFh), bits b10 to b5 can be read
Watchdog timer counter initialization	The watchdog timer counter is initialized and starts counting by writing to the WDTS register.	Write 00h, and then FFh to the WDTR register
Count start conditions		• Count automatically starts after reset by setting the WDTON bit in the OFS1 address to 0. • Count starts by writing to the WDTS register.
Refresh possible period	100% (can be refreshed constantly)	25%, 50%, 75%, 100% (selectable)
Watchdog timer detect flag	The D43 bit in the D4INT register WDT overflow detect flag 0: Not detected 1: Detected	The VW2C3 bit in the VW2C register WDT detection flag 0: Not detected 1: Watchdog timer underflow detected

Note:
1. When the CSPROINI bit in the OFS1 address is 0, the value after reset becomes 1.

Table 4.9.2 Differences in Registers Associated with the Watchdog Timer

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
WDTS	000Eh	037Eh	—	Difference in address	
				The watchdog timer is initialized and starts counting after a write instruction to this register. The watchdog timer value is always initialized to 7FFFh regardless of the value written.	The watchdog timer starts counting by writing to this register.
WDC	000Fh	037Fh	—	Difference in address	
			0	Watchdog timer high-order bits	Bits b10 to b5 can be read when the count source protect mode is disabled. When the count source protect mode is enabled, while bits WDTUFS1 and WDTUFS0 in the OFS2 address are: 00b (03FFh), bits b5 to b0 can be read 01b (0FFFh), bits b8 to b3 can be read 10b (1FFFh), bits b9 to b4 can be read 11b (3FFFh), bits b10 to b5 can be read
			1		
			2		
			3		
			4		
			5	Reserved bit	
VW2C	—	002Ch	3	—	WDT detection flag 0: Not detected 1: Watchdog timer underflow detected
CSPR	—	037Ch	7	—	Count source protection mode select bit 0: Count source protect mode disabled 1: Count source protect mode enabled
WDTR	—	037Dh	7 - 0	—	The watchdog timer counter is refreshed by writing 00h and then FFh to this register. The default value is indicated by bits WDTUFS1 and WDTUFS0 in the OFS2 address.
OFS2	—	FFFDBh	1 - 0	—	Watchdog timer reset value setting bit 00: 03FFh 01: 0FFFh 10: 1FFFh 11: 3FFFh
			3 - 2		Watchdog timer refresh duty cycle setting bit 00: 25% 01: 50% 10: 75% 11: 100%
			7 - 4		Reserved bits Set to 1
OFS1	—	FFFFFh	0	—	Watchdog timer start select bit 0: Watchdog timer starts automatically after reset. 1: Watchdog timer is in a stopped state after reset.

4.10 Differences in DMAC

Table 4.10.1 lists Differences in DMAC and Table 4.10.2 to Table 4.10.5 list Differences in DMAi Request Sources (i = 0 to 4), and Table 4.10.6 lists Differences in Registers Associated with DMAC.

Table 4.10.1 Differences in DMAC

Item	M16C/29	M16C/5LD
Number of channels	2 channels	4 channels
Trigger sources	23	42

Table 4.10.2 Differences in DMA0 Request Sources

DSEL4 to DSEL0	M16C/29		M16C/5LD	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b	Falling edge of $\overline{\text{INT0}}$ pin	IC/OC base timer	Falling edge of $\overline{\text{INT0}}$ pin	IC/OC base timer
00001b	Software trigger	—	Software trigger	A/D1 converter
00010b	Timer A0	IC/OC channel 0	Timer A0	IC/OC channel 0
00011b	Timer A1	IC/OC channel 1	Timer A1	IC/OC channel 1
00100b	Timer A2	—	Timer A2	—
00101b	Timer A3	—	Timer A3	—
00110b	Timer A4	Both edges of $\overline{\text{INT0}}$ pin	Timer A4	Both edges of $\overline{\text{INT0}}$ pin
00111b	Timer B0	—	Timer B0	—
01000b	Timer B1	—	Timer B1	—
01001b	Timer B2	—	Timer B2	—
01010b	UART0 transmit	IC/OC channel 2	UART0 transmit	IC/OC channel 2
01011b	UART0 receive	IC/OC channel 3	UART0 receive	IC/OC channel 3
01100b	UART2 transmit	IC/OC channel 4	UART2 transmit	IC/OC channel 4
01101b	UART2 receive	IC/OC channel 5	UART2 receive	IC/OC channel 5
01110b	A/D converter	IC/OC channel 6	A/D converter	IC/OC channel 6
01111b	UART1 transmit	IC/OC channel 7	UART1 transmit	IC/OC channel 7
10000b			UART1 receive	Falling edge of $\overline{\text{INT4}}$ pin
10001b			—	Both edges of $\overline{\text{INT4}}$ pin
10010b			—	—
10011b			UART4 transmit	—
10100b			UART4 receive	—
10101b			UART3 transmit	—
10110b			UART3 receive	—

Table 4.10.3 Differences in DMA1 Request Sources

DSEL4 to DSEL0	M16C/29		M16C/5LD	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b	Falling edge of $\overline{\text{INT1}}$ pin	IC/OC base timer	Falling edge of $\overline{\text{INT1}}$ pin	IC/OC base timer
00001b	Software trigger	—	Software trigger	A/D1 converter
00010b	Timer A0	IC/OC channel 0	Timer A0	IC/OC channel 0
00011b	Timer A1	IC/OC channel 1	Timer A1	IC/OC channel 1
00100b	Timer A2	—	Timer A2	—
00101b	Timer A3	SI/O3	Timer A3	—
00110b	Timer A4	SI/O4	Timer A4	—
00111b	Timer B0	Both edges of $\overline{\text{INT1}}$ pin	Timer B0	Both edges of $\overline{\text{INT1}}$ pin
01000b	Timer B1	—	Timer B1	—
01001b	Timer B2	—	Timer B2	—
01010b	UART0 transmit	IC/OC channel 2	UART0 transmit	IC/OC channel 2
01011b	UART0 receive	IC/OC channel 3	UART0 receive	IC/OC channel 3
01100b	UART2 transmit	IC/OC channel 4	UART2 transmit	IC/OC channel 4
01101b	UART2 receive/ACK2	IC/OC channel 5	UART2 receive/ACK2	IC/OC channel 5
01110b	A/D conversion	IC/OC channel 6	A/D conversion	IC/OC channel 6
01111b	UART1 receive	IC/OC channel 7	UART1 receive	IC/OC channel 7
10000b			UART1 transmit	Falling edge of $\overline{\text{INT5}}$ pin
10001b			—	Both edges of $\overline{\text{INT5}}$ pin
10010b			—	—
10011b			UART4 transmit	—
10100b			UART4 receive	—
10101b			UART3 transmit	—
10110b			UART3 receive	—

Table 4.10.4 Differences in DMA2 Request Sources

DSEL4 to DSEL0	M16C/29		M16C/5LD	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b			Falling edge of $\overline{\text{INT2}}$ pin	IC/OC base timer
00001b			Software trigger	A/D1 conversion
00010b			Timer A0	IC/OC channel 0
00011b			Timer A1	IC/OC channel 1
00100b			Timer A2	—
00101b			Timer A3	—
00110b			Timer A4	Both edges of $\overline{\text{INT2}}$ pin
00111b			Timer B0	—
01000b			Timer B1	—
01001b			Timer B2	—
01010b			UART0 transmit	IC/OC channel 2
01011b			UART0 receive	IC/OC channel 3
01100b			UART2 transmit	IC/OC channel 4
01101b			UART2 receive	IC/OC channel 5
01110b			A/D conversion	IC/OC channel 6
01111b			UART1 transmit	IC/OC channel 7
10000b			UART1 receive	—
10001b			—	—
10010b			—	—
10011b			UART4 transmit	—
10100b			UART4 receive	—
10101b			UART3 transmit	—
10110b			UART3 receive	—

Table 4.10.5 Differences in DMA3 Request Sources

DSEL4 to DSEL0	M16C/29		M16C/5LD	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b			Falling edge of $\overline{\text{INT3}}$ pin	IC/OC base timer
00001b			Software trigger	A/D1 conversion
00010b			Timer A0	IC/OC channel 0
00011b			Timer A1	IC/OC channel 1
00100b			Timer A2	—
00101b			Timer A3	—
00110b			Timer A4	—
00111b			Timer B0	Both edges of $\overline{\text{INT3}}$ pin
01000b			Timer B1	—
01001b			Timer B2	—
01010b			UART0 transmit	IC/OC channel 2
01011b			UART0 receive	IC/OC channel 3
01100b			UART2 transmit	IC/OC channel 4
01101b			UART2 receive/ACK2	IC/OC channel 5
01110b			A/D conversion	IC/OC channel 6
01111b			UART1 receive	IC/OC channel 7
10000b			UART1 transmit	—
10001b			—	—
10010b			—	—
10011b			UART4 transmit	—
10100b			UART4 receive	—
10101b			UART3 transmit	—
10110b			UART3 receive	—

Table 4.10.6 Differences in Registers Associated with DMAC

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
SAR0	0020h 0021h 0022h	0180h 0181h 0182h	—	Difference in address	
DAR0	0024h 0025h 0026h	0184h 0185h 0186h	—	Difference in address	
TCR0	0028h 0029h	0188h 0189h	—	Difference in address	
DM0CON	002Ch	018Ch	—	Difference in address	
SAR1	0030h 0031h 0032h	0190h 0191h 0192h	—	Difference in address	
DAR1	0034h 0035h 0036h	0194h 0195h 0196h	—	Difference in address	
TCR1	0038h 0039h	0198h 0199h	—	Difference in address	
DM1CON	003Ch	019Ch	—	Difference in address	
SAR2	—	01A0h 01A1h 01A2h	—	—	M16C/5LD only
DAR2	—	01A4h 01A5h 01A6h	—	—	M16C/5LD only
TCR2	—	01A8h 01A9h	—	—	M16C/5LD only
DM2CON	—	01ACh	—	—	M16C/5LD only
SAR3	—	01B0h 01B1h 01B2h	—	—	M16C/5LD only
DAR3	—	01B4h 01B5h 01B6h	—	—	M16C/5LD only
TCR3	—	01B8h 01B9h	—	—	M16C/5LD only
DM3CON	—	01BCh	—	—	M16C/5LD only
DM2SL	—	0390h	—	—	M16C/5LD only Refer to Table 4.10.4
DM3SL	—	0392h	—	—	M16C/5LD only Refer to Table 4.10.5
DM0SL	03B8h	0398h	—	Difference in address	
				Refer to Table 4.10.2	Refer to Table 4.10.2
DM1SL	03BAh	039Ah	—	Difference in address	
				Refer to Table 4.10.3	Refer to Table 4.10.3

4.11 Differences in Timer A

Table 4.11.1 lists Differences in Timer A, and Table 4.11.2 to Table 4.11.4 list Differences in Registers Associated with Timer A.

Table 4.11.1 Differences in Timer A

Item	M16C/29	M16C/5LD
Count source	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32
Output polarity inverse function	No	Yes
Programmable output mode	No	Yes
Count direction (up/down) selected by the TAiOUT pin (i = 0 to 4)	Yes	No

Table 4.11.2 Differences in Registers Associated with Timer A (1/3)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
TABSR	0380h	0320h	—	Difference in address	
CPSRF	0381h	0015h	—	Difference in address	
ONSF	0382h	0322h	—	Difference in address	
TRGSR	0383h	0323h	—	Difference in address	
UDF	0384h	0324h	—	Difference in address	
TA0MR	0396h	0336h	4	Event counter mode (when not using two-phase pulse signal processing)	
TA1MR	0397h	0337h		Up/down switching cause select bit 0: UDF register 1: Input signal to TAiOUT pin (i = 0 to 4)	Set to 0 in event counter mode.
TA2MR	0398h	0338h			
TA3MR	0399h	0339h			
TA4MR	039Ah	033Ah			

Table 4.11.3 Differences in Registers Associated with Timer A (2/3)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PCLKR	025Eh	0012h	—	Difference in address	
TACS0	—	01D0h	2 - 0	—	TA0 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			3		TA0 count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4		TA1 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			7		TA1 count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TACS1	—	01D1h	2 - 0	—	TA2 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			3		TA2 count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4		TA3 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			7		TA3 count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled

Table 4.11.4 Differences in Registers Associated with Timer A (3/3)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
TACS2	—	01D2h	2 - 0	—	TA4 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			3		TA4 count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
PWMFS	—	01D4h	1	—	Timer A1 programmable output mode select bit 0: PWM mode 16-bit PWM 1: Programmable output mode
			2		Timer A2 programmable output mode select bit 0: PWM mode 16-bit PWM 1: Programmable output mode
			4		Timer A4 programmable output mode select bit 0: PWM mode 16-bit PWM 1: Programmable output mode
TAPOFS	—	01D5h	0	—	TA0OUT output polar control bit 0: Output waveform high-level active 1: Output waveform low-level active (output reversed)
			1		TA1OUT output polar control bit 0: Output waveform high-level active 1: Output waveform low-level active (output reversed)
			2		TA2OUT output polar control bit 0: Output waveform high-level active 1: Output waveform low-level active (output reversed)
			3		TA3OUT output polar control bit 0: Output waveform high-level active 1: Output waveform low-level active (output reversed)
			4		TA4OUT output polar control bit 0: Output waveform high-level active 1: Output waveform low-level active (output reversed)
TAOW	—	01D8h	1	—	Timer A1 output waveform change enable bit 0: Change disabled 1: Change enabled
			2		Timer A2 output waveform change enable bit 0: Change disabled 1: Change enabled
			4		Timer A4 output waveform change enable bit 0: Change disabled 1: Change enabled
TA11	—	0302h to 0303h	15 - 0	—	With n being a set value of TAi1 register, m being a set value of TAi register, high-level duration: m/fj low-level duration: n/fj fj: Count source frequency
TA21	—	0304h to 0305h			
TA41	—	0306h to 0307h			

4.12 Differences in Timer B

Table 4.12.1 lists Differences in Timer B and Table 4.12.2 to Table 4.12.3 list Differences in Registers Associated with Timer B.

Table 4.12.1 Differences in Timer B

Item	M16C/29	M16C/5LD
Count sources	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32
Operating modes	Timer mode, event counter mode, pulse period/pulse width measurement mode, A/D trigger mode	Timer mode, event counter mode, pulse period/pulse width measurement mode
Read from timer register in pulse period/ pulse width measurement modes	Contents of the reload register (measurement result) can be read by reading the TBi register (i = 0 to 2)	When bits PPWFS12 to PPWFS10 in the PPWFS1 register are 0: • Contents of the reload register (measurement result) can be read by reading the TBi register When bits PPWFS12 to PPWFS10 in the PPWFS1 register are 1: • Contents of the counter (counter value) can be read by reading the TBi register • Contents of the reload register (measurement result) can be read by reading the TBi1 register
Write to timer register in pulse period/pulse width measurement modes	Value written to the TBi register is written to neither the reload register nor the counter	When not counting Value written to the TBi register is written to both reload register and counter When counting Value written to the TBi register is written to only reload register (transferred to counter when reloaded next)

Table 4.12.2 Differences in Registers Associated with Timer B (1/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PCLKR	025Eh	0012h	—	Difference in address	
TB0MR TB1MR TB2MR	039Bh 039Ch 039Dh	033Bh 033Ch 033Dh	—	Difference in address	
			1 - 0	Operation mode select bit 00: Timer mode or A/D trigger mode	Operation mode select bit 00: Timer mode
			3 - 2	No effect in timer mode Can be set to 0 or 1.	Set to 0 in timer mode.
			4	TB0MR register Set to 0 in timer mode. TB1MR, TB2MR registers No register bit	No register bit
TB0	0390h to 0391h	0330h to 0331h	—	Difference in address	
			15 - 0	Pulse period/pulse width measurement mode	
TB1	0392h to 0393h	0332h to 0333h		Measures a pulse period or width	Set an initial value. Measures a pulse period or width. Read the counter value while counting is in progress.
TB2	0394h to 0395h	0334h to 0335h		A/D trigger mode	
				Divide the count source by n + 1 where n = set value and cause the timer stop	No
TABSR	0380h	0320h	—	Difference in address	
CPSRF	0381h	0015h	—	Difference in address	
TB2SC	039Eh	033Eh	—	Difference in address	
TB01	—	01C0h to 01C1h	15 - 0	—	Pulse period/pulse width measurement mode Measures a pulse period or width
TB11	—	01C2h to 01C3h		—	
TB21	—	01C4h to 01C5h		—	

Table 4.12.3 Differences in Registers Associated with Timer B (2/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PPWFS1	—	01C6h	0	—	Timer B0 pulse period/pulse width measurement mode function select bit 0: Measurement result is stored in the TB0 register. The TB01 register is not used 1: The counter value is read in the TB0 register. Measurement result is stored in the TB01 register
			1		Timer B1 pulse period/pulse width measurement mode function select bit 0: Measurement result is stored in the TB1 register. The TB11 register is not used 1: The counter value is read in the TB1 register. Measurement result is stored in the TB11 register
			2		Timer B2 pulse period/pulse width measurement mode function select bit 0: Measurement result is stored in the TB2 register. The TB21 register is not used 1: The counter value is read in the TB2 register. Measurement result is stored in the TB21 register
TBCS0	—	01C8h	2 - 0	—	TB0 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			3		TB0 count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4		TB1 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			7		TB1 count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TBCS1	—	01D9h	2 - 0	—	TB2 count source select bit 000: f1TIMAB or f2TIMAB 001: f8TIMAB 010: f32TIMAB 011: f64TIMAB 100: Do not set 101: fOCO-S 110: fC32 111: Do not set
			3		TB2 count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled

4.13 Differences in Three-Phase Motor Control Timer

Table 4.13.1 lists Difference in the Three-Phase Motor Control Timer, and Table 4.13.2 lists Differences in Registers Associated with the Three-Phase Motor Control Timer.

Table 4.13.1 Difference in the Three-Phase Motor Control Timer

Item	M16C/29	M16C/5LD
Count source	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fC32

Table 4.13.2 Differences in Registers Associated with the Three-Phase Motor Control Timer

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
DTT	034Ch	030Ch	—	Difference in address	
ICTB2	034Dh	030Dh	—	Difference in address	
IDB0	034Ah	030Ah	—	Difference in address	
IDB1	034Bh	030Bh	—	Difference in address	
INVC0	0348h	0308h	—	Difference in address	
INVC1	0349h	0309h	—	Difference in address	
TA1	0388h to 0389h	0328h to 0329h	—	Difference in address	
TA2	038Ah to 038Bh	032Ah to 032Bh	—	Difference in address	
TA4	038Eh to 038Fh	032Eh to 032Fh	—	Difference in address	
TA11	0342h to 0343h	0302h to 0303h	—	Difference in address	
TA21	0344h to o345h	0304h to 0305h	—	Difference in address	
TA41	0346h to 0347h	0306h to 0307h	—	Difference in address	
TB2SC	039Eh	033Eh	—	Difference in address	
TB2	0394h to 0395h	0334h to 0335h	—	Difference in address	
TRGSR	0383h	0323h	—	Difference in address	
TABSR	0380h	0320h	—	Difference in address	
TA1MR	0397h	0337h	—	Difference in address	
TA2MR	0398h	0338h	—	Difference in address	
TA4MR	039Ah	033Ah	—	Difference in address	
TB2MR	039Dh	033Dh	—	Difference in address	
PDRF	034Eh	030Eh	—	Difference in address	
PFCR	0358h	0318h	—	Difference in address	
TPRC	025Ah	01DAh	—	Difference in address	

4.14 Differences in Timer S

Table 4.14.1 lists Differences in Timer S and Table 4.14.2 to Table 4.14.3 list Differences in Registers Associated with Timer S.

Table 4.14.1 Differences in Timer S

Item	M16C/29	M16C/5LD
When the base timer is operating: Read from timer	The value of base timer plus one can be read by reading the G1BT register.	The actual base timer value can be read by reading the G1BT register.
When the base timer is operating: Write to timer	The counter starts counting from the value written.	The value written is synchronized with the base timer count source (fBT1), and reflected in the base timer. Count continues from the value written.
Clearing the G1IR register	Write a 0, then each bit becomes 0. Write to 0 (no interrupt request) by using AND, or BCLR instruction.	The G1IRi bit (i = 0 to 7) becomes 1 (interrupt requested) when an interrupt request is generated. Use AND or BCLR instruction to set it to 0 (interrupt not requested) after one fBT1 clock cycle or more.
Compare match output function when generating a waveform	No	Yes
Output disable function when generating a waveform	No	Yes

Table 4.14.2 Differences in Registers Associated with Timer S (1/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
G1BT	0320h to 0321h	02E1h to 02E0h	—	Difference in address	
			15-0	When the base timer is counting: When read, the value of base timer plus 1 can be read.	When the base timer is counting: When read, the actual base timer value is returned.
G1BCR0	0322h	02E2h	—	Difference in address	
G1BCR1	0323h	02E3h	—	Difference in address	
G1BTRR	0328h to 0329h	02E8h to 02E9h	—	Difference in address	
G1DV	032Ah	02EAh	—	Difference in address	

Table 4.14.3 Differences in Registers Associated with Timer S (2/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
G1TMCR0	0318h	02D8h	—	Difference in address	
G1TMCR1	0319h	02D9h	—	Difference in address	
G1TMCR2	031Ah	02DAh	—	Difference in address	
G1TMCR3	031Bh	02DBh	—	Difference in address	
G1TMCR4	031Ch	02DCh	—	Difference in address	
G1TMCR5	031Dh	02DDh	—	Difference in address	
G1TMCR6	031Eh	02DEh	—	Difference in address	
G1TMCR7	031Fh	02DFh	—	Difference in address	
G1TPR6	0324h	02E4h	—	Difference in address	
G1TPR7	0325h	02E5h	—	Difference in address	
G1TM0	0300h to 0301h	02C0h to 02C1h	—	Difference in address	
G1TM1	0302h to 0303h	02C2h to 02C3h	—	Difference in address	
G1TM2	0304h to 0305h	02C4h to 02C5h	—	Difference in address	
G1TM3	0306h to 0307h	02C6h to 02C7h	—	Difference in address	
G1TM4	0308h to 0309h	02C8h to 02C9h	—	Difference in address	
G1TM5	030Ah to 030Bh	02CAh to 02CBh	—	Difference in address	
G1TM6	030Ch to 030Dh	02CCh to 02CDh	—	Difference in address	
G1TM7	030Eh to 030Fh	02CEh to 02CFh	—	Difference in address	
G1POCR0	0310h	02D0h	—	Difference in address	
G1POCR1	0311h	02D1h	—	Difference in address	
G1POCR2	0312h	02D2h	—	Difference in address	
G1POCR3	0313h	02D3h	—	Difference in address	
G1POCR4	0314h	02D4h	—	Difference in address	
G1POCR5	0315h	02D5h	—	Difference in address	
G1POCR6	0316h	02D6h	—	Difference in address	
G1POCR7	0317h	02D7h	—	Difference in address	
G1PO0	0300h to 0301h	02C0h to 02C1h	—	Difference in address	
G1PO1	0302h to 0303h	02C2h to 02C3h	—	Difference in address	
G1PO2	0304h to 0305h	02C4h to 02C5h	—	Difference in address	
G1PO3	0306h to 0307h	02C6h to 02C7h	—	Difference in address	
G1PO4	0308h to 0309h	02C8h to 02C9h	—	Difference in address	
G1PO5	030Ah to 030Bh	02CAh to 02CBh	—	Difference in address	
G1PO6	030Ch to 030Dh	02CCh to 02CDh	—	Difference in address	
G1PO7	030Eh to 030Fh	02CEh to 02CFh	—	Difference in address	
G1FE	0326h	02E6h	—	Difference in address	
G1FS	0327h	02E7h	—	Difference in address	
G1IR	0330h	02F0h	—	Difference in address	
G1IE0	0331h	02F1h	—	Difference in address	
G1IE1	0332h	02F2h	—	Difference in address	
G1OER	—	02ECh	—	—	M16C/5LD only
G1IOR0	—	02EEh	—	—	M16C/5LD only
G1IOR1	—	02EFh	—	—	M16C/5LD only

4.15 Differences in Serial Interface

Table 4.15.1 lists Differences in Serial Interface, and Table 4.15.2 to Table 4.15.3 list Differences in Registers Associated with Serial Interface.

Table 4.15.1 Differences in Serial Interface

Item	M16C/29	M16C/5LD
Number of channels	Clock synchronous/asynchronous x 3 Dedicated clock-synchronous x 2	Clock synchronous/asynchronous x 5
Serial data logic invert function	1 channel (UART2)	5 channels (UART0 to UART4)
Parity error signal output	1 channel (UART2)	5 channels (UART0 to UART4)
Transfer clock output from multiple pins selection	1 channel (UART1)	No
$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ separate function	1 channel (UART0)	No
TXD and RXD I/O polarity inverse function	1 channel (UART2)	5 channels (UART0 to UART4)

Table 4.15.2 Differences in Registers Associated with Serial Interface (1/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
PACR	025Dh	0370h	—	Difference in address	
U0MR	03A0h	0248h	—	Difference in address	
			7	Reserved bit	TXD, RXD I/O polarity inverse bit 0: No reverse 1: Reverse
U0BRG	03A1h	0249h	—	Difference in address	
U0TB	03A2h 03A3h	024Ah 024Bh	—	Difference in address	
U0C0	03A4h	024Ch	—	Difference in address	
U0C1	03A5h	024Dh	—	Difference in address	
			4	No register bits	UART0 transmit interrupt source select bit 0: U0TB register empty (TI = 1) 1: Transmit completed (TXEPT = 1)
			5		UART0 continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			6		Data logic select bit 0: No reverse 1: Reverse
			7		Error signal output enable bit 0: Output disabled 1: Output enabled
U0RB	03A6h 03A7h	024Eh 024Fh	—	Difference in address	
U1MR	03A8h	0258h	—	Difference in address	
			7	Reserved bit	TXD, RXD I/O polarity inverse bit 0: No reverse 1: Reverse

Table 4.15.3 Differences in Registers Associated with Serial Interface (2/2)

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
U1BRG	03A9h	0259h	—	Difference in address	
U1TB	03AAh 03ABh	025Ah 025Bh	—	Difference in address	
U1C0	03ACh	025Ch	—	Difference in address	
U1C1	03ADh	025Dh	—	Difference in address	
			4	No register bits	UART1 transmit interrupt source select bit 0: U1TB register empty (TI = 1) 1: Transmit completed (TXEPT = 1)
			5		UART1 continuous receive mode enable bit 0: Continuous receive mode disabled 1: Continuous receive mode enabled
			6		Data logic select bit 0: No reverse 1: Reverse
			7		Error signal output enable bit 0: Output disabled 1: Output enabled
U1RB	03AEh 03AFh	025Eh 025Fh	—	Difference in address	
U2SMR4	0374h	0264h	—	Difference in address	
U2SMR3	0375h	0265h	—	Difference in address	
U2SMR2	0376h	0266h	—	Difference in address	
U2SMR	0377h	0267h	—	Difference in address	
U2MR	0378h	0268h	—	Difference in address	
U2BRG	0379h	0269h	—	Difference in address	
U2TB	037Ah 037Bh	026Ah 026Bh	—	Difference in address	
U2C0	037Ch	026Ch	—	Difference in address	
U2C1	037Dh	026Dh	—	Difference in address	
U2RB	037Eh 037Fh	026Eh 026Fh	—	Difference in address	
UCON	03B0h	—	—	M16C/29 only	—
U3MR	—	02A8h	—	—	M16C/5LD only
U3BGR	—	02A9h	—	—	M16C/5LD only
U3TB	—	02AAh 02ABh	—	—	M16C/5LD only
U3C0	—	02ACh	—	—	M16C/5LD only
U3C1	—	02ADh	—	—	M16C/5LD only
U3RB	—	02AEh 02AFh	—	—	M16C/5LD only
U4MR	—	0298h	—	—	M16C/5LD only
U4BRG	—	0299h	—	—	M16C/5LD only
U4TB	—	029Ah 029Bh	—	—	M16C/5LD only
U4C0	—	029Ch	—	—	M16C/5LD only
U4C1	—	029Dh	—	—	M16C/5LD only
U4RB	—	029Eh 029Fh	—	—	M16C/5LD only

4.16 Differences in the Multi-Master I²C-bus Interface

Table 4.16.1 lists Differences in the Multi-Master I²C-bus Interface, and Table 4.16.2 lists Differences in Registers Associated with Multi-Master I²C-bus Interface.

Table 4.16.1 Differences in the Multi-Master I²C-bus Interface

Item	M16C/29	M16C/5LD
Slave address setting	1	3 (maximum)
SDA/port function switch SCL/port function switch	Yes	No

Table 4.16.2 Differences in Registers Associated with the Multi-Master I²C-bus Interface

Symbol	Address		Bits	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
S0D0	02E2h	02B2h	—	Difference in address	
S0D1	—	02BAh	—	—	M16C/5LD only
S0D2	—	02BBh	—	—	M16C/5LD only
S00	02E0h	02B0h	—	Difference in address	
S20	02E4h	02B4h	—	Difference in address	
S1D0	02E3h	02B3h	—	Difference in address	
S10	02E8h	02B8h	—	Difference in address	
S3D0	02E6h	02B6h	—	Difference in address	
			2	SDA/port function switch bit 0: SDA I/O pin 1: Port output pin	Reserved bits
			3	SCL/port function switch bit 0: SCL I/O pin 1: Port output pin	
S4D0	02E7h	02B7h	—	Difference in address	
			6	Reserved bit	Slave address compare bit 0: S0D0 register only 1: Registers S0D0 to S0D2
S2D0	02E5h	02B5h	—	Difference in address	
S11	—	02B9h	—	—	M16C/5LD only

4.17 Differences in CAN Module

Table 4.17.1 lists Differences in the CAN Module, and Table 4.17.2 to Table 4.17.9 list Differences in Registers Associated with CAN Module

Table 4.17.1 Differences in the CAN Module

Item	M16C/29	M16C/5LD
Message boxes	16 mailboxes	32 mailboxes
Mailbox modes	No	• Normal mailbox mode • FIFO mailbox mode
Acceptance filtering	3 acceptance masks	8 acceptance masks (Masks can be individually enabled or disabled)
Interrupt sources	4 types: • Reception complete • Transmission complete • Error • Wake-up	6 types: • Reception complete interrupt • Transmission complete interrupt • Receive FIFO interrupt • Transmit FIFO interrupt • Error interrupt • Wake-up interrupt
Clock select function	Yes	No
Loop back function	Yes	No
Basic CAN mode	Yes	No
Interface sleep function	Yes	No
Message order select function	Yes (selectable from word access and byte access)	No (byte access only)
Remote frame auto response function	Yes	No
Number of sampling times selectable	Yes	No
Selectable ID priority transmit mode or mailbox number priority transmit mode	No	Yes
FIFO transmit/receive mode	No	Yes
Transmit/receive ID format select	No	Yes
One-shot transmission/ reception function	No	Yes
Mailbox number search function	No	Yes
Channel search support function	No	Yes
Bus-off recovery mode selectable	No	Yes
Halt mode (communication stop mode)	No	Yes
Self-diagnosis mode	No	Yes
PLL bypass clock mode	No	Yes

Table 4.17.2 Differences in Registers Associated with the CAN Module (1/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
29: CCLKR 5LD: C0CLKR	025Fh	D7C7h	0	CAN0 clock select bits 000: No division 001: Divide-by-2 010: Divide-by-4 011: Divide-by-8 100: Divide-by-16 Do not set to values not listed above	CAN clock source select bit 0: BCLK 1: Main clock
			1		Reserved bit
			2		No register bit
			3	CAN0 CPU interface sleep bit 0: CAN0 CPU interface operation 1: CAN0 CPU interface in sleep	Reserved bit
C0CTLR	0210h 0211h	D7C0h D7C1h	0	CAN module reset bit 0: Operation mode 1: Reset/initialization mode	CAN operating mode select bit 00: CAN operation mode 01: CAN reset mode 10: CAN halt mode 11: Do not use this combination
			1	Loop back mode select bit 0: Loop back mode disabled 1: Loop back mode enabled	
			2	Message order select bit 0: Word access 1: Byte access	CAN sleep mode bit 0: Other than CAN sleep mode 1: CAN sleep mode
			3	Basic CAN mode select bit 0: Basic CAN mode disabled 1: Basic CAN mode enabled	Bus-Off recovery mode select bit 00: Normal mode 01: Entry to CAN halt mode automatically at bus-off entry 10: Entry to CAN halt mode automatically at bus-off end 11: Entry to CAN halt mode by a program request
			4	Bus error interrupt enable bit 0: Bus error interrupt disabled 1: Bus error interrupt enabled	
			5	Sleep mode select bit 0: Sleep mode disabled 1: Sleep mode enabled; clock supply stopped	Forcible return from bus-off bit 0: Nothing occurred 1: Forcible return from bus-off
			6	CAN port enable bit 0: I/O port function 1: CTx/CRx function	Reserved bit
			7	No register bit	CAN port enable bit 0: Function as I/O ports 1: Function as CAN I/O
			8	Time stamp prescaler 00: Period of 1 bit time 01: Period of 1/2 bit time 10: Period of 1/4 bit time 11: Period of 1/8 bit time	CAN mailbox mode select bit 0: Normal mailbox mode 1: FIFO mailbox mode
			9		ID format mode select bit 00: Standard ID mode 01: Extended ID mode 10: Mixed ID mode 11: Do not use this combination
			10	Time stamp counter reset bit 0: In an idle state 1: Force reset of the time stamp counter	

Table 4.17.3 Differences in Registers Associated with CAN Module (2/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
C0CTLR	0210h 0211h	D7C0h D7C1h	11	Return from bus off command bit 0: In an idle state 1: Force return from bus off	Message lost mode select bit 0: Overwrite mode 1: Overrun mode
			12	No register bit	Transmit priority mode select bit 0: ID priority transmit mode 1: Mailbox number priority transmit mode
			13	Listen-only mode select bit 0: Listen-only mode disabled 1: Listen-only mode enabled	Time stamp counter reset bit 0: Nothing occurred 1: Reset
			14	No register bits	Time stamp prescaler select bit 00: Every bit time 01: Every 2-bit time 10: Every 4-bit time 11: Every 8-bit time
			15		

C0STR	0212h 0213h	D7C2h D7C3h	0	Active slot bits 0000: Slot 0 0001: Slot 1 : 1110: Slot 14 1111: Slot 15	CAN reset status flag 0: Not in CAN reset mode 1: In CAN reset mode
			1		CAN halt status flag 0: Not in CAN halt mode 1: In CAN halt mode
			2		CAN sleep status flag 0: Not in CAN sleep mode 1: In CAN sleep mode
			3		Error-passive status flag 0: Not in error-passive state 1: In error-passive state
			4	Successful transmission flag 0: No [successful] transmission 1: The CAN module has transmitted a message successfully	Bus-off status flag 0: Not in bus-off state 1: In bus-off state
			5	Successful reception flag 0: No [successful] reception 1: CAN module received a message successfully	Transmit status flag 0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state
			6	Transmission flag (Transmitter) 0: CAN module is idle or receiver 1: CAN module is transmitter	Receive status flag 0: Bus idle or transmission in progress 1: Reception in progress
			7	Reception flag (Receiver) 0: CAN module is idle or transmitter 1: CAN module is receiver	No register bit
			8	Reset state flag 0: Operation mode 1: Reset mode	NEWDATA status flag 0: No mailbox with NEWDATA bit = 1 1: Mailbox(es) with NEWDATA bit = 1
			9	Loop back state flag 0: Loop back mode disabled 1: Loop back mode enabled	SENTDATA status flag 0: No mailbox with SENTDATA bit = 1 1: Mailbox(es) with SENTDATA bit = 1
			10	Message order state flag 0: Word access 1: Byte access	Receive FIFO status flag 0: No message in receive FIFO 1: Message in receive FIFO

Table 4.17.4 Differences in Registers Associated with CAN Module (3/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
C0STR	0212h 0213h	D7C2h D7C3h	11	Basic CAN mode state flag 0: Basic CAN mode disabled 1: Basic CAN mode enabled	Transmit FIFO status flag 0: Transmit FIFO is full 1: Transmit FIFO is not full
			12	Bus error state flag 0: No error has occurred. 1: A CAN bus error has occurred.	Normal mailbox message lost status flag 0: No mailbox with MSGLOST bit = 1 1: Mailbox(es) with MSGLOST bit = 1
			13	Error passive state flag 0: The CAN module is not in error passive state. 1: The CAN module is in error passive state.	FIFO mailbox message lost status flag 0: RFMLF bit = 0 1: RFMLF bit = 1
			14	Error bus off state flag 0: The CAN module is not in error bus off state. 1: The CAN module is in error bus off state.	Transmission abort status flag 0: No mailbox with TRMABT bit = 1 1: Mailbox(es) with TRMABT bit = 1
			15	No register bit	Error status flag 0: No error occurred 1: Error occurred
C0SSTR	0214h 0215h	—	—	M16C/29 only	—
29: C0ICR 5LD: C0MIER	0216h 0217h	D72Ch to D72Fh	29: 15 - 0 5LD: 31 - 0	Interrupt enable bits	Interrupt enable bit 0: Interrupt disabled 1: Interrupt enabled
C0IDR	0218h 0219h	—	15 - 0	M16C/29 only	—

Table 4.17.5 Differences in Registers Associated with CAN Module (4/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
29: C0CONR 5LD: C0BCR	021Ah 021Bh	D7C4h to D7C6	0 1 2 3	Prescaler division ratio select bits 0000: Divide-by-1 of fCAN 0001: Divide-by-2 of fCAN : 1111: Divide-by-16 of fCAN	Prescaler division ratio set bit (10 bits) If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1
			4	Sampling control bit 0: One time sampling 1: Three times sampling	
			5 6 7	Propagation time segment control bits 000: 1Tq 001: 2Tq : 111: 8Tq	
			8 9 10	Phase buffer segment 1 control bits 000: Do not set 001: 2Tq 010: 3Tq 111: 8Tq	Reserved bit
			11 12 13	Phase buffer segment 2 control bits 000: Do not set 001: 2Tq 010: 3Tq : 111: 8Tq	No register bit Time segment 1 control bit 0000: Do not use this combination 0001: Do not use this combination 0010: Do not use this combination 0011: 4 Tq 0100: 5 Tq 0101: 6 Tq : 1110: 15 Tq 1111: 16 Tq
			14 15	Resynchronization jump width control bits 00: 1Tq 01: 2Tq 10: 3Tq 11: 4Tq	
			18 - 16		Time segment 2 control bit 000: Do not use this combination 001: 2 Tq 010: 3 Tq 011: 4 Tq 100: 5 Tq 101: 6 Tq 110: 7 Tq 111: 8 Tq
			19		No register bit
			21 - 20		Resynchronization jump width control bit 00: 1 Tq 01: 2 Tq 10: 3 Tq 11: 4 Tq
			23 - 22		No register bits

Table 4.17.6 Differences in Registers Associated with CAN Module (5/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
C0RECR	021Ch	D7CEh	—	Difference in address	
C0TECR	021Dh	D7CFh	—	Difference in address	
C0TSR	021Eh 021Fh	D7D4h D7D5h	—	Difference in address	
29: C0AFS 5LD: C0AFSR	0242h 0243h	D7D6h D7D7h	—	Difference in address	
C0MCTLj 29: j = 0 to 15 5LD: j = 0 to 31	0200h to 020Fh	D7A0h to D7BFh	2	Overwrite flag 0: No message has been overwritten in this slot 1: This slot already contained a message, but it has been overwritten by a new one	(When the TRMREQ bit is 0 and the RECREQ bit is 1) Message lost flag 0: Message is not overwritten or overrun 1: Message is overwritten or overrun (When the TRMREQ bit is 1 and the RECREQ bit is 0) Transmission abort complete flag 0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed
			3	Remote frame transmission/ reception status flag 0: Data frame transmission/ reception status 1: Remote frame automatic transfer status	No register bit
			4	Auto response lock mode select bit 0: After a remote frame is received, it will be answered automatically 1: After a remote frame is received, no transmission will be started as long as this bit is set to 1 (Not responding)	One-shot enable bit 0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled
			5	Remote frame corresponding slot select bit 0: Slot not corresponding to remote frame 1: Slot corresponding to remote frame	No register bit

Table 4.17.7 Differences in Registers Associated with CAN Module (6/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
29: CAN0 slot 0 to 15 5LD: C0MB0 to 31	0060h to 015Fh	D500h to D6FFh	0	Standard ID: 11bits	Extended ID: 18bits
			1		
			2		
			3		
			4		
			5	—	
			6	—	
			7	—	
			8	Standard ID: 11bits	
			9		
			10		
			11		
			12		
			13		
			14	—	
			15	—	
			16	Extended ID: 18bits	
			17		
			18		Standard ID: 11bits
			19		
			20	—	
			21	—	
			22	—	
			23	—	
			24	Extended ID: 18bits	
			25		
			26		
			27		
			28		
			29		Reserved bit
			30		Remote frame request bit
			31		ID extension bit
			32		Reserved bits
			33		
			34		
			35		
			36		
			37		
			119-112	Time stamp high-order byte	Time stamp lower byte
			127-120	Time stamp low-order byte	Time stamp higher byte

Table 4.17.8 Differences in Registers Associated with CAN Module (7/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
29: C0GMR C0LMAR C0LMBR 5LD: C0MKR0 to 7	C0GMR: 0160h to 0164h C0LMAR: 0166h to 016Ah C0LMBR: 016Ch to 0170h	D700h to D71Fh	0	Standard ID mask: 11bits	Extended ID mask: 18bits
			1		
			2		
			3		
			4		
			5	—	
			6	—	
			7	—	
			8	Standard ID mask: 11bits	
			9		
			10		
			11		
			12		
			13		
			14	—	
			15	—	
			16	Extended ID mask: 18bits	
			17		
			18		Standard ID mask: 11bits
			19		
			20	—	
			21	—	
			22	—	
			23	—	
			24	Extended ID mask: 18bits	
			25		
			26		
			27		
			28		
			29		Reserved bits
			30		
			31		
			32		
			33		
			34		
			35		
			36		
			37		

Table 4.17.9 Differences in Registers Associated with CAN Module (8/8)

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
C0FIDCR0	—	D720h to D723h	—	—	M16C/5LD only
C0FIDCR1	—	D724h to D727h	—	—	M16C/5LD only
C0MKIVLR	—	D728h to D72Bh	—	—	M16C/5LD only
C0RFCR	—	D7C8h	—	—	M16C/5LD only
C0RFPCR	—	D7C9h	—	—	M16C/5LD only
C0TFCR	—	D7CAh	—	—	M16C/5LD only
C0TFPCR	—	D7CBh	—	—	M16C/5LD only
C0MSSR	—	D7D2h	—	—	M16C/5LD only
C0MSMR	—	D7D3h	—	—	M16C/5LD only
C0CSSR	—	D7D1h	—	—	M16C/5LD only
C0EIER	—	D7CCh	—	—	M16C/5LD only
C0EIFR	—	D7CDh	—	—	M16C/5LD only
C0ECSR	—	D7D0h	—	—	M16C/5LD only
C0TCR	—	D7D8h	—	—	M16C/5LD only

4.18 Differences in A/D Converter

Table 4.18.1 lists Differences in A/D Converter, and Table 4.18.2 lists Differences in Registers Associated with A/D Converter.

Table 4.18.1 Differences in A/D Converter

Item	M16C/29	M16C/5LD
Number of circuits	1 circuit	2 circuits
Resolution	8-bit or 10-bit (selectable)	10 bits
Integral nonlinearity error	AVCC = VREF = 5 V •With 8-bit resolution: ±2 LSB •With 10-bit resolution: ±3 LSB AVCC = VREF = 3.3 V •With 8-bit resolution: ±2 LSB •With 10-bit resolution: ±5 LSB	AVCC = VREF = 5 V ±3 LSB AVCC = VREF = 3.0 V ±3 LSB
Operation modes	One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1 Simultaneous sample sweep mode Delayed trigger mode 0 Delayed trigger mode 1	One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0
Conversion rate per pin	Without sample and hold function •8-bit resolution: 49 ϕAD cycles •10-bit resolution: 59 ϕAD cycles With sample and hold function •8-bit resolution: 28 ϕAD cycles •10-bit resolution: 33 ϕAD cycles	Minimum 43 ϕAD cycles
Analog input pins	8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2)	A/D circuit: 8 pins (AN0 to AN7) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7) + 3 pins (AN3_0 to AN3_2) A/D1 circuit: 4 pins (AN0 to AN3)

Table 4.18.2 Differences in Registers Associated with A/D Converter

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
TB2SC	039Eh	033Eh	—	Difference in address	
ADTRGCON	03D2h	03D2h	0	A/D operation mode select bit 2 0: Other than simultaneous sample sweep mode or delayed trigger mode 0,1 1: Simultaneous sample sweep mode or delayed trigger mode 0,1	Reserved bits
			1	A/D operation mode select bit 3 0: Other than delayed trigger mode 0,1 1: Delayed trigger mode 0,1	
ADSTAT0	03D3h	—	—	M16C/29 only	—
ADCON2	03D4h	03D4h	0	A/D conversion method select bit 0: Without sample and hold 1: With sample and hold	No register bit
			5	Trigger select bit Function varies with each operation mode	Reserved bits
ADCON0	03D6h	03D6h	4 - 3	A/D operation mode select bit 0 00: One-shot mode or Delayed trigger mode 0,1 01: Repeat mode 10: Single sweep mode or Simultaneous sample sweep mode 11: Repeat sweep mode 0 or Repeat sweep mode 1	A/D operation mode select bit 0 00: One-shot mode 01: Repeat mode 10: Single sweep mode 11: Repeat sweep mode 0
			5	Trigger select bit 0: Software trigger 1: Hardware trigger	Trigger select bit 0: Software trigger 1: ADTRG or timer trigger
ADCON1	03D7h	03D7h	2	A/D operation mode select bit 1 0: Other than repeat sweep mode 1 1: Repeat sweep mode 1	Reserved bit
			3	8/10-bit mode select bit 0: 8-bit mode 1: 10-bit mode	No register bit
			5	Vref connect Bit 0: Vref not connected 1: Vref connected	A/D standby bit 0: A/D operation stopped (standby) 1: A/D operation enabled
AD10	—	0140h 0141h	—	—	M16C/5LD only
AD11	—	0142h 0143h	—	—	M16C/5LD only
AD12	—	0144h 0145h	—	—	M16C/5LD only
AD13	—	0146h 0147h	—	—	M16C/5LD only
AD1TRGCON	—	0152h	—	—	M16C/5LD only
AD1CON2	—	0154h	—	—	M16C/5LD only
AD1CON0	—	0156h	—	—	M16C/5LD only
AD1CON1	—	0157h	—	—	M16C/5LD only

4.19 Differences in Flash Memory

Table 4.19.1 lists Differences in Flash Memory, Table 4.19.2 lists Differences in Software Commands, and Table 4.19.3 lists Differences in Registers Associated with Flash Memory.

Table 4.19.1 Differences in Flash Memory

Item	M16C/29		M16C/5LD	
Operating mode (Rewrite mode)	4 modes (CPU rewrite, standard serial I/O, parallel I/O, CAN I/O)		3 modes (CPU rewrite, standard serial I/O, parallel I/O)	
Program method	In units of 1 word (16-bit)		In units of 2 words (32-bit)	
Protect method	Blocks 0 to 5 are write protected by FMR16 bit. In addition, the block 0 and block 1 are write protected by FMR02 bit		Block protection using lock bit	
Number of commands	5 commands		8 commands	
Program and erase endurance	Block 0 to 5 (program area)	100 times or 1,000 times (1)	Program ROM 1 and program ROM 2	1,000 times
	Block A and B (data area)	100 times or 10,000 times (1)	Data flash	10,000 times
ROM code protection	Set the 7 to 6 bits of the ROM Code Protect Control Address besides 11b		Set the ROMCP bit of the Optional Function Select Address 1 to 0	
User boot function	No		Yes	
Forced erase function	No		Yes	
Standard serial I/O mode disable function	No		Yes	
Suspend function	Erase suspend		Erase suspend Program suspend	

Note:
1. Refer to hardware manual for electrical characteristics and more details.

Table 4.19.2 Differences in Software Commands

Software Commands	M16C/29				M16C/5LD					
	First Bus Cycle		Second Bus Cycle		First Bus Cycle		Second Bus Cycle		Third Bus Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Program	WA	XX40h	WA	WD	WA	XX41h	WA	WD0	WA	WD1
Lock bit program	—	—	—	—	BA	XX77h	BA	XXD0h	—	—
Read lock bit status	—	—	—	—	X	XX71h	BA	XXD0h	—	—
Block blank check	—	—	—	—	X	XX25h	BA	XXD0h	—	—

WA: Even write address (but in M16C/5LD, set the end of the address to 0, 4, 8, or C (hexadecimal) only.)
WD: 16-bit write data
WD0: 16-bit write data lower word
WD1: 16-bit write data upper word
BA: Highest-order block address (even address)
X: Any even address in user ROM area (M16C/29)
Given even address in the program ROM 1, program ROM 2, and data flash (M16C/5LD)
XX: Eight high-order bits of command code (ignored)

Table 4.19.3 Differences in Registers Associated with Flash Memory

Symbol	Address		Bit	Differences	
	M16C/29	M16C/5LD		M16C/29	M16C/5LD
FMR4	01B3h	—	—	M16C/29 only	—
FMR1	01B5h	0221h	—	Difference in address	
			1	EW mode 1 select bit 0: EW mode 0 1: EW mode 1	FMR6 register write enable bit 0: Disabled 1: Enabled
			6	Block 0 to 5 rewrite enable bit Set write protection for user ROM area 0: Disable 1: Enable	Lock bit status flag 0: Lock 1: Unlock
			7	Block A, B access wait bit 0: PM17 enabled 1: With wait state (1 wait)	Data flash wait bit 0: 1 wait 1: Follow the PM17 bit setting
FMR0	01B7h	0220h	—	Difference in address	
			2	Block 0, 1 rewrite enable bit Set write protection for user ROM area	Lock bit disable select bit 0: Lock bit enabled 1: Lock bit disabled
FMR2	—	0222h	—	—	M16C/5LD only
FMR3	—	0223h	—	—	M16C/5LD only
FMR6	—	0230h	—	—	M16C/5LD only
OFS1	—	FFFFFh	—	—	M16C/5LD only

4.20 Differences in Flash Memory Block Configuration

The following figure shows the Differences in Flash Memory Block Configuration.

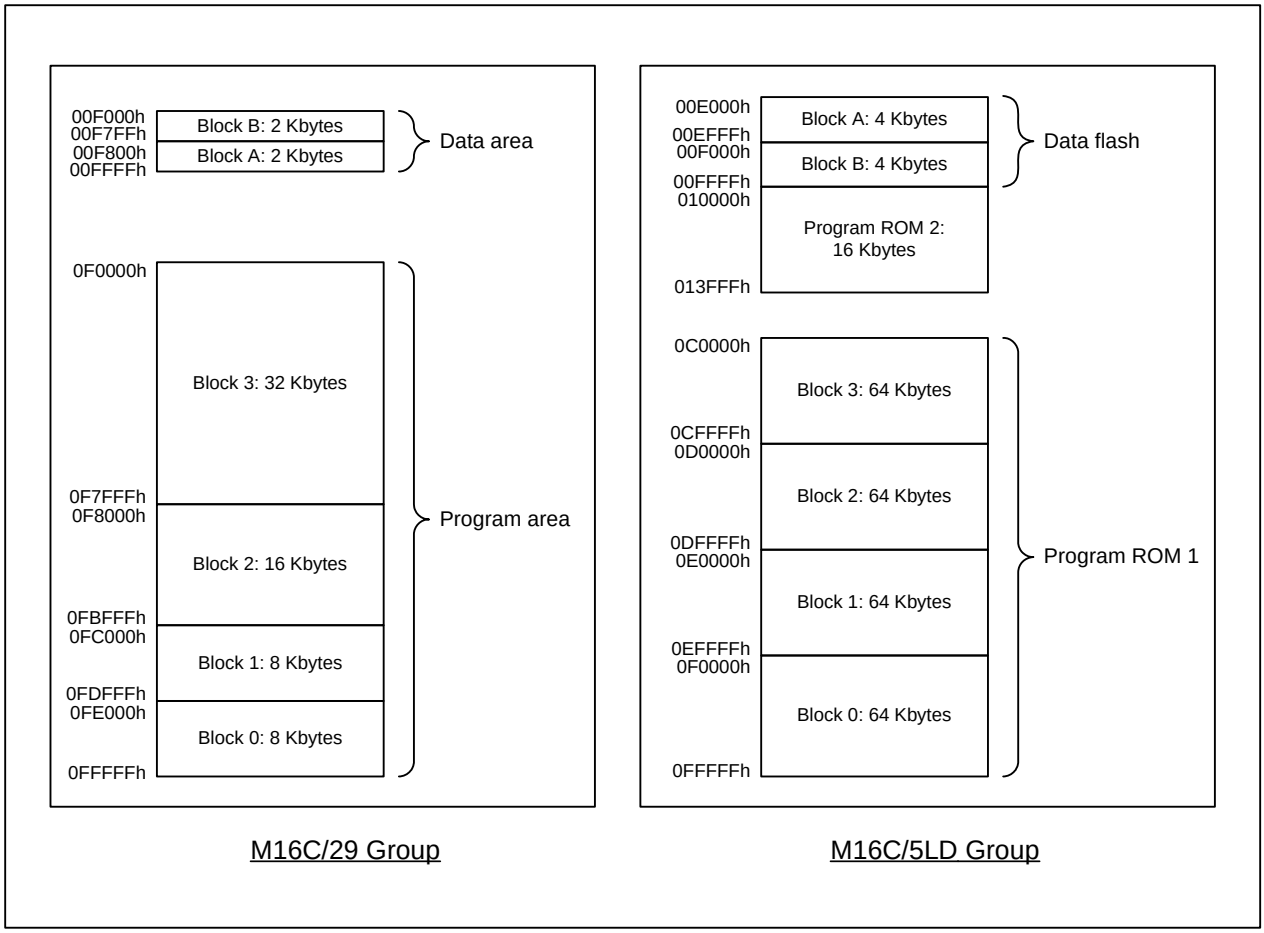

Figure 4.1 Differences in Flash Memory Block Configuration

4.21 New Functions in M16C/5LD

The M16C/5LD Group is a further development of the M16C/29 Group and includes the following new functions:

- Task monitor timer
- Real-time clock

4.22 Differences in Development Tools

Table 4.22.1 lists Differences in Development Tools.

Table 4.22.1 Differences in Development Tools

Types of Tool	M16C/29	M16C/5LD
C compiler	M3T-NC30WA	M3T-NC30WA
Real-time OS	M3T-MR30	M3T-MR30
Emulator debugger	PC7501	E100
MCU unit	—	R0E535M00MCU00
Emulation probe	M3028BT-EPB-4	—
Compact emulator	M3028BT2-CPE	—
On-chip debugging emulator	E8 E8a	E8a

5. Reference Documents

Hardware Manuals
M16C/29 Group Hardware Manual Rev.1.13
M16C/5LD Group Hardware Manual Rev.0.70
Download the most recent versions from the Renesas Technology website.

Technical News/Technical Update
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Website and Support

Renesas Technology Website
http://www.renesas.com/

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REVISION HISTORY	M16C/29 Group, M16C/5LD Group Differences between M16C/29 and M16C/5LD

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		Page	Summary
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