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R32C/100 Series

Configuring PLL Mode

1. Abstract

This document describes and provides an example of how to exit PLL self-oscillation mode and enter PLL mode.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

This application note describes how to exit PLL self-oscillation mode and enter PLL mode.

In PLL mode, the PLL clock is generated using the main clock as a source.

In PLL self-oscillation mode, the PLL frequency synthesizer self-oscillates from a fixed oscillation frequency.

The figure below shows the MCU entering PLL mode.

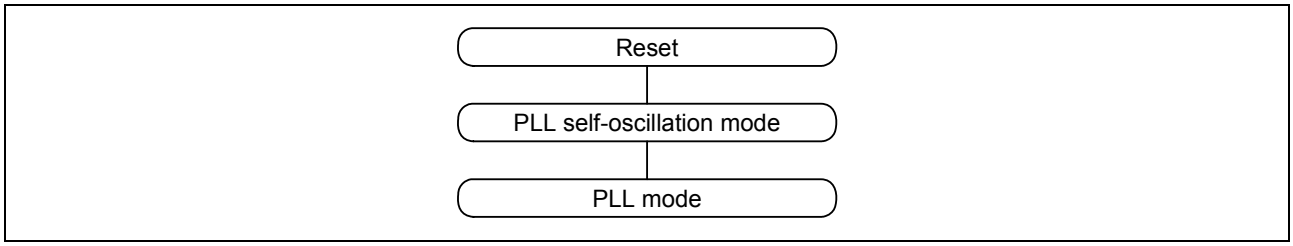


Figure 3.1 MCU Entering PLL Mode

4. Setting

This section describes the settings for exiting PLL self-oscillation mode and entering PLL mode.

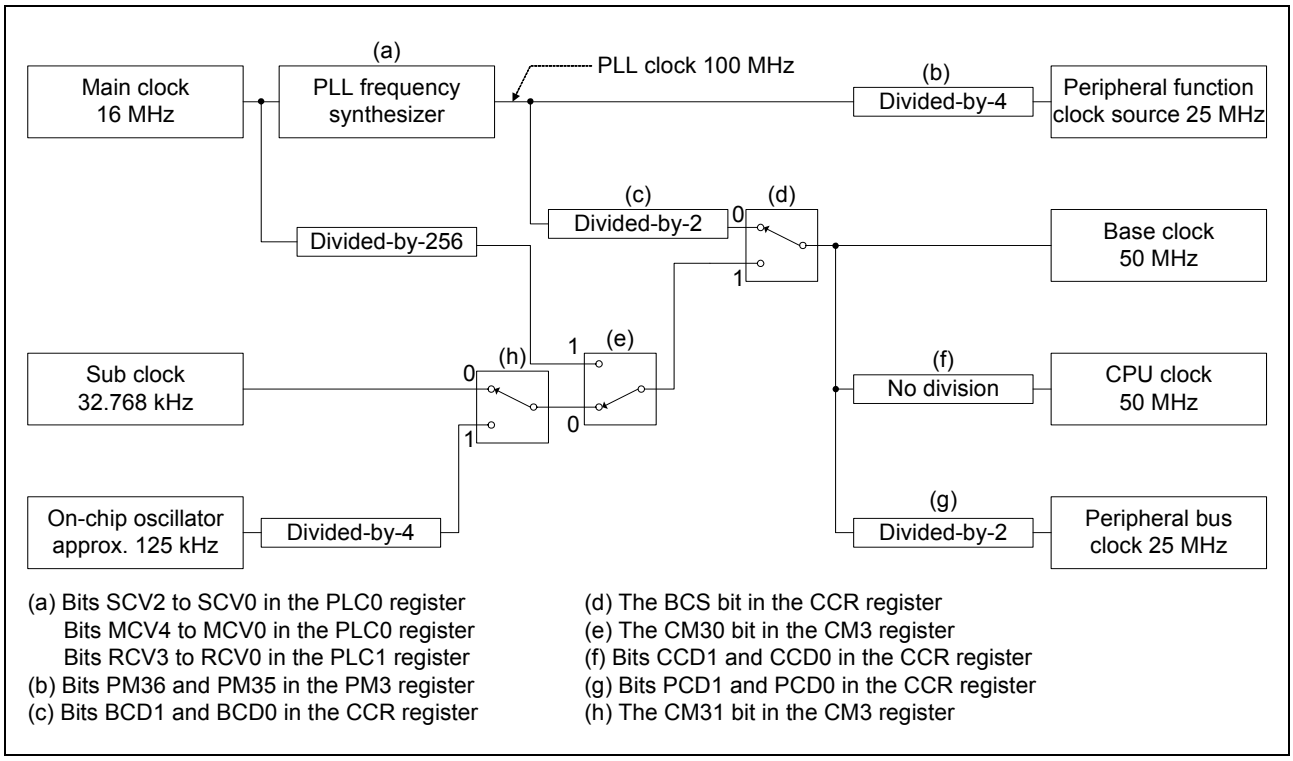
4.1 Clock and Individual Register Settings

In this application, individual clock frequencies are set in the PLL mode as shown in the table below.

Table 4.1 Individual Clock Frequency Settings

Clock Name	Frequency
Main clock (XIN)	16 MHz
PLL clock	100 MHz
Base clock	50 MHz
CPU clock	50 MHz
Peripheral bus clock	25 MHz
Peripheral function clock source	25 MHz

Clock relationships are shown in the figure below. For setting PLL mode, see **Table 4.2** to set registers PLC1, PLC0, PM3, and CCR.



(a) Bits SCV2 to SCV0 in the PLC0 register
Bits MCV4 to MCV0 in the PLC0 register
Bits RCV3 to RCV0 in the PLC1 register
(b) Bits PM36 and PM35 in the PM3 register
(c) Bits BCD1 and BCD0 in the CCR register
(d) The BCS bit in the CCR register
(e) The CM30 bit in the CM3 register
(f) Bits CCD1 and CCD0 in the CCR register
(g) Bits PCD1 and PCD0 in the CCR register
(h) The CM31 bit in the CM3 register

Figure 4.1 Clock Division Ratio Setting Block Diagram

Table 4.2 Settings for Registers PLC1, PLC0, PM3, and CCR

Register	Value	Reference
PLC1	03h	Refer to section **4.2 "Conditions for Setting the PLL Control Register"**.
PLC0	04h	Refer to section **4.2 "Conditions for Setting the PLL Control Register"**.
PM3	40h	Bits PM36 and PM35: 10 (divide by 4)
CCR	1Fh	Bits PCD1 and PCD0: 01b (divide by 2) Bits CCD1 and CCD0: 11b (no division) Bits BCD1 and BCD0: 11b (divide by 2) BCS bit: 0 (PLL clock)

Set the PBC register before setting the CCR register. Only set the PBC register once after resetting the MCU.

Values for bits PWR4 to PWR0 and PRD4 to PRD0 in the PBC register are dependent on the values set to bits PCD1 and PCD0 in the CCR register (as shown in the table below).

Table 4.3 PWR4 to PWR0 and PRD4 to PRD0 Bit Settings Based on PCD1 and PCD0 Bit Settings

CCR Register	PBC Register	
Bits PCD1 and PCD0	Bits PWR4 to PWR0	Bits PRD4 to PRD0
00b (do not set this value)	-	-
01b	00101b	00100b
10b	01010b	01101b
11b	01111b	01111b

4.2 Conditions for Setting the PLL Control Register

The PLL frequency synthesizer division ratio *m* is represented by the main counter division ratio *n* and swallow counter divider ratio *a* in the following equation: $m = 5n + a$. However, the value of *a* can only be set as follows: $0 \leq a < 5$ or $0 \leq a \leq n$. Set the division ratio *m* to $25 \leq m \leq 100$.

The PLL clock frequency is the reference counter division ratio *r* and the main clock division ratio. Therefore, PLL clock frequency becomes:

$= \frac{m}{r}$ × main clock frequency

$= \frac{5n + a}{r}$ × main clock frequency

Set the clock generated by dividing the main clock by *r* to a value between 2 MHz and 4 MHz.

In this application note, set $n = 5$, $a = 0$, and $r = 4$ to get the following:

PLL clock frequency $= \frac{5 \times 5 + 0}{4} \times 16$ = 100 MHz

Therefore, set bits SCV2 to SCV0 in the PLC register to 0 as $a = 0$, bits MCV4 to MCV0 to 5 as $n - 1 = 4$, and bits RCV3 to RCV0 to 2 as $r - 1 = 3$. The result is PLC1 = 03h, and PLC0 = 04h.
The figure below shows an example of setting PLC1 and PLC0 register values.

Table 4.4 PLC1 and PLC0 Register Values (1)

Main Clock (MHz)	r	Reference Clock (MHz)	n	a	m	PLC1 Value	PLC0 Value	$\frac{m}{r}$	PLL Clock (MHz)
4	2	2	9	3	48	01h	68h	24	96
6	2	3	6	2	32	01h	45h	16	96
8	3	2.6667	7	1	36	02h	26h	12	96
10	5	2	9	3	48	04h	68h	9.6	96
12	4	3	6	2	32	03h	45h	8	96
16	5	3.2	6	0	30	04h	05h	6	96
4	1	4	5	0	25	00h	04h	25	100
6	3	2	10	0	50	02h	09h	16.6667	100
8	2	2	5	0	25	01h	04h	12.5	100
10	3	3.3333	6	0	30	02h	05h	10	100
12	3	4	5	0	25	02h	04h	8.3333	100
16	4	4	5	0	25	03h	04h	6.25	100
4	1	4	6	2	32	00h	45h	32	128
6	3	2	12	4	64	02h	8Bh	21.3333	128
8	2	4	6	2	32	01h	45h	16	128
10	5	2	12	4	64	04h	8Bh	12.8	128
12	3	4	6	2	32	02h	45h	10.6667	128
16	4	4	6	2	32	03h	45h	8	128

Note:
1. Use the values listed in this table.
Refer to the "Clock Generator" chapter in the corresponding hardware manual for the latest information on setting values.

4.3 Notes on Setting the PLL Clock

After rewriting the PLL clock value, wait at least $t_{LOCK(PLL)}$ until the PLL clock stabilizes. This section describes setting the time to 1 ms using timer A1 to measure the wait time until the PLL clock stabilizes. The table below shows the values for timer A1. For more information on $t_{LOCK(PLL)}$, refer to the Electrical Characteristics chapter in the hardware manual.

Table 4.5 Timer A1 Settings

Timer	Operation Mode	Count Source Division Ratio	Count Source	f2n Division Ratio	f2n Clock Source
Timer A1	Timer mode	16000 (1)	f2n	No division	Main clock (16 MHz)

Note:
1. These values correspond to a 1 ms wait time. Use the formula below to calculate wait time.
   Wait time = Timer for 1 count of the count source × count source divide ratio

$$\frac{1}{16\times10^{6}} \times 16000 = 0.001 \text{ ms (1 ms)}$$

4.4 Notes on Rewriting Protected Registers

Registers set in this application (CCR, PM2, PM3, PLC1, PLC0, and PBC) are protected by the protect register.

The protect function protects important registers from being unintentionally rewritten due to a program runaway. After deasserting the protect function, protected registers can be rewritten.

After enabling writing to the PRC2 bit in the PRCR register, the bit becomes write disabled after writing to an arbitrary address. Rewrite registers PLC0 and PLC1 with the next instruction after enabling writing to the PRC2 bit. Do not generate an interrupt or perform DMA transfer in between enabling writing to the PRC2 bit and setting registers PLC0 and PLC1. Regardless of writing to an arbitrary address, bits PRC0 and PRC1, and the PRR register will not become write disabled and must be set to write disabled by the user.

Table 4.6 Protect Register and Protected Registers

Protect Register	Write Disabled/Enabled	Protected Registers
PRCR	PRC0 Bit 0: Write disabled 1: Write enabled	CM0 to CM2, and PM3
	PRC1 Bit 0: Write disabled 1: Write enabled	PM0, PM2, CSOP0, CSOP1, CSOP2, INVC0, INVC1, IOBC, and I2CMR
	PRC2 Bit 0: Write disabled 1: Write enabled	PD9, P9_iS (i = 0 to 7), PLC0, and PLC1
PRCR2	PRC27 Bit 0: Write disabled 1: Write enabled	CM3
PRCR3	PRC31 Bit 0: Write disabled 1: Write enabled	VRCR, LVDC, and DVCR
PRR	b7 to b0 Value Other than AAh: Write disabled AAh: Write enabled	CCR, FMCR, PBC, FEBC0,FEBC3,EBC0 to EBC3, CB01, CB12, and CB23

4.5 Setting Overview

The flowchart below shows the steps for exiting PLL self-oscillation mode and entering PLL mode. Refer to section **4.6 "Detailed Settings"** for individual settings.

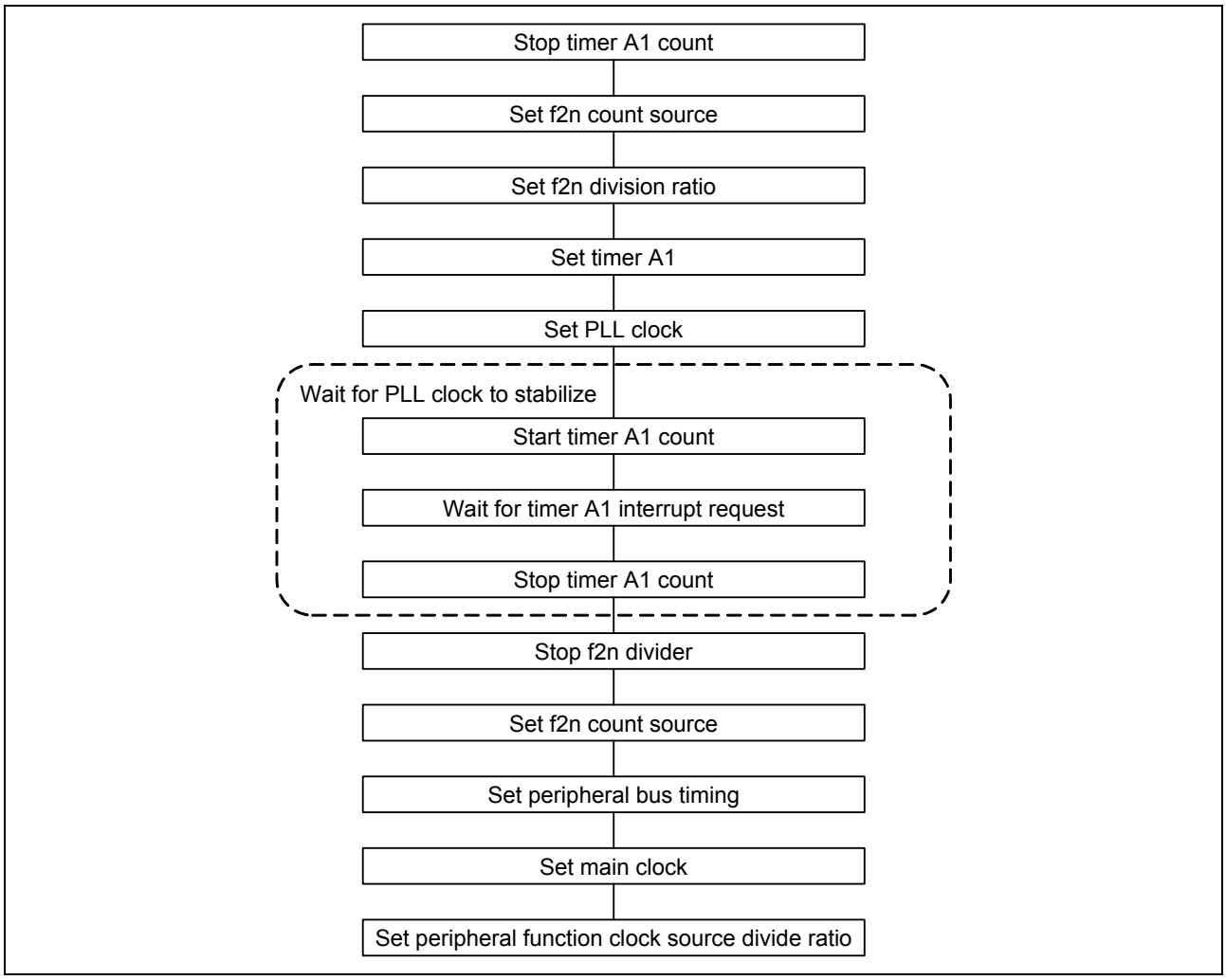
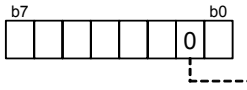


Figure 4.2 Entering PLL Mode

4.6 Detailed Settings

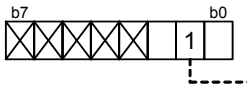
(1) Stop the timer A1 count.



Count Start Register (TABSR)

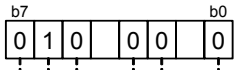
TA1S — Timer A1 Count Start Bit
0: Count stopped

(2) Set the f2n count source.



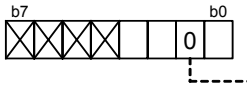
Protect Register (PRCR)

PRC1 — Protect Bit 1
1: Write enabled for registers PM0, PM2, CSOP0, CSOP1, CSOP2, INVC0, INVC1, IOBC, and I2CMR



Processor Mode Register 2 (PM2)

Set to 0.
PM26 — f2n Count Source Select Bit
1: Main clock
Set to 0.

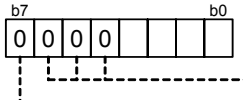


Protect Register (PRCR)

PRC1 (1) — Protect Bit 1
0: Write disabled for registers PM0, PM2, CSOP0, CSOP1, CSOP2, INVC0, INVC1, IOBC, and I2CMR

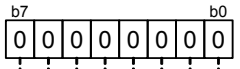
Note:
1. After setting this bit to 1 (write enabled), make sure to set it to 0 (write disabled).

(3) Set the f2n division ratio.



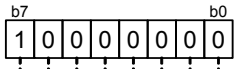
Count Source Prescaler Register (TCSPR)

Set to 0.
CST (1) — Divider Operation Enable Bit
0: Divider stopped



Count Source Prescaler Register (TCSPR)

CNT3 to CNT0 (2) — Divide Ratio Select Bit
0000b: No division
Set to 0.
CST — Divider Operation Enable Bit
0: Divider stopped



Count Source Prescaler Register (TCSPR)

CNT3 to CNT0 — Divide Ratio Select Bit
0000b: No division
Set to 0.
CST — Divider Operation Enable Bit
1: Divider enabled

Notes:
1. Set this bit to 0 (divider stopped) before rewriting bits CNT3 to CNT0.
2. Assuming the value for these bits is n, the main clock or PLL clock divided by 2n becomes f2n. When n = 0, there is no division.

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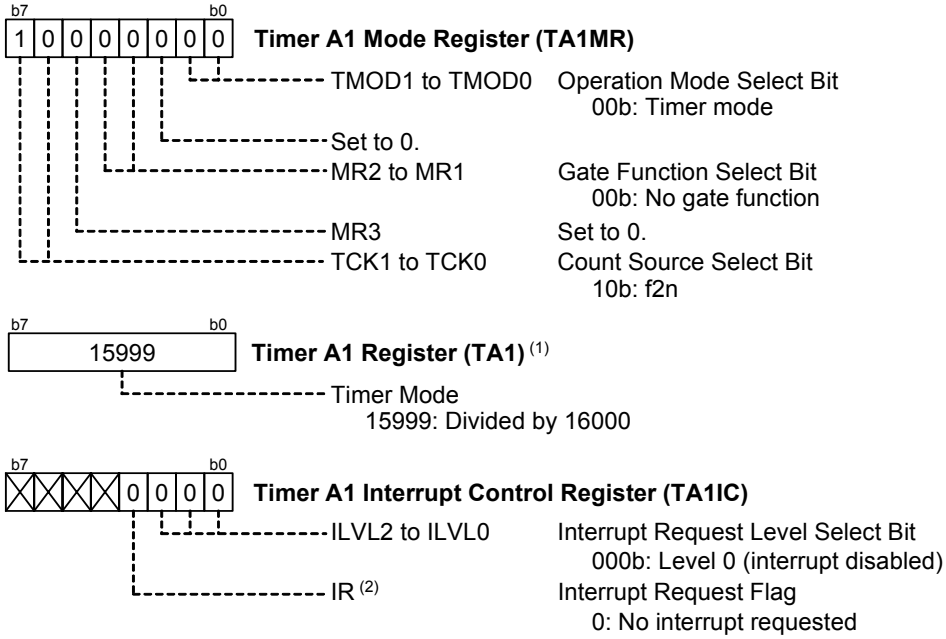
(4) Set timer A1.



Notes:
1. Read/Write this register in 16-bit units.
2. Set this bit to 0.

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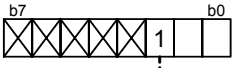
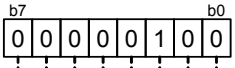
(5) Set the PLL clock.



Protect Register (PRCR)

PRC2 (1)

Protect Bit 2
1: Write enabled for registers PD9, P9_iS (i = 0 to 7), PLC0, and PLC1



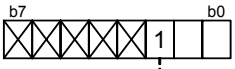
PLL Control Register 0 (PLC0) (2)

MCV4 to MCV0

Main Counter Division Ratio Set Bit
000b: If the main counter division ratio is n, then set n - 1. Refer to section 4.2 for detailed settings.

SVC2 to SVC0

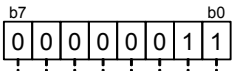
Swallow Counter Division Ratio Set Bit
If the setting value is *a*, the division ratio for two modular prescalers is 6 for *a* times out of *n* times, and 5 for *n - a* times. Refer to section 4.2 “Conditions for Setting the PLL Control Register” for more details.



Protect Register (PRCR)

PRC2

Protect Bit 2
1: Write disabled for registers PD9, P9_iS (i = 0 to 7), PLC0, and PLC1



PLL Control Register 1 (PLC1)

RCV3 to RCV0

Reference Counter Division Ratio Set Bit
To divide the main clock by *r*, set these bits to *r - 1*.

SEO

Self-oscillation Mode Setting Bit
0: Main clock multiplication mode

Set to 0.

Notes:
1. After setting the PRC2 bit to 1 (write enabled), by writing to an arbitrary address, this bit becomes 0 (write disabled). Therefore, when setting multiple registers protected by this bit, set this bit to 1 after setting each register.
2. This register can be rewritten once after being reset.

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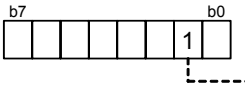
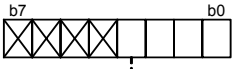
(6) Start the timer A1 count.



Count Start Register (TABSR)

TA1S — Timer A1 Count Start Bit
1: Count started

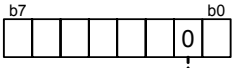
(7) Wait for the timer A1 interrupt request. Wait until the IR bit becomes 1.



Timer A1 Interrupt Control Register (TA1IC)

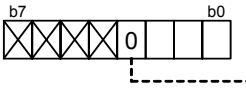
IR — Interrupt Request Flag
0: No interrupt requested
1: Interrupt requested

(8) Stop the timer A1 count.



Count Start Register (TABSR)

TA1S — Timer A1 Count Start Bit
0: Count stopped



Timer A1 Interrupt Control Register (TA1IC)

IR (1) — Interrupt Request Flag
0: No interrupt requested

Note:
1. Set this bit to 0.

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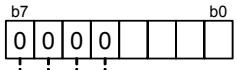
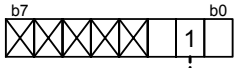
(9) Stop the f2n divider.



Count Source Prescaler Register (TCSPR)

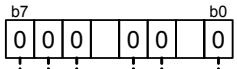
- Set to 0.
- CST — Divider Operation Enable Bit
  0: Divider stopped

(10) Set the f2n count source.



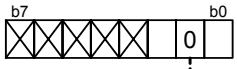
Protect Register (PRCR)

- PRC1 — Protect Bit 1
  1: Write enabled for registers PM0, PM2, CSOP0, CSOP1, CSOP2, INVC0, INVC1, IOBC, and I2CMR



Processor Mode Register 2 (PM2)

- Reserved — Set to 0.
- PM26 — f2n Clock Source Select Bit
  0: Peripheral function clock source
- Set to 0.

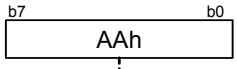


Protect Register (PRCR)

- PRC1 (1) — Protect Bit 1
  0: Write disabled for registers PM0, PM2, CSOP0, CSOP1, CSOP2, INVC0, INVC1, IOBC, and I2CMR

Note:
1. After setting this bit to 1 (write enabled), make sure to set it to 0 (write disabled).

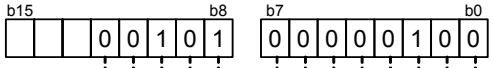
(11) Set timer A1.



Protect Deassert Register (PRR)

Controls the protection of registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23.

AAh: Write enabled



Peripheral Bus Control Register (PBC) (1)

- PRD4 to PRD0 — Read Timing Set Bit
  When bits PCD1 and PCD0 are 01b, set these bits to 00100b.
- Set to 0.
- PWR4 to PWR0 — Write Timing Set Bit
  When bits PCD1 and PCD0 are 01b, set these bits to 00101b.

Notes:
1. Only set this register once after MCU reset. Do not rewrite this register after setting the CCR register.
2. Even at the next step, registers protected by the PRR register are written to, so leave the PRR register setting as AAh (write enabled).

Continued on next page

Continued from previous page

(12) Set the main clock.

b7 b0

0	0	0	1	1	1	1	1

Clock Control Register (CCR)

- BCD1 and BCD0 — Base Clock Division Select Bit
  - 11b: Divide by 2
- CCD1 and CCD0 — CPU Clock Division Select Bit
  - 11b: No division
- PCD1 and PCD0 (1) — Peripheral Bus Clock Division Select Bit
  - 01b: Divide by 2
- Set to 0.
- BCS — Base Clock Source Select Bit
  - 0: PLL clock

b7 b0

00h

Protect Deassert Register (PRR) (4)

- Controls protection over registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0 to EBC3, CB01, CB12, and CB23
  - Value Other than AAh: Write disabled

Notes:
1. Set the PBC register before setting these bits. Only set these bits once after resetting the MCU. Do not rewrite these bits after setting them.
2. Do not rewrite the base clock division value and peripheral bus clock division value simultaneously. Do not make the CPU clock division value larger than the bus clock division ratio.
3. Increase the peripheral bus clock division value before decreasing the base clock division value.
4. After setting this register to AAh (write enabled), make sure to set it to a value other than AAh (write disabled).

(13) Set the peripheral function clock source division ratio.

b7 b0

X	X	X	X	X			1

Protect Register (PRCR)

- PRC0 — Protect Bit 0
  - 1: Write enabled for registers CM0, CM1, CM2, and PM3

b7 b0

0	1	0	0	0	0	0	0

Processor Mode Register 3 (PM3)

- Set to 0.
- PM36 and PM35 (1) — Peripheral Function Clock Source Division Ratio Select Bit
  - 10b: Divided-by-4
- Set to 0.

b7 b0

X	X	X	X				0

Protect Register (PRCR)

- PRC0 (2) — Protect Bit 0
  - 0: Write disabled for registers CM0, CM1, CM2, and PM3

Notes:
1. Set these bits to the peripheral function clock source (f1) frequency is 32 MHz or less.
2. After setting this bit to 1 (write enabled), make sure to set it to 0 (write disabled).

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

The sample program is made up of main functions and main clock multiplication mode setting functions (shown in the following flowcharts). Numbers in parenthesis ((1) to (14)) coincide with the flow numbers in the sample program.

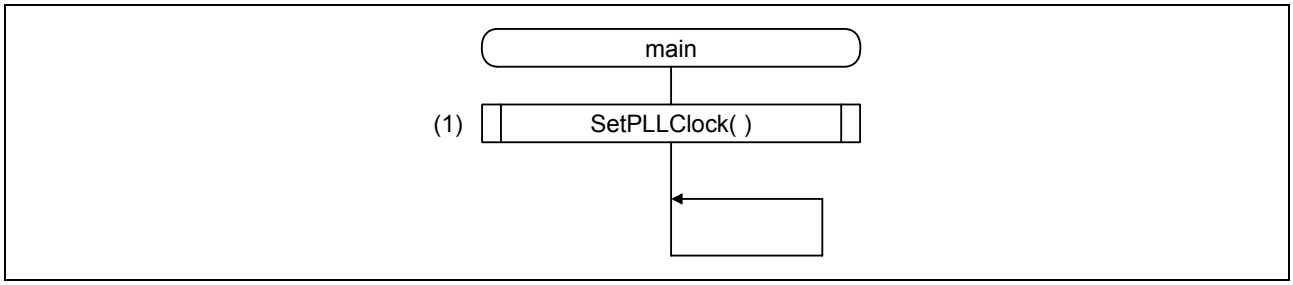


Figure 5.1 Main Function Flowchart

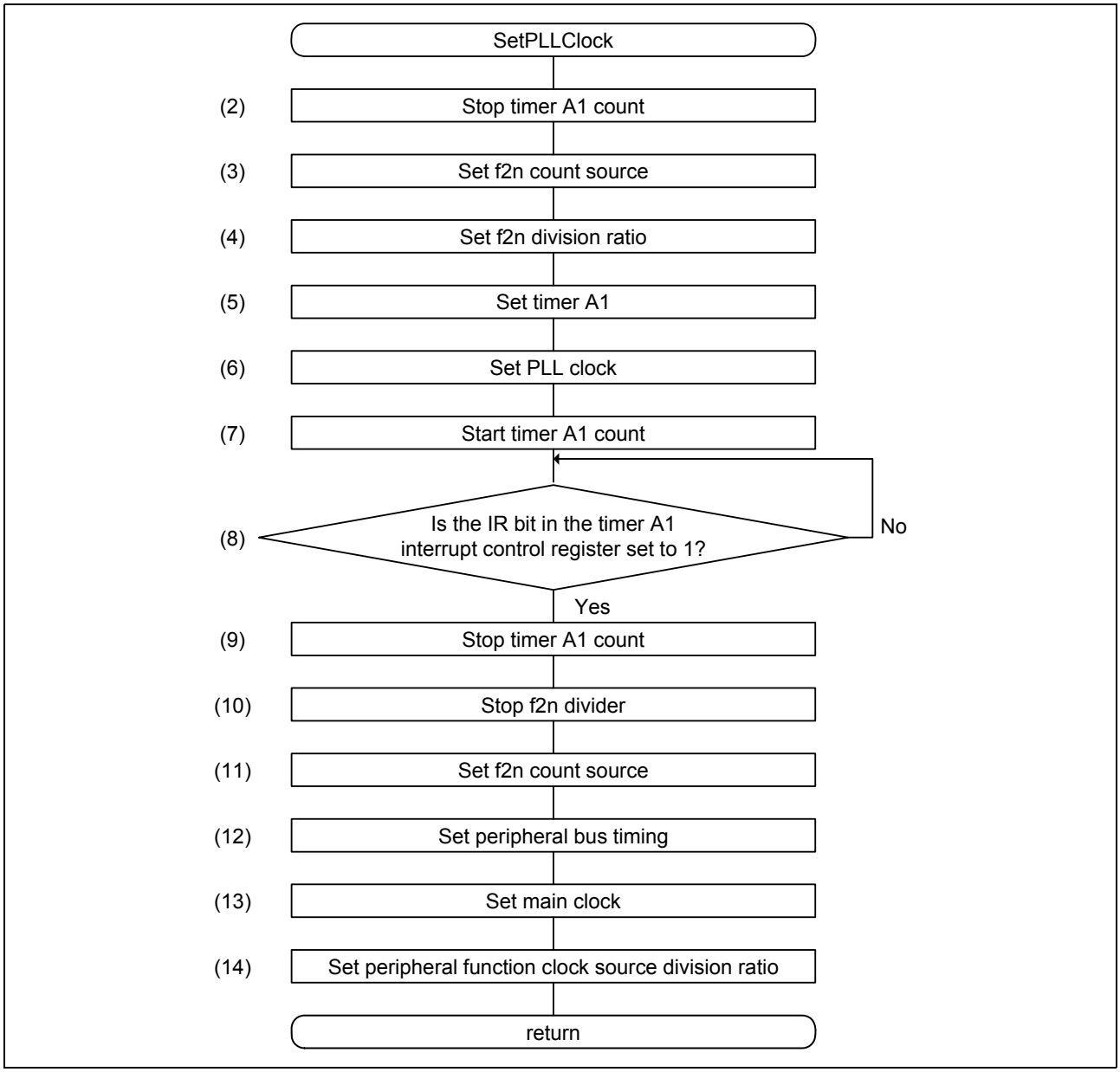


Figure 5.2 Main Clock Multiplication Mode Setting Functions

6. Reference Documents

Hardware Manual: R32C/118 Group Hardware Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual: R32C/100 Series C Compiler Ver. 1.02 User's Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology Website
http://www.renesas.com/

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Revision History	Configuring PLL Mode

Revision	Date	Page	Summary
1.00	Jan.29, 2010	—	Initial release

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