R32C/111 Group

Configuring Function Select Register

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1. Abstract

This document describes how to set the function select registers to enable I/O pin settings for the internal peripheral functions of the R32C/111 Group 100-pin package. Refer to the user's manual for details on each function.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):
MCU: R32C/111 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/111 Group. Check the user's manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

Each pin in the R32C/111 Group function as a programmable I/O port, an I/O pin for internal peripheral functions, or a bus control pin. These functions can be switched by setting the function select registers or the processor mode registers. This document particularly addresses setting the function select registers to enable input/output of the internal peripheral functions.
The registers that control I/O pins are as follows:

- Output function select register

This register selects an output function of either the programmable I/O port or a peripheral function if these two functions share a pin. This register also selects an output function of analog I/O pin, a programmable I/O port or a peripheral function to enable input/output of the analog I/O pin if these three functions share a pin.

- Input function select register

When a peripheral function input is assigned to multiple pins, this register selects which input pin should be connected to the peripheral function.

4. Settings

The following describes setting the function select register to enable pin input/output, and setting the input function select register to select the peripheral function input pin.

4.1 Function Select Register Settings

Table 4.1 to Table 4.3 list the Settings of the Programmable I/O Ports When Used as Output Ports.
Table 4.4 lists the Settings of the Timer When Used as Output Ports.
Table 4.5 and Table 4.6 list the Settings of the Serial Interface When Used as Output Ports.
Table 4.7 lists the Settings of the Intelligent I/O When Used as Output Ports.
Table 4.8 lists the Settings of the A/D Converter When Used as Output Ports.
Table 4.9 lists the Settings of the D/A Converter When Used as Output Ports.

Table 4.1 Settings of the Programmable I/O Ports When Used as Output Ports (1/3)

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Output port 0	P0_0	P0_0	PD0_0	1	P0_0S	00h
	P0_1	P0_1	PD0_1	1	P0_1S	00h
	P0_2	P0_2	PD0_2	1	P0_2S	00h
	P0_3	P0_3	PD0_3	1	P0_3S	00h
	P0_4	P0_4	PD0_4	1	P0_4S	00h
	P0_5	P0_5	PD0_5	1	P0_5S	00h
	P0_6	P0_6	PD0_6	1	P0_6S	00h
	P0_7	P0_7	PD0_7	1	P0_7S	00h
Output port 1	P1_0	P1_0	PD1_0	1	P1_0S	00h
	P1_1	P1_1	PD1_1	1	P1_1S	00h
	P1_2	P1_2	PD1_2	1	P1_2S	00h
	P1_3	P1_3	PD1_3	1	P1_3S	00h
	P1_4	P1_4	PD1_4	1	P1_4S	00h
	P1_5	P1_5	PD1_5	1	P1_5S	00h
	P1_6	P1_6	PD1_6	1	P1_6S	00h
	P1_7	P1_7	PD1_7	1	P1_7S	00h
Output port 2	P2_0	P2_0	PD2_0	1	P2_0S	00h
	P2_1	P2_1	PD2_1	1	P2_1S	00h
	P2_2	P2_2	PD2_2	1	P2_2S	00h
	P2_3	P2_3	PD2_3	1	P2_3S	00h
	P2_4	P2_4	PD2_4	1	P2_4S	00h
	P2_5	P2_5	PD2_5	1	P2_5S	00h
	P2_6	P2_6	PD2_6	1	P2_6S	00h
	P2_7	P2_7	PD2_7	1	P2_7S	00h

Table 4.2 Settings of the Programmable I/O Ports When Used as Output Ports (2/3)

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Output port 3	P3_0	P3_0	PD3_0	1	P3_0S	00h
	P3_1	P3_1	PD3_1	1	P3_1S	00h
	P3_2	P3_2	PD3_2	1	P3_2S	00h
	P3_3	P3_3	PD3_3	1	P3_3S	00h
	P3_4	P3_4	PD3_4	1	P3_4S	00h
	P3_5	P3_5	PD3_5	1	P3_5S	00h
	P3_6	P3_6	PD3_6	1	P3_6S	00h
	P3_7	P3_7	PD3_7	1	P3_7S	00h
Output port 4	P4_0	P4_0	PD4_0	1	P4_0S	00h
	P4_1	P4_1	PD4_1	1	P4_1S	00h
	P4_2	P4_2	PD4_2	1	P4_2S	00h
	P4_3	P4_3	PD4_3	1	P4_3S	00h
	P4_4	P4_4	PD4_4	1	P4_4S	00h
	P4_5	P4_5	PD4_5	1	P4_5S	00h
	P4_6	P4_6	PD4_6	1	P4_6S	00h
	P4_7	P4_7	PD4_7	1	P4_7S	00h
Output port 5	P5_0	P5_0	PD5_0	1	P5_0S	00h
	P5_1	P5_1	PD5_1	1	P5_1S	00h
	P5_2	P5_2	PD5_2	1	P5_2S	00h
	P5_3	P5_3	PD5_3	1	P5_3S	00h
	P5_4	P5_4	PD5_4	1	P5_4S	00h
	P5_5	P5_5	PD5_5	1	P5_5S	00h
	P5_6	P5_6	PD5_6	1	P5_6S	00h
	P5_7	P5_7	PD5_7	1	P5_7S	00h
Output port 6	P6_0	P6_0	PD6_0	1	P6_0S	00h
	P6_1	P6_1	PD6_1	1	P6_1S	00h
	P6_2	P6_2	PD6_2	1	P6_2S	00h
	P6_3	P6_3	PD6_3	1	P6_3S	00h
	P6_4	P6_4	PD6_4	1	P6_4S	00h
	P6_5	P6_5	PD6_5	1	P6_5S	00h
	P6_6	P6_6	PD6_6	1	P6_6S	00h
	P6_7	P6_7	PD6_7	1	P6_7S	00h
Output port 7	P7_0 (1)	P7_0	PD7_0	1	P7_0S	00h
	P7_1 (1)	P7_1	PD7_1	1	P7_1S	00h
	P7_2	P7_2	PD7_2	1	P7_2S	00h
	P7_3	P7_3	PD7_3	1	P7_3S	00h
	P7_4	P7_4	PD7_4	1	P7_4S	00h
	P7_5	P7_5	PD7_5	1	P7_5S	00h
	P7_6	P7_6	PD7_6	1	P7_6S	00h
	P7_7	P7_7	PD7_7	1	P7_7S	00h

Note:
1. These ports are N-channel open drain output.

Table 4.3 Settings of the Programmable I/O Ports When Used as Output Ports (3/3)

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Output port 8	P8_0	P8_0	PD8_0	1	P8_0S	00h
	P8_1	P8_1	PD8_1	1	P8_1S	00h
	P8_2	P8_2	PD8_2	1	P8_2S	00h
	P8_3	P8_3	PD8_3	1	P8_3S	00h
	P8_4	P8_4	PD8_4	1	P8_4S	00h
	P8_6	P8_6	PD8_6	1	P8_6S	00h
	P8_7	P8_7	PD8_7	1	P8_7S	00h
Output port 9	P9_3	P9_3	PD9_3 (1)	1	P9_3S (1)	00h
	P9_4	P9_4	PD9_4 (1)	1	P9_4S (1)	00h
	P9_5	P9_5	PD9_5 (1)	1	P9_5S (1)	00h
	P9_6	P9_6	PD9_6 (1)	1	P9_6S (1)	00h
	P9_7	P9_7	PD9_7 (1)	1	P9_7S (1)	00h
Output port 10	P10_0	P10_0	PD10_0	1	P10_0S	00h
	P10_1	P10_1	PD10_1	1	P10_1S	00h
	P10_2	P10_2	PD10_2	1	P10_2S	00h
	P10_3	P10_3	PD10_3	1	P10_3S	00h
	P10_4	P10_4	PD10_4	1	P10_4S	00h
	P10_5	P10_5	PD10_5	1	P10_5S	00h
	P10_6	P10_6	PD10_6	1	P10_6S	00h
	P10_7	P10_7	PD10_7	1	P10_7S	00h

Note:

1. The instruction to set this register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupts or DMA transfers should be generated between these two instructions.

Table 4.4 Settings of the Timer When Used as Output Ports

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Timer output	TA0OUT	P3_0	PD3_0	1	P3_0S	01h
		P7_0 (1)	PD7_0	1	P7_0S	01h
	TA1OUT	P3_2	PD3_2	1	P3_2S	01h
		P7_2	PD7_2	1	P7_2S	01h
	TA2OUT	P3_4	PD3_4	1	P3_4S	01h
		P7_4	PD7_4	1	P7_4S	01h
	TA3OUT	P3_1	PD3_1	1	P3_1S	01h
		P7_6	PD7_6	1	P7_6S	01h
	TA4OUT	P3_6	PD3_6	1	P3_6S	01h
		P8_0	PD8_0	1	P8_0S	01h
Three-phase motor control timers	V	P3_2	PD3_2	1	P3_2S	02h
		P7_2	PD7_2	1	P7_2S	02h
	$\overline{V}$	P3_3	PD3_3	1	P3_3S	02h
		P7_3	PD7_3	1	P7_3S	02h
	W	P3_4	PD3_4	1	P3_4S	02h
		P7_4	PD7_4	1	P7_4S	02h
	$\overline{W}$	P3_5	PD3_5	1	P3_5S	02h
		P7_5	PD7_5	1	P7_5S	02h
	U	P3_6	PD3_6	1	P3_6S	02h
		P8_0	PD8_0	1	P8_0S	02h
	$\overline{U}$	P3_7	PD3_7	1	P3_7S	02h
		P8_1	PD8_1	1	P8_1S	02h

Note:
1. This port is N-channel open drain output.

Table 4.5 Settings of the Serial Interface When Used as Output Ports (1/2)

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
UART0	$\overline{\text{RTS0}}$	P6_0	PD6_0	1	P6_0S	03h
	CLK0 output	P6_1	PD6_1	1	P6_1S	03h
	SCL0 output	P6_2	PD6_2	1	P6_2S	03h
	TXD0/SDA0 output	P6_3	PD6_3	1	P6_3S	03h
UART1	$\overline{\text{RTS1}}$	P6_4	PD6_4	1	P6_4S	03h
	CLK1 output	P6_5	PD6_5	1	P6_5S	03h
	SCL1 output	P6_6	PD6_6	1	P6_6S	03h
	TXD1/SDA1 output	P6_7	PD6_7	1	P6_7S	03h
UART2	TXD2/SDA2 output	P7_0 (1)	PD7_0	1	P7_0S	03h
	SCL2 output	P7_1 (1)	PD7_1	1	P7_1S	03h
	CLK2 output	P7_2	PD7_2	1	P7_2S	03h
	$\overline{\text{RTS2}}$	P7_3	PD7_3	1	P7_3S	03h
UART3	$\overline{\text{RTS3}}$	P4_0	PD4_0	1	P4_0S	03h
	CLK3 output	P4_1	PD4_1	1	P4_1S	03h
	SCL3 output	P4_2	PD4_2	1	P4_2S	03h
	TXD3/SDA3 output	P4_3	PD4_3	1	P4_3S	03h
UART4	$\overline{\text{RTS4}}$	P9_4	PD9_4 (2)	1	P9_4S (2)	03h
	CLK4 output	P9_5	PD9_5 (2)	1	P9_5S (2)	03h
	TXD4/SDA4 output	P9_6	PD9_6 (2)	1	P9_6S (2)	03h
	SCL4 output	P9_7	PD9_7 (2)	1	P9_7S (2)	03h

Notes:
1. These ports are N-channel open drain output.
2. The instruction to set this register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupts or DMA transfers should be generated between these two instructions.

Table 4.6 Settings of the Serial Interface When Used as Output Ports (2/2)

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
UART5	TXD5/SDA5 output	P7_6	PD7_6	1	P7_6S	03h
	CLK5 output	P7_7	PD7_7	1	P7_7S	03h
	SCL5 output	P8_0	PD8_0	1	P8_0S	03h
	$\overline{\text{RTS5}}$	P8_1	PD8_1	1	P8_1S	03h
UART6	$\overline{\text{RTS6}}$	P4_4	PD4_4	1	P4_4S	03h
	CLK6 output	P4_5	PD4_5	1	P4_5S	03h
	SCL6 output	P4_6	PD4_6	1	P4_6S	03h
	TXD6/SDA6 output	P4_7	PD4_7	1	P4_7S	03h
UART7	TXD7	P5_4	PD5_4	1	P5_4S	03h
	CLK7 output	P5_5	PD5_5	1	P5_5S	03h
	$\overline{\text{RTS7}}$	P5_7	PD5_7	1	P5_7S	03h
UART8	TXD8	P7_3	PD7_3	1	P7_3S	07h
	CLK8 output	P7_4	PD7_4	1	P7_4S	07h
	$\overline{\text{RTS8}}$	P7_6	PD7_6	1	P7_6S	07h
UART0 special function	STXD0	P6_2	PD6_2	1	P6_2S	04h
UART1 special function	STXD1	P6_6	PD6_6	1	P6_6S	04h
UART2 special function	STXD2	P7_1 (1)	PD7_1	1	P7_1S	04h
UART3 special function	STXD3	P4_2	PD4_2	1	P4_2S	04h
UART4 special function	STXD4	P9_7	PD9_7 (2)	1	P9_7S (2)	04h
UART5 special function	STXD5	P8_0	PD8_0	1	P8_0S	04h
UART6 special function	STXD6	P4_6	PD4_6	1	P4_6S	04h

Notes:
1. This port is N-channel open drain output.
2. The instruction to set this register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupts or DMA transfers should be generated between these two instructions.

Table 4.7 Settings of the Intelligent I/O When Used as Output Ports

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Intelligent I/O group 0	IIO0_0	P1_0	PD1_0	1	P1_0S	05h
	IIO0_1	P1_1	PD1_1	1	P1_1S	05h
	IIO0_2	P1_2	PD1_2	1	P1_2S	05h
	IIO0_3	P1_3	PD1_3	1	P1_3S	05h
	IIO0_4	P1_4	PD1_4	1	P1_4S	05h
	IIO0_5	P1_5	PD1_5	1	P1_5S	05h
	IIO0_6	P1_6	PD1_6	1	P1_6S	05h
	IIO0_7	P1_7	PD1_7	1	P1_7S	05h
Intelligent I/O group 1	IIO1_0	P1_0	PD1_0	1	P1_0S	06h
		P7_3	PD7_3	1	P7_3S	06h
	IIO1_1	P1_1	PD1_1	1	P1_1S	06h
		P7_4	PD7_4	1	P7_4S	06h
	IIO1_2	P1_2	PD1_2	1	P1_2S	06h
		P7_5	PD7_5	1	P7_5S	06h
	IIO1_3	P1_3	PD1_3	1	P1_3S	06h
		P7_6	PD7_6	1	P7_6S	06h
	IIO1_4	P1_4	PD1_4	1	P1_4S	06h
		P7_7	PD7_7	1	P7_7S	06h
	IIO1_5	P1_5	PD1_5	1	P1_5S	06h
		P8_1	PD8_1	1	P8_1S	06h
	IIO1_6	P1_6	PD1_6	1	P1_6S	06h
		P7_0 (1)	PD7_0	1	P7_0S	06h
	IIO1_7	P1_7	PD1_7	1	P1_7S	06h
		P7_1 (1)	PD7_1	1	P7_1S	06h
Intelligent I/O group 2	OUTC2_0/ ISTXD2/ IEOUT	P4_3	PD4_3	1	P4_3S	05h
		P7_0 (1)	PD7_0	1	P7_0S	05h
	OUTC2_1/ ISCLK2	P6_4	PD6_4	1	P6_4S	05h
	OUTC2_2	P7_1 (1)	PD7_1	1	P7_1S	05h

Note:
1. These ports are N-channel open drain output.

Table 4.8 Settings of the A/D Converter When Used as Output Ports

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
A/D converter	AN0_0	P0_0	PD0_0	0	P0_0S	80h
	AN0_1	P0_1	PD0_1	0	P0_1S	80h
	AN0_2	P0_2	PD0_2	0	P0_2S	80h
	AN0_3	P0_3	PD0_3	0	P0_3S	80h
	AN0_4	P0_4	PD0_4	0	P0_4S	80h
	AN0_5	P0_5	PD0_5	0	P0_5S	80h
	AN0_6	P0_6	PD0_6	0	P0_6S	80h
	AN0_7	P0_7	PD0_7	0	P0_7S	80h
	AN2_0	P2_0	PD2_0	0	P2_0S	80h
	AN2_1	P2_1	PD2_1	0	P2_1S	80h
	AN2_2	P2_2	PD2_2	0	P2_2S	80h
	AN2_3	P2_3	PD2_3	0	P2_3S	80h
	AN2_4	P2_4	PD2_4	0	P2_4S	80h
	AN2_5	P2_5	PD2_5	0	P2_5S	80h
	AN2_6	P2_6	PD2_6	0	P2_6S	80h
	AN2_7	P2_7	PD2_7	0	P2_7S	80h
	AN_0	P10_0	PD10_0	0	P10_0S	80h
	AN_1	P10_1	PD10_1	0	P10_1S	80h
	AN_2	P10_2	PD10_2	0	P10_2S	80h
	AN_3	P10_3	PD10_3	0	P10_3S	80h
	AN_4	P10_4	PD10_4	0	P10_4S	80h
	AN_5	P10_5	PD10_5	0	P10_5S	80h
	AN_6	P10_6	PD10_6	0	P10_6S	80h
	AN_7	P10_7	PD10_7	0	P10_7S	80h
	ANEX0	P9_5	PD9_5 (1)	0	P9_5S (1)	80h
	ANEX1	P9_6	PD9_6 (1)	0	P9_6S (1)	80h

Note:
1. The instruction to set this register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupts or DMA transfers should be generated between these two instructions.

Table 4.9 Settings of the D/A Converter When Used as Output Ports

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
D/A converter	DA0	P9_3	PD9_3 (1)	0	P9_3S (1)	80h
	DA1	P9_4	PD9_4 (1)	0	P9_4S (1)	80h

Note:
1. The instruction to set this register should be written immediately after the instruction to set the PRC2 bit in the PRCR register to 1 (write enabled). No interrupts or DMA transfers should be generated between these two instructions.

4.2 Input Function Select Register Settings

Table 4.10 lists the Settings of the Input Function Select Register When Timer A input is Used.
Table 4.11 lists the Settings of the Input Function Select Register When Intelligent I/O Group 0 Two-phase Pulse Input Pin is Used.
Table 4.12 lists the Settings of the Input Function Select Register When Intelligent I/O Group 1 Input Pin is Used.
Table 4.13 lists the Settings of the Input Function Select Register When Intelligent I/O Group 1 Two-phase Pulse Input Pin is Used.
Table 4.14 lists the Settings of the Input Function Select Register When Intelligent I/O Group 2 Input Pin is Used.

Table 4.10 Settings of the Input Function Select Register When Timer A input is Used

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Timer A input pin switch bit	TA0OUT input	P3_0	PD3_0	0	IFS00	0
		P7_0 (1)	PD7_0	0		1
	TA1OUT input	P3_2	PD3_2	0		0
		P7_2	PD7_2	0		1
	TA1IN	P3_3	PD3_3	0		0
		P7_3	PD7_3	0		1
	TA2OUT input	P3_4	PD3_4	0		0
		P7_4	PD7_4	0		1
	TA2IN	P3_5	PD3_5	0		0
		P7_5	PD7_5	0		1
	TA3OUT input	P3_1	PD3_1	0		0
		P7_6	PD7_6	0		1
	TA4OUT input	P3_6	PD3_6	0		0
		P8_0	PD8_0	0		1
	TA4IN	P3_7	PD3_7	0		0
		P8_1	PD8_1	0		1

Note:
1. This port is N-channel open drain output.

Table 4.11 Settings of the Input Function Select Register When Intelligent I/O Group 0 Two-phase Pulse Input Pin is Used

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Intelligent I/O group 0 two-phase pulse input pin switch bit	UD0A	P8_0	PD8_0	0	IFS23 and IFS22	00b
		P7_6	PD7_6	0		01b
		P3_0	PD3_0	0		10b
		P3_0	PD3_0	0		11b
	UD0B	P8_1	PD8_1	0		00b
		P7_7	PD7_7	0		01b
		P3_1	PD3_1	0		10b
		P3_1	PD3_1	0		11b
	UD0Z	P8_3 ($\overline{\text{INT1}}$)	PD8_3	0		00b
		P8_2 ($\overline{\text{INT0}}$)	PD8_2	0		01b
		P8_3 ($\overline{\text{INT1}}$)	PD8_3	0		10b
		P8_2 ($\overline{\text{INT0}}$)	PD8_2	0		11b

Table 4.12 Settings of the Input Function Select Register When Intelligent I/O Group 1 Input Pin is Used

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Intelligent I/O group 1 two-phase pulse input pin switch bit	IIO1_0 input	P7_3	PD7_3	0	IFS25	0
		P1_0	PD1_0	0		1
	IIO1_1 input	P7_4	PD7_4	0		0
		P1_1	PD1_1	0		1
	IIO1_2 input	P7_5	PD7_5	0		0
		P1_2	PD1_2	0		1
	IIO1_3 input	P7_6	PD7_6	0		0
		P1_3	PD1_3	0		1
	IIO1_4 input	P7_7	PD7_7	0		0
		P1_4	PD1_4	0		1
	IIO1_5 input	P8_1	PD8_1	0		0
		P1_5	PD1_5	0		1
	IIO1_6 input	P7_0 (1)	PD7_0	0		0
		P1_6	PD1_6	0		1
	IIO1_7 input	P7_1 (1)	PD7_1	0		0
		P1_7	PD1_7	0		1

Note:
1. These ports are N-channel open drain output.

Table 4.13 Settings of the Input Function Select Register When Intelligent I/O Group 1 Two-phase Pulse Input Pin is Used

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Intelligent I/O group 1 two-phase pulse input pin switch bit	UD1A	P8_0	PD8_0	0	IFS27 and IFS26	00b
		P7_7	PD7_7	0		01b
		P3_0	PD3_0	0		10b
		P3_0	PD3_0	0		11b
	UD1B	P8_1	PD8_1	0		00b
		P7_7	PD7_7	0		01b
		P3_1	PD3_1	0		10b
		P3_1	PD3_1	0		11b
	UD1Z	P8_3 (INT1)	PD8_3	0		00b
		P8_2 (INT0)	PD8_2	0		01b
		P8_3 (INT1)	PD8_3	0		10b
		P8_2 (INT0)	PD8_2	0		11b

Table 4.14 Settings of the Input Function Select Register When Intelligent I/O Group 2 Input Pin is Used

Function	Output Port	Port	Port Direction Register		Function Select Register	
			Direction bit	Setting value	Register	Setting value
Intelligent I/O group 2 two-phase pulse input pin switch bit	ISCLK2 input	P6_4	PD6_4	0	IFS31 and IFS30	00b
		P6_4	PD6_4	0		11b
	ISRXD2/IEIN	P7_1 (1)	PD7_1	0		00b
		P4_2	PD4_2	0		11b

Note:
1. This port is N-channel open drain output.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
The sample program shows examples of setting programmable I/O ports to output ports after setting the MCU clock.
The sample program shows the following:

- Set the P0_0 as an output port (unprotected port)
- Set the P9_3 as an output port (protected port)

Refer to the user's manual for details on the MCU clock settings.

6. Reference Documents

User’s Manual
R32C/111 Group User’s Manual Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/111 Group Configuring Function Select Register

Rev.	Date	Description	
		Page	Summary
1.00	May 28, 2010	-	First Edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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