Application Note

Potentiometer Controlled by an Encoder

AN-CM-320

Abstract

This application note illustrates how to use the SLG47004 to control a potentiometer with an encoder and to implement an adjustable voltage divider based on it.
The application note comes complete with design files which can be found in the References section.

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1 Terms and Definitions

CLK	Clock
DFF	D Flip-Flop

2 References

For related documents and software, please visit:

GreenPAK™ Programmable Mixed-Signal Products | Renesas
Download our free GreenPAK Designer software [1] to open the .gp file [1] and view the proposed circuit design. Use the GreenPAK development tools [2] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [3] featuring design examples, as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-320 Potentiometer Controlled by Encoder.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

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3 Introduction

There are a variety of applications where a mechanical potentiometer is part of a user control interface. These mechanical potentiometers can be changed to more updated and reliable encoder controlled elements and digital rheostats, being components that change electrical parameters of the signal.

SLG47004 is a perfect solution that combines two digital rheostats and configurable logic to process the encoder information. This combination allows to implement many designs: a regulated power supply, an amplifier with a tunable gain, and others. In addition, the presence of digital logic allows determining the speed of rotation of the encoder. This approach is shown in Figure 1.

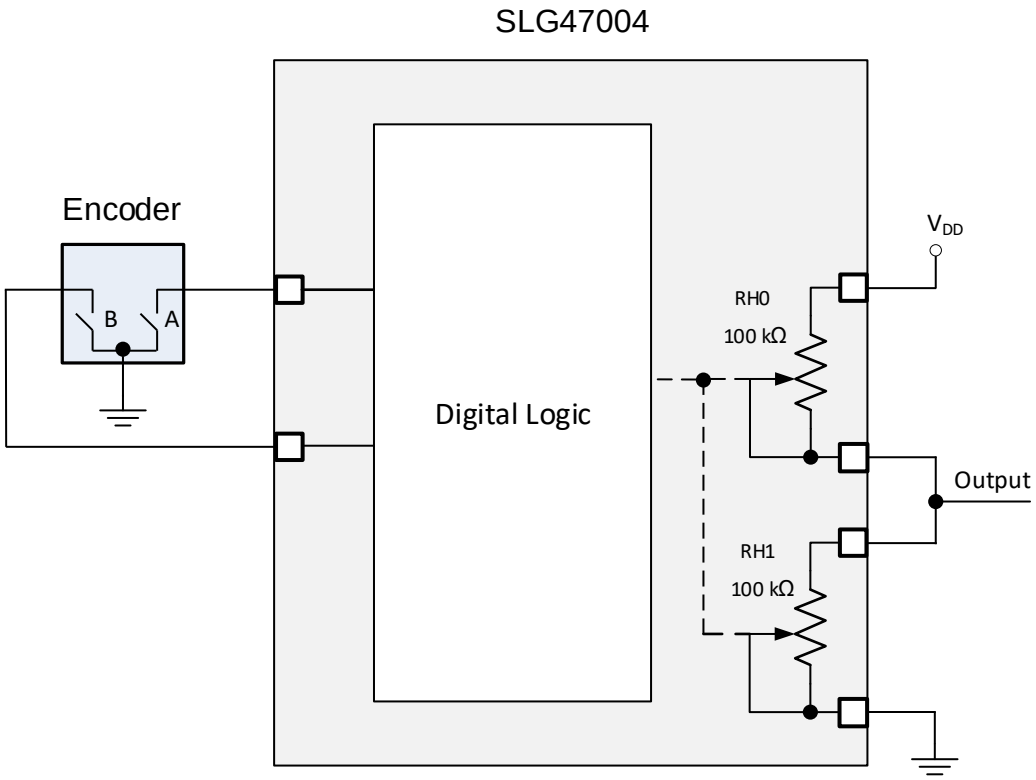

Figure 1: General Schematic of a Voltage Divider Controlled by the Encoder

4 System Overview

Figure 2 shows the internal design based on the SLG47004.

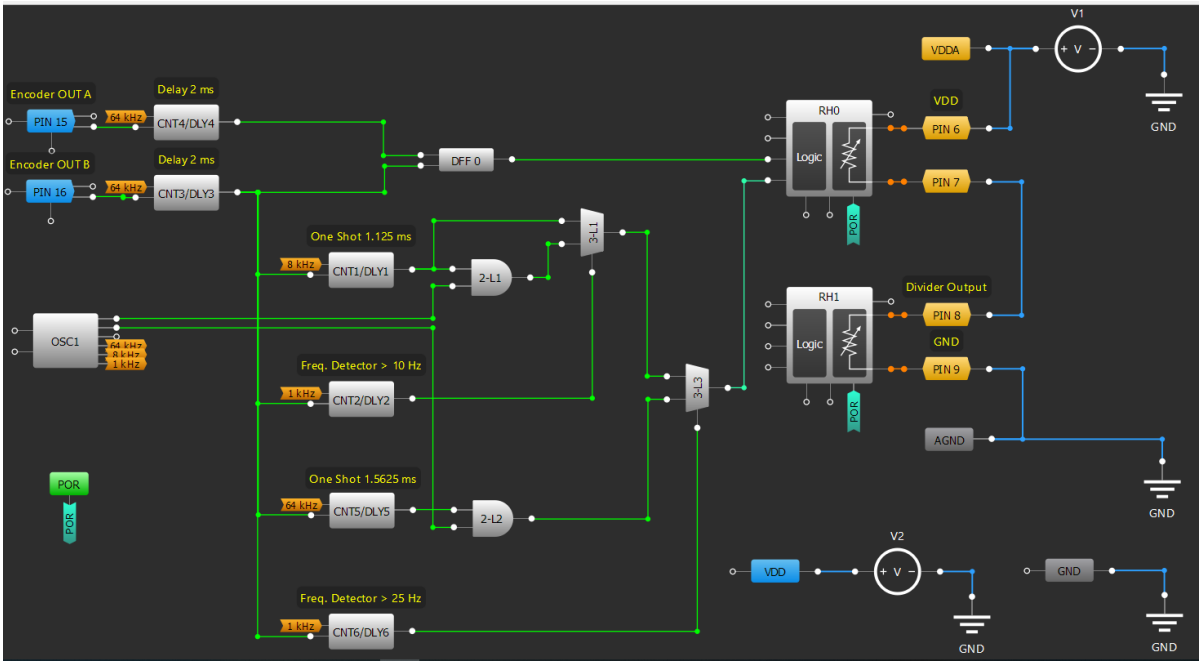

Figure 2: GreenPAK Designer Project

An incremental encoder generates its A and B output signals which are used to change digital rheostats resistance. Rheostats form the potentiometer and allow to implement the adjustable voltage divider to regulate an output voltage.

At any particular time, the phase difference between the A and B signals will be positive or negative depending on the encoder's direction of movement.

A speed determination function is built from Frequency Detectors, One Shots and Multiplexers.

In this application note the EC11 encoder was used. The encoder produces noisy output oscillations due to switch bounce. To eliminate that noise, 2 mS delays were used. Please note that this delay is adjusted for the EC11 encoder (according to its datasheet). For other encoders the delay value should be assessed accordingly.

5 Functional Block Architecture

5.1 Digital Logic Description

5.1.1 Determining the Encoder Direction

At first, Delay macrocells delay both edges of the encoder output signals for 2 mS. Delay macrocells work like a deglitch filter to eliminate switch bouncing. Delayed signal B appears on DLY inputs of One Shots and Frequency Detectors, and CLK input of DFF. Delayed signal A appears on D input of DFF. When the encoder disk is rotating in a clockwise direction signal A leads signal B and DFF output is High, and when the disk is rotating in a counterclockwise direction signal B leads signal A and DFF output is Low. So DFF can determine the direction of rotation. High or Low signal on Rheostat Up/Down input determines if internal counter's value increases or decreases for each pulse at CLK input.

A timing diagram for the clockwise encoder rotation is shown in Figure 3 and for the counterclockwise encoder rotation in Figure 4.

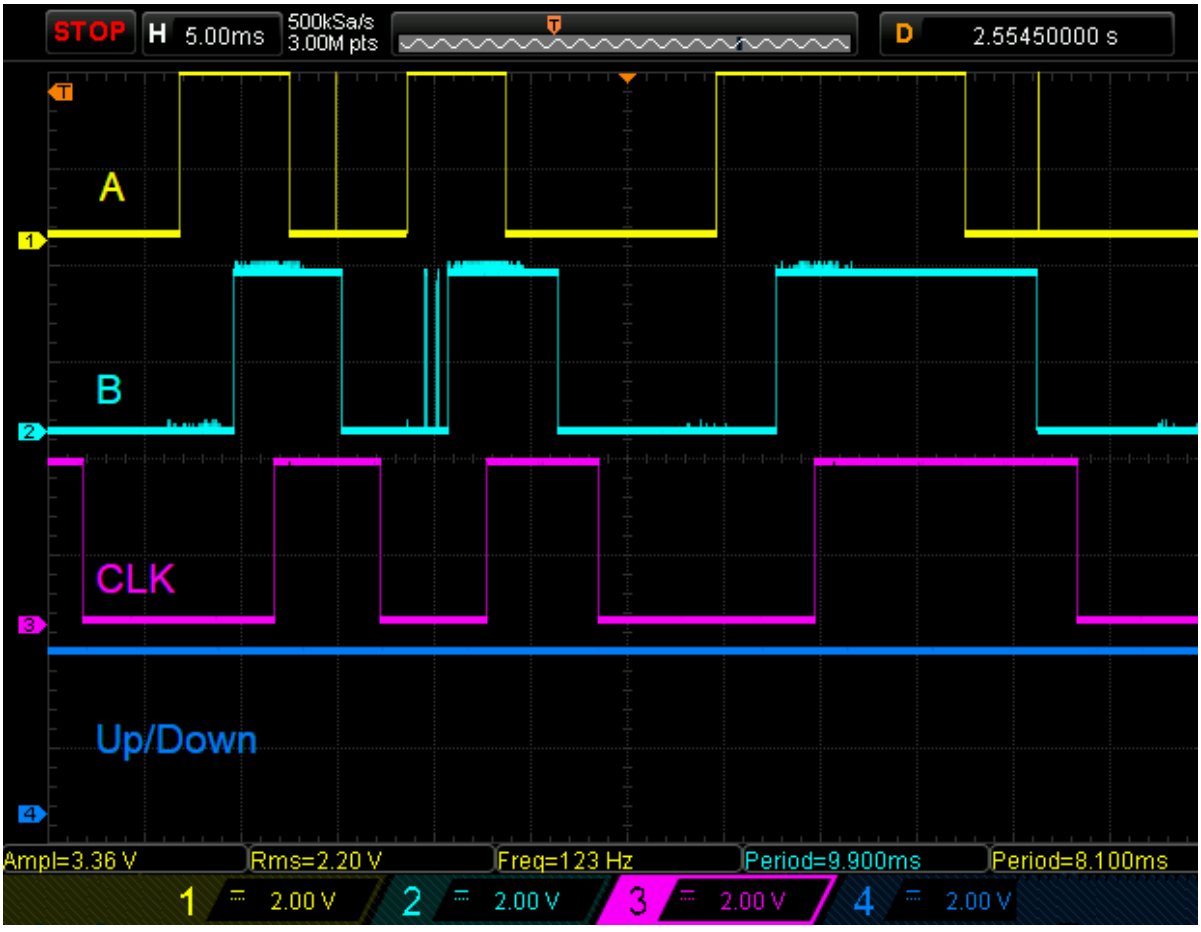

Figure 3: Timing Diagrams for Clockwise Encoder Rotation

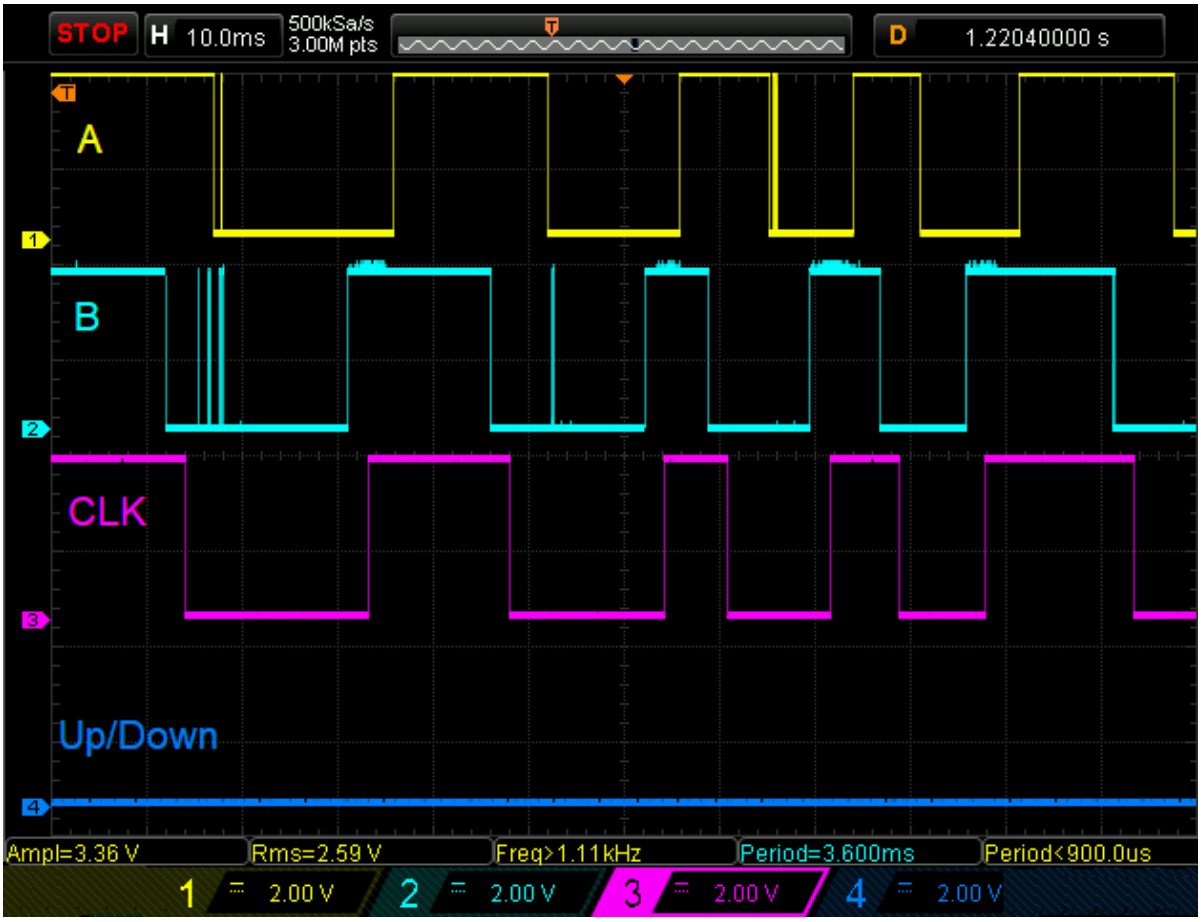

Figure 4: Timing Diagrams for Counterclockwise Encoder Rotation

5.1.2 Determing the Encoder Speed

The SLG47004 has 10-bit digital rheostats, which in turn allows implementation of 1024 regulation steps. The adjustable voltage divider has 3 regulation modes. The user can change output signal with step = 1 digital code (mode 1), step = 10 digital codes (mode 2) and step = 100 digital codes (mode 3). To have 3 modes was used 2 frequency detectors. The first mode is assigned to adjust the output signal smoothly and accurately. It activates when a user adjusts a knob with a frequency less than 10 Hz. The second mode activates when the frequency is greater than 10 Hz, but less than 25 Hz. The last one works when the frequency is greater than 25 Hz.

One Shots set time intervals for the required number of pulses.

Digital multiplexers provide the passage of either one, or ten, or hundred pulses on CLK input of rheostat according to frequency detectors outputs.

5.1.3 Detents and Pulses per Revolution

The encoder with a different number of pulses and detents (positions) was used in this project. With 15 pulses, you have two detents per full pulse. This means that for every pulse (or cycle) in the rotary encoder there are two detents: rising edge of the pulse (one change) and falling edge of the pulse (another change). If your rotary encoder has one detent per pulse, then it has two changes for every pulse. For this type of encoder, the design remains the same, except for Frequency Detectors and One Shots settings. In their settings, Edge Select should be set "Falling" or "Rising". In encoders where the number of pulses and detents do not match, Edge Select should be set to "Both".

5.2 Potentiometer Mode

For this design we used digital rheostats in potentiometer mode. This mode allows two 2-pin rheostats to work as one 3-pin potentiometer. When this mode is active (register [917] = 1), the user changes the value of the RH0 internal counter. In this mode, the value of the RH1 counter is the inverted value of the RH0 counter. Note that the RH0_B pin and the RH1_A pin must be connected externally.

5.3 Macrocells Settings

3-bit LUT1 and 3-bit LUT3 settings: Standard Gate - Multiplexer.

Table 1: 2-bit LUTs Settings

IN1	IN0	LUT1 OUT	LUT2 OUT
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

Table 2: DFF Settings

Properties	DFF0
Type	DFF/LATCH
Mode	DFF
Initial Polarity	Low
Q Output Polarity	Inverted (nQ)

Table 3: PINs Settings

Properties	PINs 6, 7, 8, 9	PINs 15, 16
I/O Selection	Analog Input/Output	Digital Input
Input Mode	Analog Input/Output	Digital In with Schmitt Trigger
Output Mode	Analog Input/Output	None
Resistor	Floating	Pull Up
Resistor Value	Floating	10 kΩ

Table 4: OSC Settings

Properties	OSC1
Control Pin Mode	Power Down
OSC Power Mode	Auto Power On
Clock Selector	OSC
OSC1 Frequency	2.048 MHz
'CLK' Pre-divider	4
OUT0 Second Divider	64

Properties	OSC1
OUT1 Second Divider	8

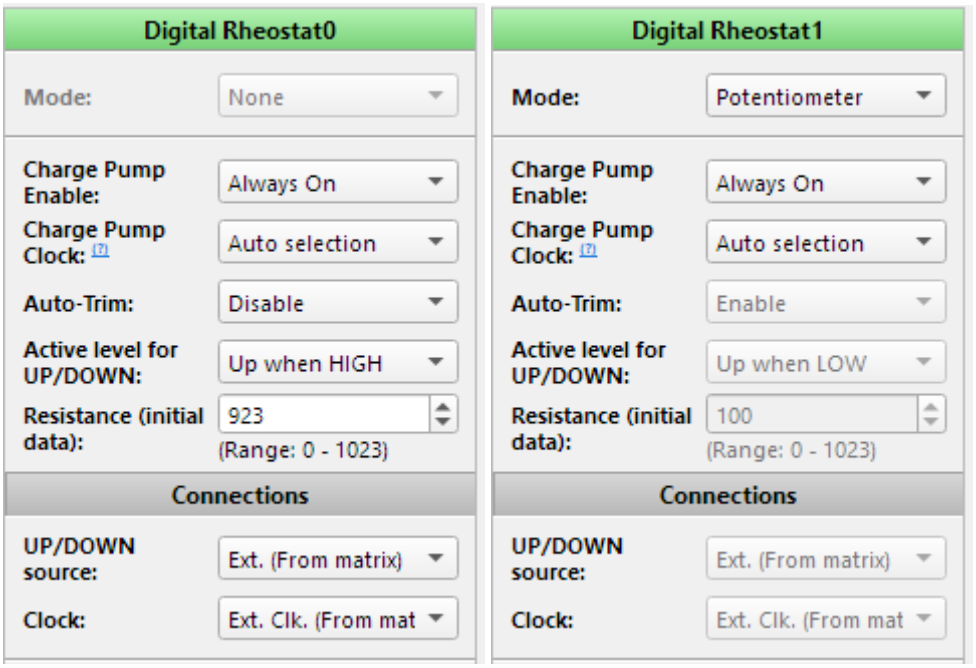

Figure 5: Digital Rheostats Settings

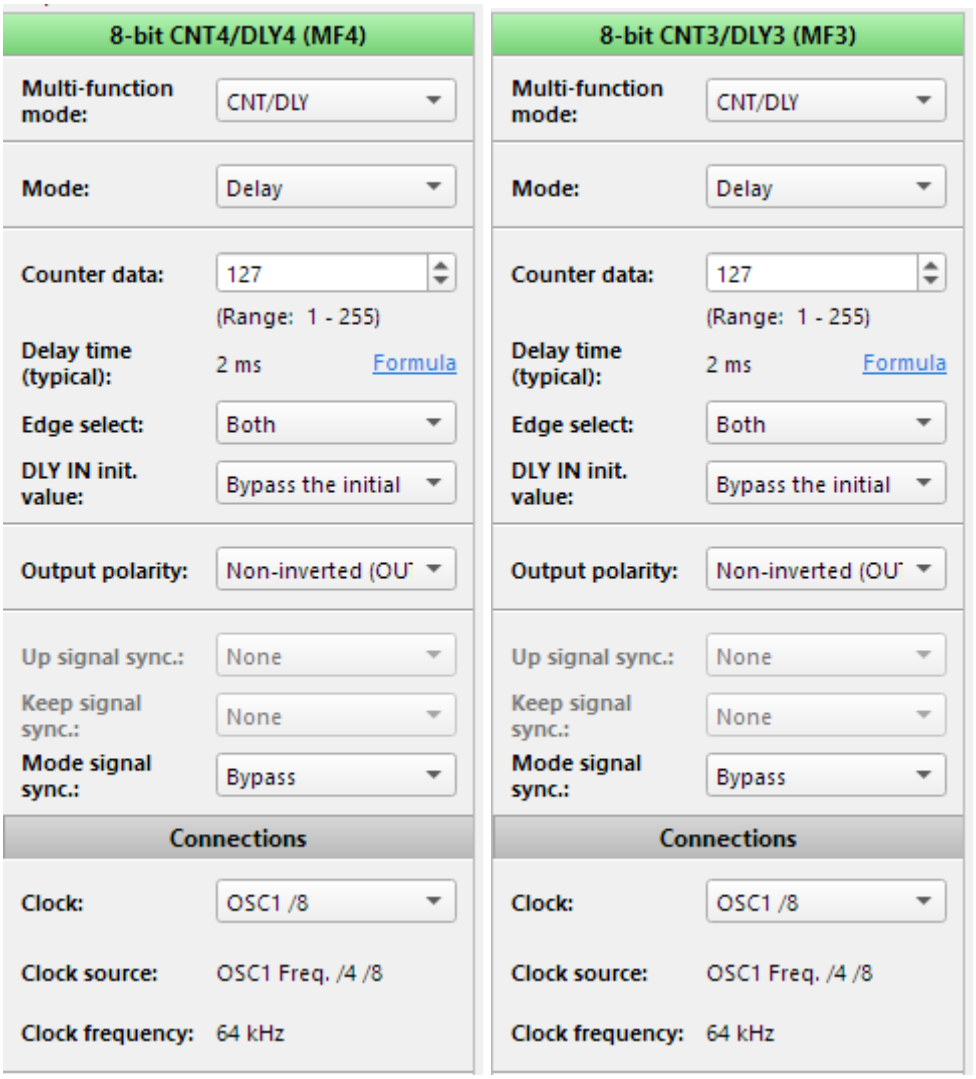

Figure 6: Delays Settings

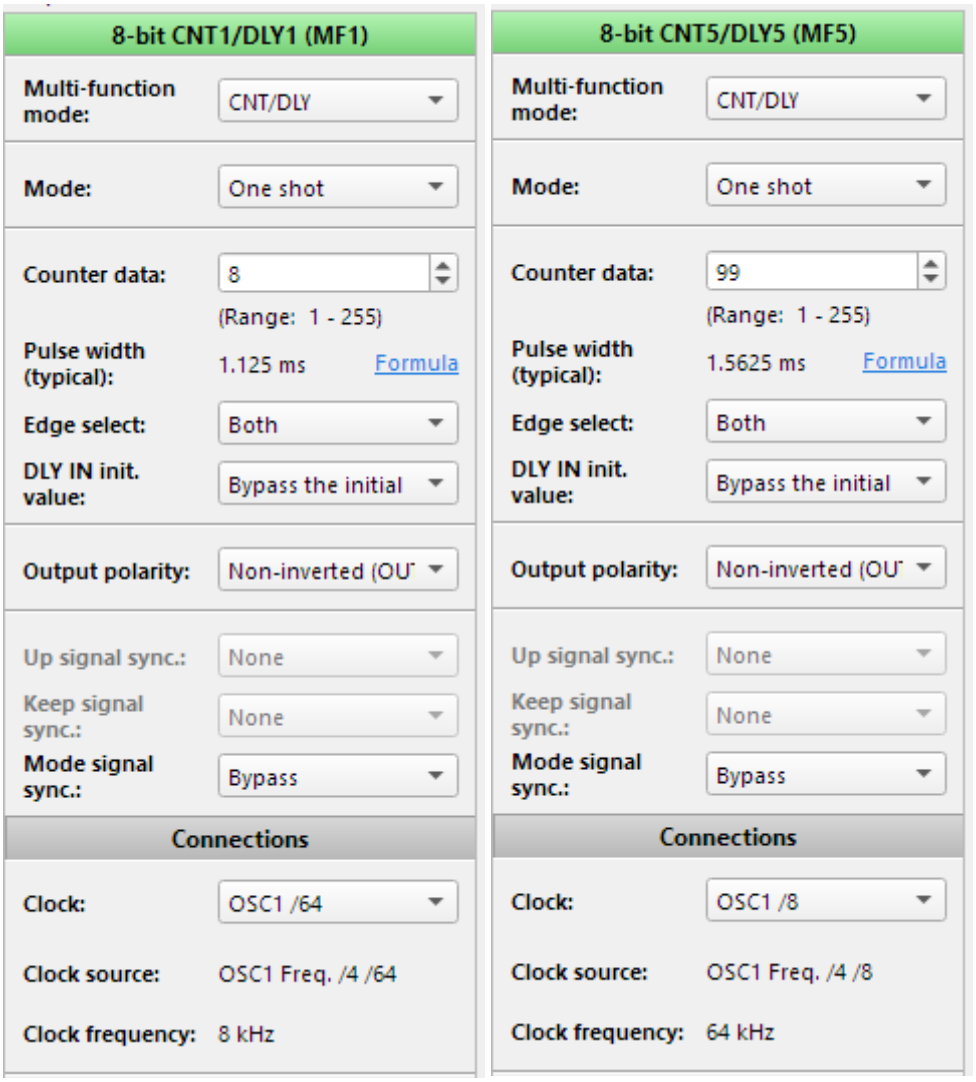

Figure 7: One Shots Settings when the Number of Pulses and Detents Do Not Match

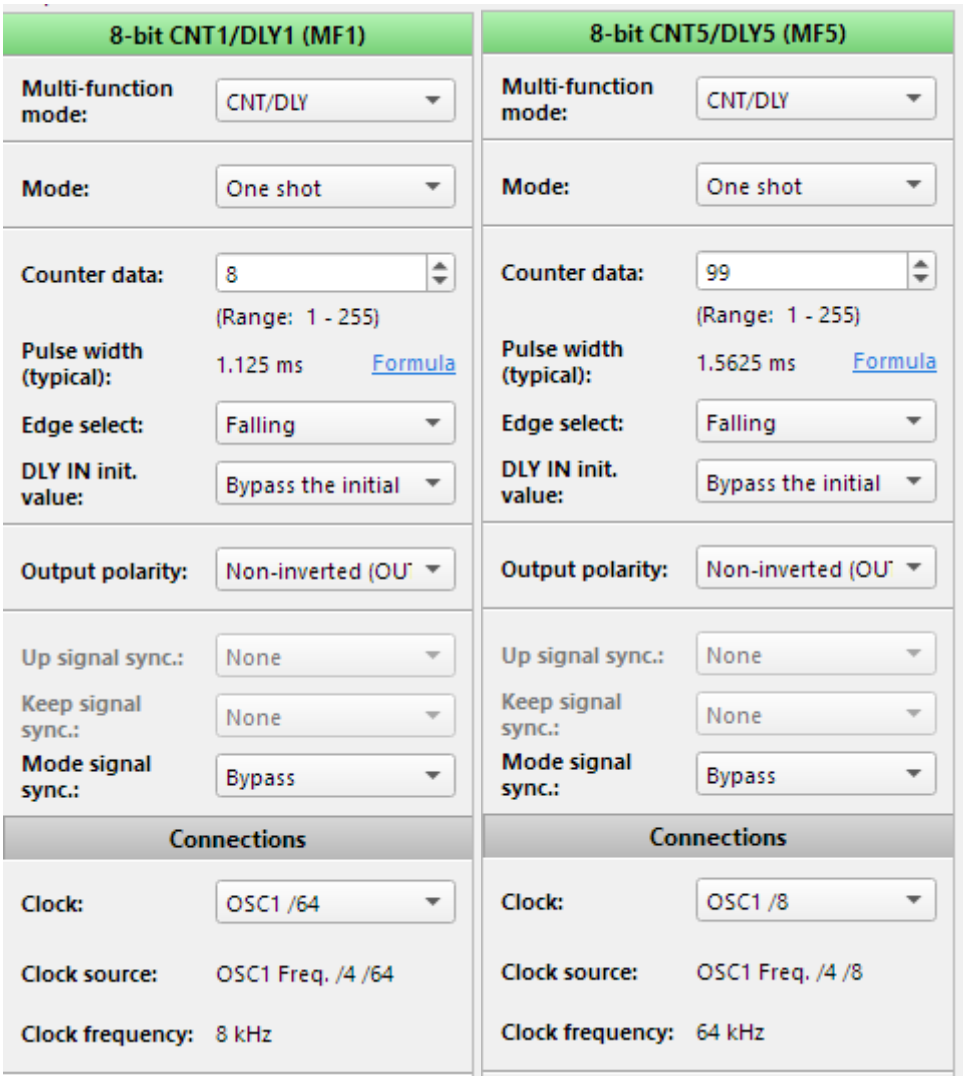

Figure 8: One Shots Settings when the Number of Pulses and Detents Match

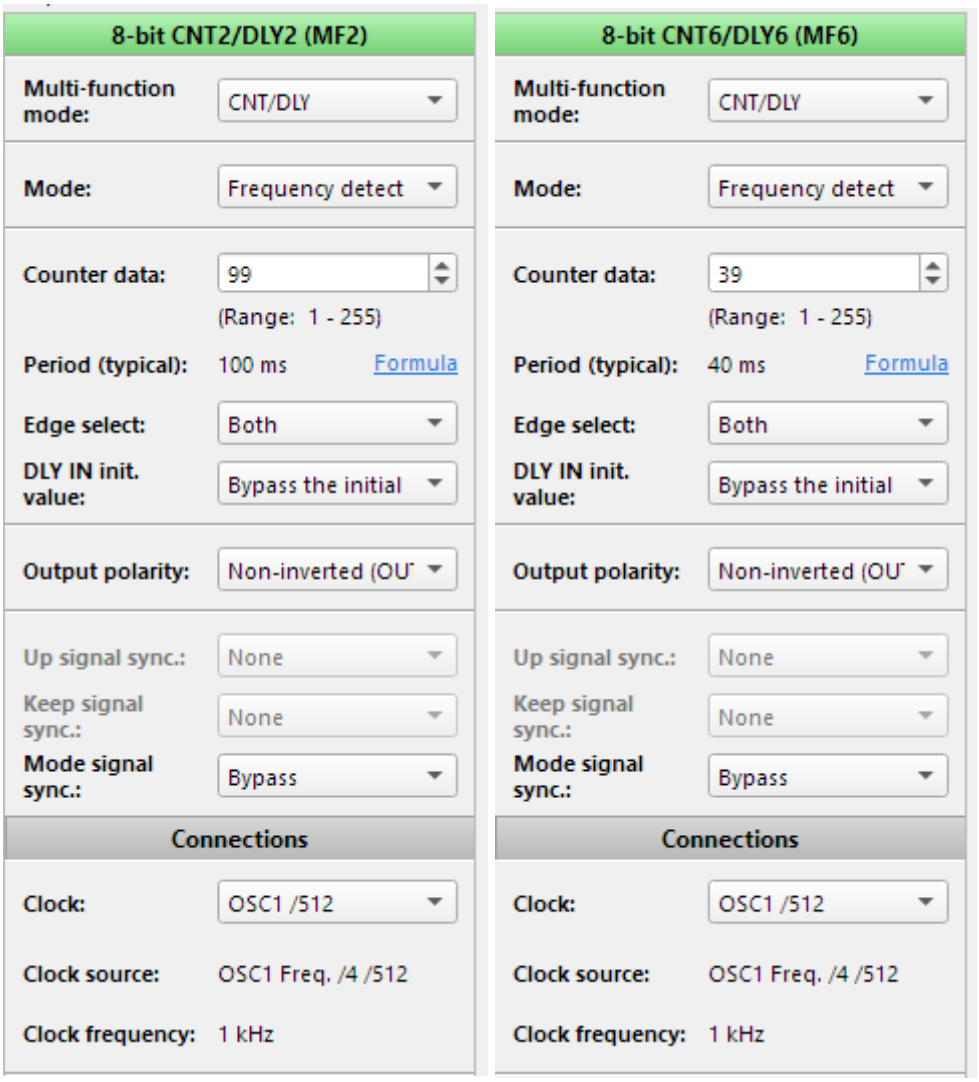

Figure 9: Frequency Detectors Settings when the Number of Pulses and Detents Do Not Match

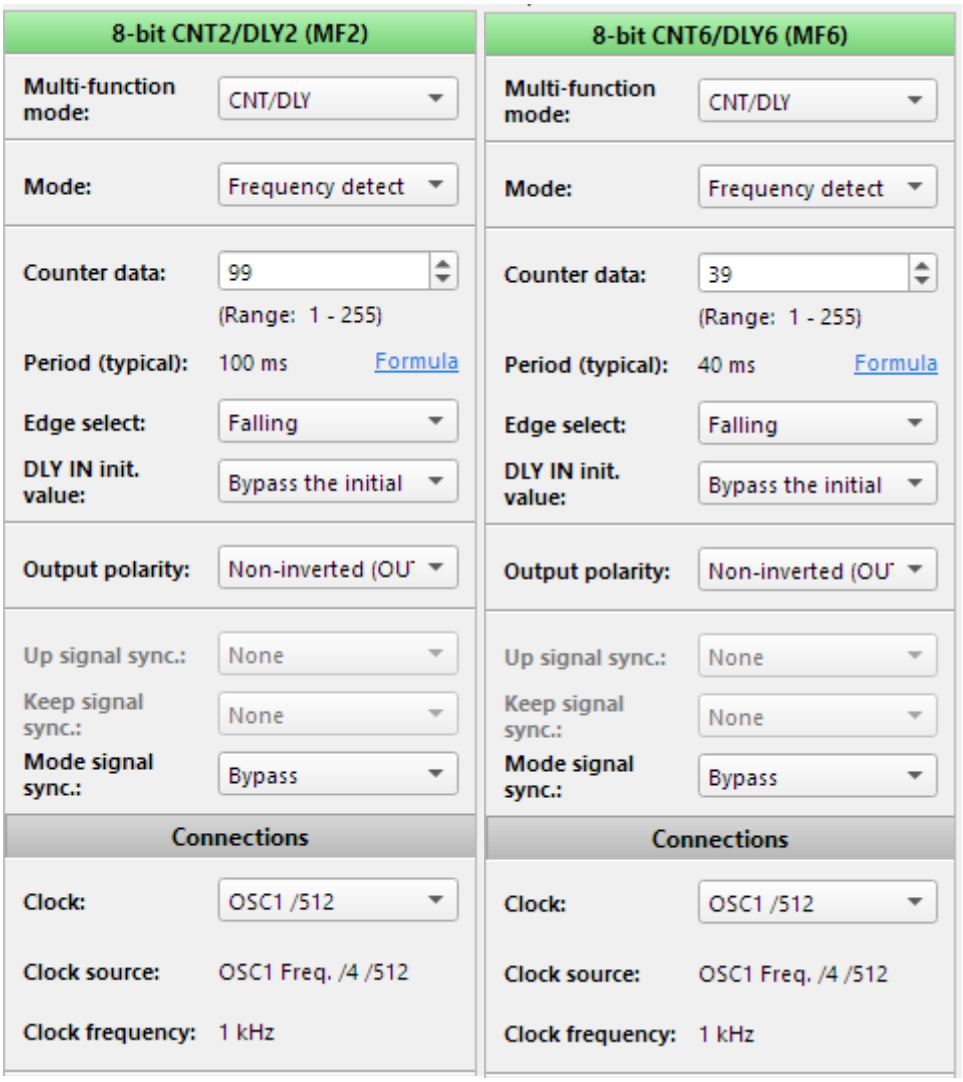

Figure 10: Frequency Detectors Settings when the Number of Pulses and Detents Match

Conclusions

The SLG47004 has two digital rheostats which allow implementing a myriad of useful applications. A case in point is using digital rheostats to replace an analog potentiometer with the help of a modern encoder. This application note illustrates how to use the SLG47004 to implement the adjustable voltage divider which is a versatile solution and can be applied to an adjustable power supply, amplifier's gain control, and others. This solution is cost-effective and with low energy consumption.

Revision History

Revision	Date	Description
1.0	25-Aug-2021	Initial Version

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