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M32C/81,82,83 Group

Clock synchronous serial communication by using Intellingent I/O group 0,1 external clock

1. Abstract

This application note describes the procedures of clock synchronous serial communication by using Intelligent I/O group 0,1 external clock.

2. Introduction

This application note is applied to the M32C/83 group microcomputer.
This program can also be used when operating other microcomputers within M16C family, provided they have the same SFR (Special Function Registers) as the M32C/83 group. However, some functions may have been modified. Refer to the User's Manual for details. Use functions covered in this Application Note only after careful evaluation.

3. Detailed description

This application example offers the features of the clock asynchronous serial communication by using M32C/83 group Intelligent I/O group 1 shown in Table 1.
The transmit data is output from the pin ISTxD1. The transfer clock is input from the pin ISCLK1, and the receive data is input from the pin ISRxD1.
Execute the operation to initialize the Intelligent I/O group 1 if the external clock stops during the communication.

Table 1 Clock synchronous serial I/O option features and selected features

Item	Definition	Selection
Transfer clock	Internal clock	
	External clock	Yes
Transfer format	LSB First	Yes
	MSB First	
TxD,RxD output polarity select	Not reverse	Yes
	Reverse	
Transfer interrupt factor	When G1TB register becomes empty	
	When the transmission is completed	Yes

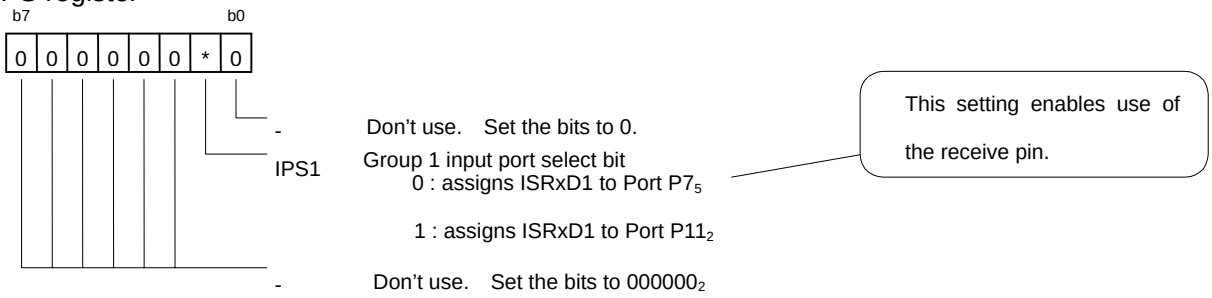
(Note) The communication setting must be operated when the port ISCLK1 is in "H".

3.1 Register setting

3.1.1 The procedures of the port setting

This section describes how to set the port to use for Intelligent I/O group 1. Refer to the M32C/83 group Hardware Manual for the details of each register.

(1) IPS register



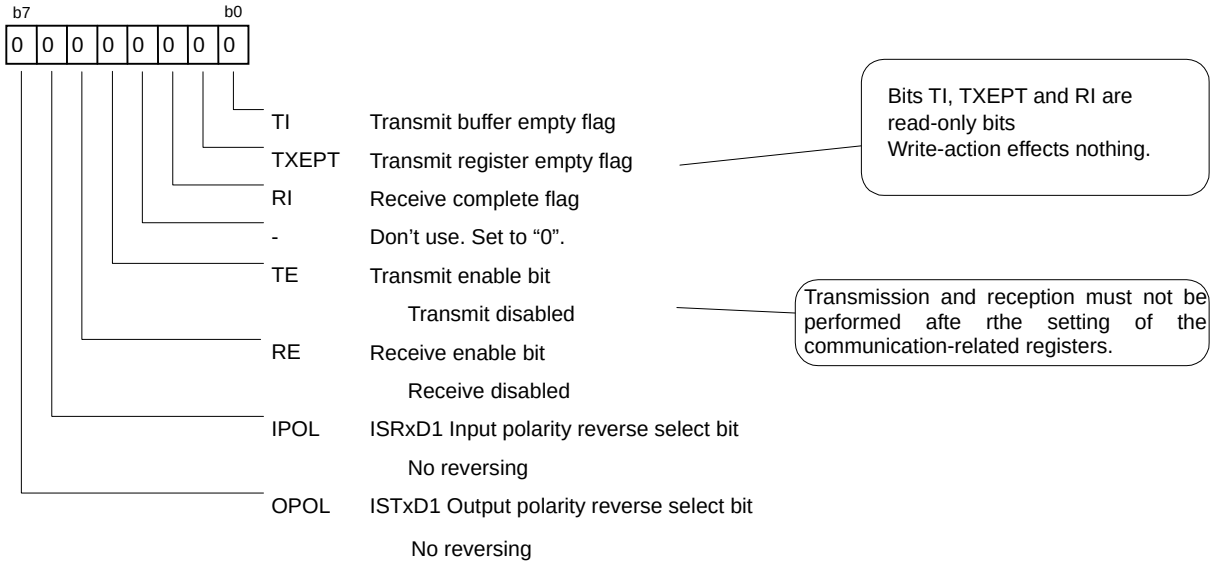
(2) PSC register, PSLa register (a=0 to 3), PSb register (b=0 to 3, 5 to 9)

3.1.2 Intelligent I/O setting

The setting procedures and the setting value will be described to enable the operation defined in “Section 3. Detailed description”. The setting must be taken place when the port ISCLK1 is in “H”.

Refer to the M32C/83 group Hardware Manual for details of each register.

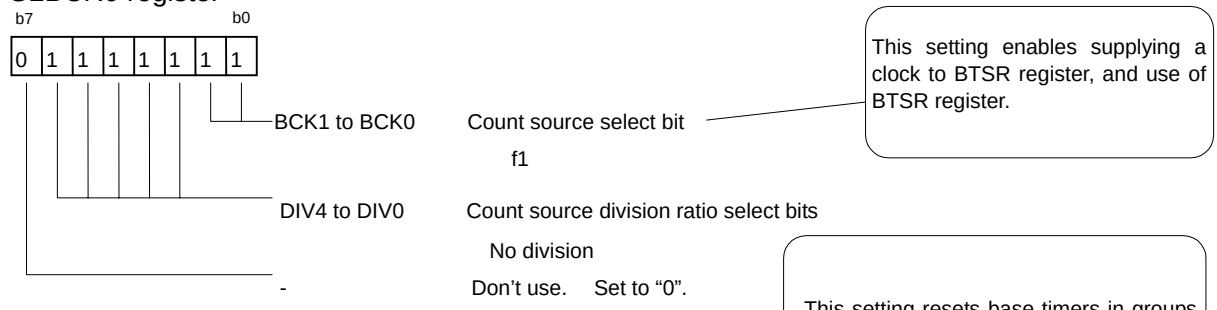
(1) G1CR register



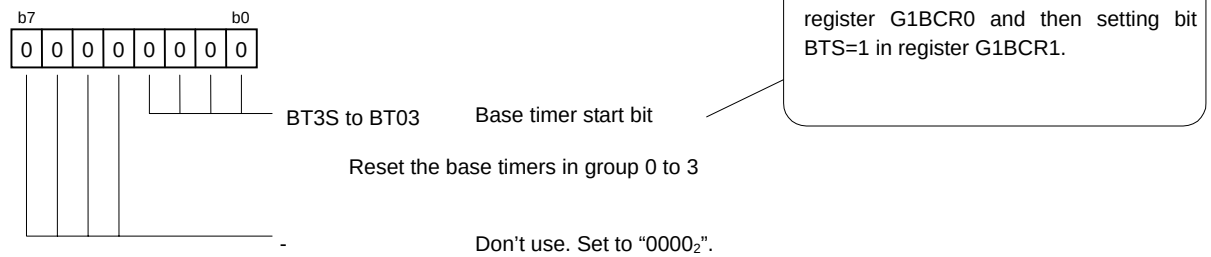
(2) Interrupt disabled

Set the I flag to “0”, or set the bits ILV2 - ILVL0 to “000_2” in the registers IIO2IC - IIO3IC where the interrupt request of the intelligent I/O is assigned.

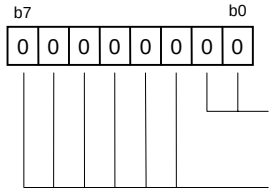
(3) G2BCR0 register



(4) BTSR register



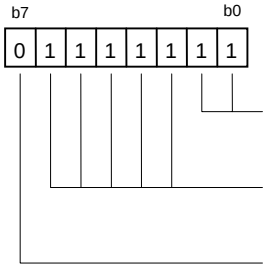
(5) G2BCR0 register



Count source select bit
No clock
Don't use. Set to 000000_2.

If group 2 and register BTSR are not used, disable supplying a clock to group 2.

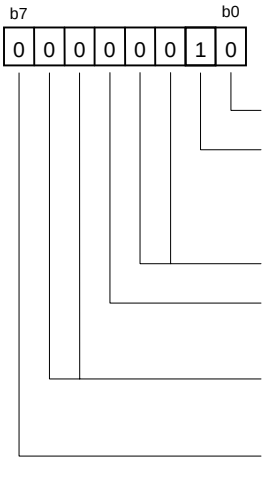
(6) G1BCR0 register



BCK1 to BCK0 Count source select bit
f1
DIV4 to DIV0 Count source division ratio select bit
No division
- Don't use. Set to 0.

This setting enables supplying a clock to registers that are defined instep (7) thru (13). Set this register to 01111111_2 before going to the following steps.

(7) G1BCR1 register

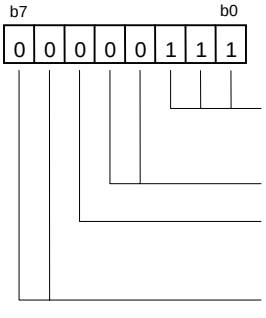


- Don't use. Set to 0.
RST1 Base timer reset cause select bit 1
Reset base timer when the base timer content matches to the content of register G1PO0
- Don't use. Set to 00_2.
BTS Base timer start bit
Reset base timer
UD1 to UD0 Up-down control bit
Up-count mode
- Don't use. Set to 0.

This register is used for generating the transfer clock. Set the bit RTS1 to 1 (The base timer is reset when the base timer content matches to the content of register G1PO0).

After setting the group 1 intelligent I/O relating register, set the BTS bit to "1" (base timer count start)

(8) G1POCR0 register

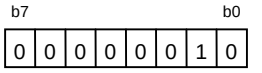


MOD2 to MOD0 Operation mode select bit
Select the output of the communication function
- Don't use. Set to 00_2.
RLD The register G1PO0 reload timing select bit
Reload when the register is written.
- Don't use. Set to "0".

This setting selects pin ISTxD1 to transmit data.

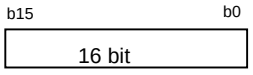
The setting configures the reload action occurs at the same time data is written to register G1PO0

(9) G1POCR3 register



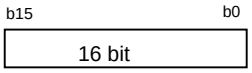
MOD2 to MOD0	Operation mode select bit
	Select phase-delayed waveform output mode
-	Don't use. Set to "0".
IVL	Output initial value select bit
	Output "0" as an initial value
RLD	The register G1PO0 reload timing select bit
	Reload when the register is written.
INV	Inverted waveform output function select bit
	No inverted waveform output

(10) G1PO0 register



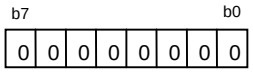
Set to 0001_{16}

(11) G1PO3 register



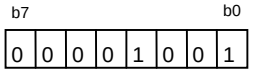
Set to 0001_{16}

(12) G1FS register



FSC1	Channel 0 time measurement, wave generation select bit
	Select the wave generation function.
-	Don't use. Set to "00_2".
FSC3	Channel 3 time measurement, wave generation select bit
	Select the wave generation function.
-	Don't use. Set to "00_2".

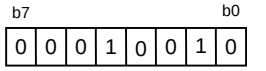
(13) G1FE register



IFE1	Channel 0 function enable bit
	Enables Channel 0 function
-	Don't use. Set to "00_2".
IFE3	Channel 3 function enable bit
	Enables Channel 3 function.
-	Don't use. Set to "00_2".

Set the bit IFE of un-used Channels to 0.

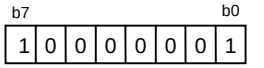
(14) G1BCR1 register



BTS Base timer start bit

Enables base timer to start counting

(15) G1MR register



GMD1 to 0 Communication mode select bit

Selects clock synchronous serial I/O mode

CKDIR Internal/External clock select bit

Selects internal clock

\- Don't use. Set to "000_2".

UFORM Transfer format select bit

LSB first

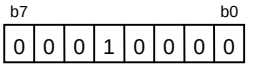
IRS Transmit interrupt cause select bit

Completes transmit (TXEPT=1)

Select a clock synchronous serial mode.

Select an internal clock.

(16) G1CR register



\- Don't use. Set to "0000_2".

TE Transmit enable bit

Enables the transmit

RE Receive enable bit

Disables the receive

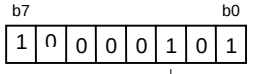
\- Don't use. Set to "00_2".

This setting enables the transmit to initialize the transmit buffer.

(17) Wait until the bit TXEPT = "1" (Transmit completes) in the register G1CR.

Outputs all data left in the transmit buffer by using the internal clock. (Initialization of the transmit buffer.)

(18) G1MR register

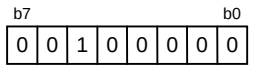


CKDIR Internal / external clock select bit

Selects external clock

Select the external clock

(19) G1ERC register



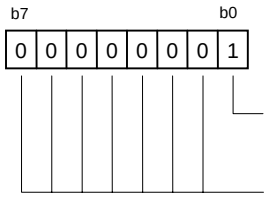
\- Don't use. Set to "00000_2".

RSHTE Receive shift operation enable bit

Enables receive shift operation

\- Don't use. Set to "00_2".

(20) IIO3IE register



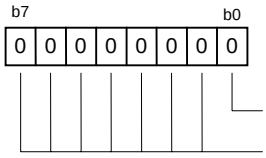
IRLT Interrupt request select bit
Selects the interrupt request bit

bit7 to 1 Interrupt enable bit 7-1
Set to "0000000_2"

Set the transfer interrupt in the steps (20) – (23)

Don't set the bit IRLT and the bit 7-1 to "1" at the same time.

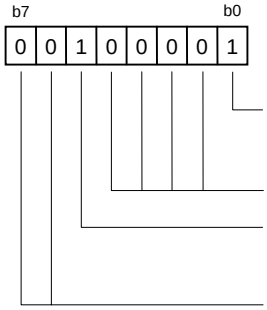
(21) IIO3IR register



Don't use. Set to "0".
Initialize the interrupt request register

The register must be set to 00_{16}.
If the register holds a value other than 00_{16}, the bit IR in the register IIO3IC will not be set to "1" when an interrupt request is generated.

(22) IIO3IE register



IRLT Interrupt request select bit
Selects the interrupt request bit

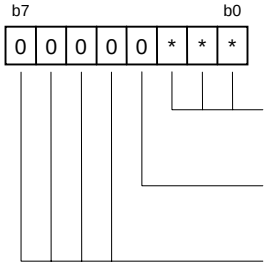
- Don't use. Set to "0000_2".

SIOiTE Transmit interrupt of intelligent I/O group 1
Enables the interrupt request

- Don't use. Set to "00_2".

Set the interrupt request bit not used for the interrupt to "0"

(23) IIO3IC register



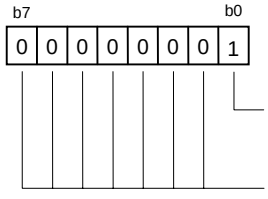
ILVL2 to ILVL0 Interrupt priority level select bit

IR Interrupt request bit
Interrupt unrequested

- Don't use. Set to "000_2".

Set the receive in the steps (24) to (27).

(24) IIO2IE register

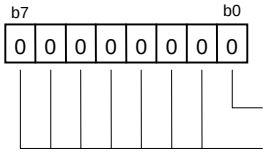


IRLT Interrupt request select bit
Selects interrupt request

bit7 - 1 Interrupt enable bit 7-1
Set to "0000000_2"

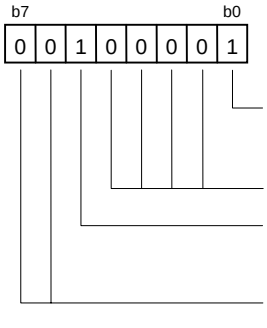
Don't set the bit IRLT and the bit 7-1 to "1" at the same time.

(25) IIO2IR register



The register must be set to 00_{16}.
If the register holds a value other than 00_{16}, the bit IR in the register IIO3IC will not be set to "1" when an interrupt request is generated.

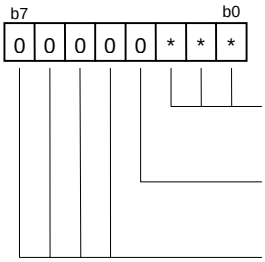
(26) IIO2IE register



IRLT Interrupt request select bit
Uses interrupt request for an interrupt
\- Don't use. Set to "0000$_2$".
SIOiRE Transmit interrupt of intelligent I/O group 1
Enables the interrupt request.
\- Don't use. Set to "00$_2$".

Set the interrupt request bit not used for the interrupt to "0"

(27) IIO2IC register

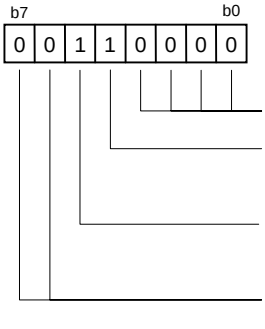


ILVL2 to ILVL0 Interrupt priority level select bit
Selects the interrupt priority level.
IR Interrupt request bit
No Interrupt requested
\- Don't use. Set to "0000$_2$".

(28) Interrupt enabled (I flag ="1")

When using the interrupt, set I flag to "1" before setting the register for enabling receive and transmit operation.

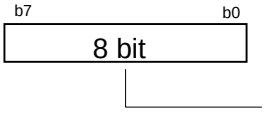
(29) G1CR register



\- Don't use. Set to "0000$_2$".
TE Transmit enable bit
Enables the transmission
RE Receive enable bit
Enables the reception
\- Don't use. Set to "00$_2$".

This register enables the transmit and receive operation after the communication related register is set.

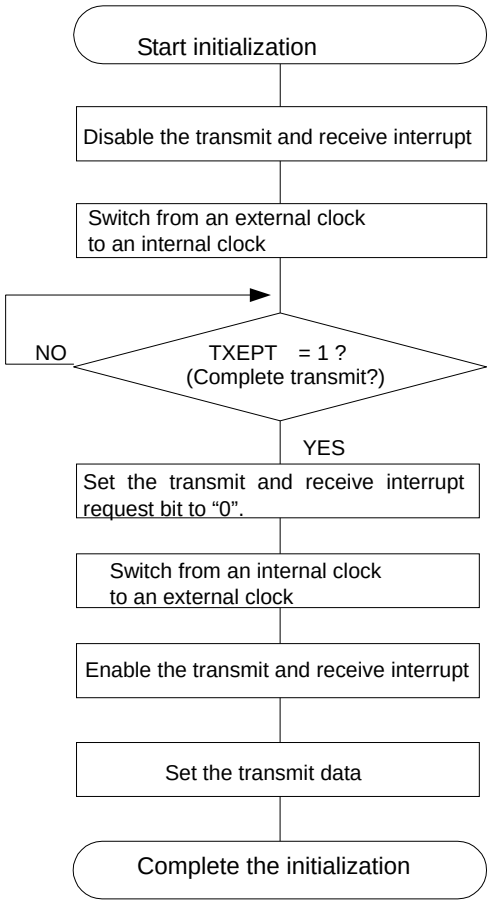
(30) G1TB register



The write –action to the register starts the transmission.

3.2 Process of an initialization when an external clock stops during the communication

Data is remained in the transmit buffer when an external clock stops during the communication. Switch from an external clock to an internal clock to output all the data remained in the transmit data. (Initialization of the transmit buffer). The receive buffer does not have to be initialized because the data is overwritten on the next data.



3.3 Precaution on Interrupts

Set the register IIOiIR (i=0 to 11) to “00_{16}” (Initialization) during the intelligent I/O interrupt routine. If you skip this procedure, the IR bit in the IIOiIC register is not set to “1” when the intelligent I/O generates the interrupt request, resulting in no interrupt being invoked.

4. The example of a reference program

The following will show the example of a reference program to use intelligent I/O external clock for a clock synchronous serial communication. Some changes and arrangements of the program will be necessary according to each user's application.

```
/*****************************************************************/
/*          File Name: rej05b0262_src.c                          */
/*          Ver    : 1.00                                        */
/*          FUNCTION:Clock synchronous serial                    */
/*          communication by using intelligent I/O group external clock      */
/*****************************************************************/
/*****************************/
/*    include fil              */
/*****************************/
#include <stdio.h>
#include "sfr32c83.h"

/*****************************/
/*    Function Definition     */
/*****************************/
void iio_init(void);
void receive_int(void);
void trans_int(void);
#pragma INTERRUPT receive_int
#pragma INTERRUPT trans_int
/*****************************/
/*    Global Variable Definition        */
/*****************************/
static int rec_buff;

/*****************************/
/*    main Function          */
/*****************************/
void main(void){
    _asm(" fclr   i");          /*  Disable the interrupt   */

    /*   main clock set     */
    prc0 = 1;                   /*   protect off   */
    mcd = 0x12;                 /*   main clock : no division   */
    prc0 = 0;                   /*   protect on   */

   /*   port set   */
    ips = 0x00;                 /*   Set P75 as ISRxD1   */
    psc = 0x08;
    psl1 = 0x00;
    ps1 = 0x08;

     iio_init();                /*   IIO synchronous communication initial set */


g1tb = 0xD5;                    /*   Write the transmit the data   */


    pd2 = 0xff;
```

```
    pd4 = 0xff;
    pd5 = 0xff;
    while(1){
        /* external clock stop? */
        if( 0/* Check external clock stop */ ){
            iio_init();             /*  IIO synchronous communication re-set  */
            g1tb = 0x8a;            /*  Set the receive data  */
        }
    }
}

/*  iio communication function initialize  */
void iio_init(void){
    short dummy;
    g1cr = 0x00;                /*  Disable the transmit and receive operation  */
    asm(" fclr  i ");           /*  Disable the interrupt request  */
    /*  base clock initial set  */
    g2bcr0 = 0x7f;              /*  Supply a clock for BTSR register */
    btsr = 0x00;                /*  Base timer reset  */
    g2bcr0 = 0x00;              /*  Stop group 2 clock  */

    /*  iio group1 initial set  */
    g1bcr0 = 0x7f;              /*  b0,b1: count source f1
                                    b2 to b6: division rate of count source: no division*/
    g1bcr1 = 0x02;
    g1pocr0 = 0x07;             /*  ISTxD1 select  */
    g1pocr3 = 0x02;
    g1po0 = 0x01;
    g1po3 = 0x00;

    g1fs = 0x00;                /*  ch0,ch3  Select a waveform generation function  */
    g1fe = 0x09;                /*  ch0,ch3  Enable the operation  */


    g1bcr1 = 0x12;              /*  Start the base timer  */

     g1mr = 0x81;               /* Internal clock  */
     g1cr = 0x10;               /*  Enable the transmit  */

    /* wait */
     while(txept_g1cr == 0)p1_5 = to p1_5; /* Output all the date remained in the transmit buffer by using the
                                              internal clock */
```

```
    dummy = g1rb;
    g1mr = 0x85;                    /*   clock synchronous serial, external clock, LSB first   */
    g1erc = 0x20;

    /*   iio group0 interrupt initial set   */
    iio2ie = 0x01;                  /*   Use the request use for interrupt     */
    iio3ie = 0x01;
    iio2ir = 0x00;
    iio3ir = 0x00;
    iio2ie = 0x21;                  /*   gr1 Enable the receive interrupt   */
    iio3ie = 0x21;                  /*   gr1 Enable the transmit interrupt   */
    iio2ic = 0x03;                  /*   Select the interrupt priority level   */
    iio3ic = 0x03;                  /*   Select the interrupt priority level   */

    /* interrupt enable     */
    _asm("fset      i");

    /*   sio initial setting   */
    g1cr = 0x30;                    /*   Enable the transmit and receive operation   */

}

/*   iio ch0 interrupt     */
void receive_int(void){
        iio2ir = 0x00;              /*   Clear the interrupt request   */
        rec_buff = g1rb;            /*   Read the received data   */
        g1tb = 0x55;            /*   Write the transmit data   */
}

void trans_int(void){
        iio3ir = 0x00;              /*   Clear the interrupt request   */
}


/*------------------------------ end program */
```

5. Reference

HADWARE MANUAL

Refer to the M32C/83 group HARDWARE MANUAL.

6. Web-site and contact for support

Renesas Web-site

http://www.renesas.com

Contact for Renesas technical support

Mail to : support_apl@renesas.com

REVISION HISTORY

Rev.	Issue date	Revised	
		Page	Point
1.00	Jan.30, 2004	-	First edition issued
1.01	Sep.16,2004	5	Inverted waveform output mode → phase-delayed waveform mode

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