

**Introduction**

There are many benefits [1] which result from the use of feedback in electronic circuits, but the drawbacks are the increased complexity of the calculations and the opportunity for the resulting circuit to ring or oscillate. This paper employs graphical techniques to simplify stability calculations, thus enabling the designer to achieve a stable, well behaved circuit which meets all reasonable performance criteria. Now the designer can obtain the advantages of feedback without worrying about ringing or oscillation.

**Development of the General Feedback Equation**

Referring to the block diagram shown in Figure 1, Equation 1, Equation 2 and Equation 3 can be written by inspection if it is assumed that there are no loading concerns between the blocks. The no loading assumption is implicit in all block diagram calculations, and this requires that the output impedance of a block be much lower than the input impedance of the block it is driving. This is usually true by one or two orders of magnitude. Algebraic manipulation of Equation 1, Equation 2 and Equation 3 yield Equation 4 and Equation 5 which are the defining equations for a feedback system.

$$V_O = EA \tag{EQ. 1}$$

$$E = V_I - \beta V_O \tag{EQ. 2}$$

$$E = V_O/A \tag{EQ. 3}$$

$$V_O/V_I = A/(1 + A\beta) \tag{EQ. 4}$$

$$E/V_I = 1/(1 + A\beta) \tag{EQ. 5}$$

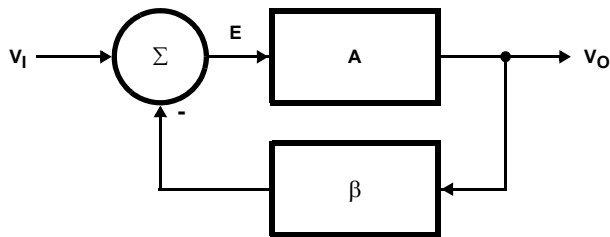


FIGURE 1. FEEDBACK SYSTEM BLOCK DIAGRAM

The parameter A, which usually includes the amplifier and thus contains active elements, is called the direct gain in this analysis. The parameter β, which normally contains only passive components, is called the feedback factor. Notice that in Equation 4 as the value of A approaches infinity, the quantity Aβ, which is called the loop gain, becomes much larger than one; thus, Equation 4 can be approximated by Equation 6. V<sub>O</sub>/V<sub>I</sub> is called the closed loop gain, and since the direct gain, or the amplifier response, is not included, the equation for the closed loop gain it is independent of amplifier parameter changes. This is the major benefit of feedback circuits.

$$V_O/V_I = 1/\beta \text{ for } A\beta \gg 1 \tag{EQ. 6}$$

Equation 4 is adequate to describe the stability of any feedback circuit because all feedback circuits can be reduced to the this form through block diagram reduction techniques [2]. The stability of the feedback circuit is determined by setting the denominator of Equation 4 equal to zero.

$$1 + A\beta = 0 \tag{EQ. 7}$$

$$A\beta = -1 = |1| \angle -180 \tag{EQ. 8}$$

Referring to Equation 4 and Equation 8, it is observed that if the magnitude of the loop gain, Aβ, can achieve one while the phase equals -180 degrees, the closed loop gain becomes infinity because of division by zero. Since this state is unstable, the circuit will oscillate, and it will oscillate at the frequency where the phase shift equals to -180 degrees. If the loop gain at the frequency of oscillation is slightly greater than one it will be reduced to one by the reduction in gain suffered by the active elements as they approach the limits of saturation, but if the value of Aβ is much greater than one, gross nonlinearities can occur and the circuit may then cycle between saturation limits. Preventing instability is the essence of feedback circuit design, thus this topic will be touched lightly here and covered in detail later. A good starting point for discussing stability is finding an easy method to calculate it. Figure 2 shows that the loop gain, Aβ, can be calculated from a block diagram by opening current inputs, shorting voltage inputs, breaking the loop and calculating the response to a test input signal.

$$V_{TO}/V_{TI} = A\beta \tag{EQ. 9}$$

The block diagram techniques can be applied to op amps thus reducing the stability analysis to a simple task. The schematic for a non-inverting amplifier is shown in Figure 3, and the block diagram equivalent is shown in Figure 4. Equation 10 and Equation 11 are combined to yield Equation 12 which describes the block diagram shown in Figure 4A, while block diagram transformations [3] are employed to get to Figure 4B.

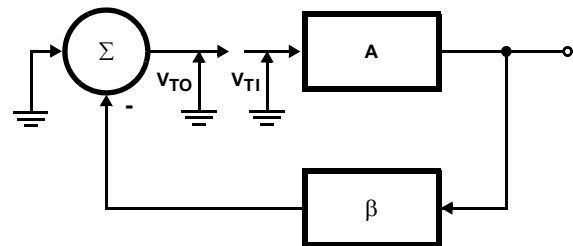


FIGURE 2. BLOCK DIAGRAM FOR COMPUTING THE LOOP GAIN

$$V_O = a(V_I - V_B) \tag{EQ. 10}$$

$$V_B = V_O Z_1 / (Z_1 + Z_2), I_B = 0 \tag{EQ. 11}$$

$$V_O = aV_I - aZ_1 V_O / (Z_1 + Z_2) \tag{EQ. 12}$$

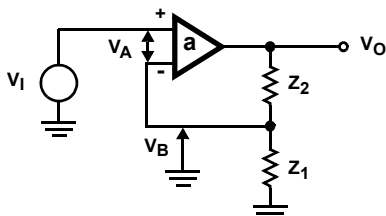


FIGURE 3. NON-INVERTING CIRCUIT

The block diagram shown in Figure 4A is written by inspection of Equation 12. The block diagram shown in Figure 4B is derived from Figure 4A by block diagram manipulations. Equation 13 is derived from Equation 12 by algebraic manipulation, or it can be written by inspection of Figure 4B because the system is shown in standard form.

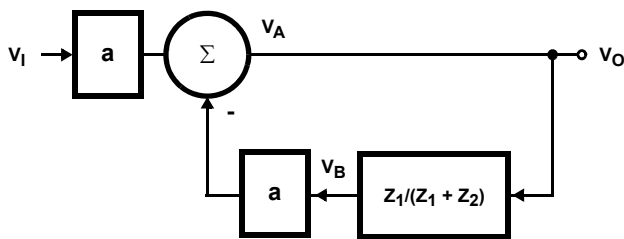


FIGURE 4A. BLOCK DIAGRAM AS WRITTEN FROM EQUATION 12

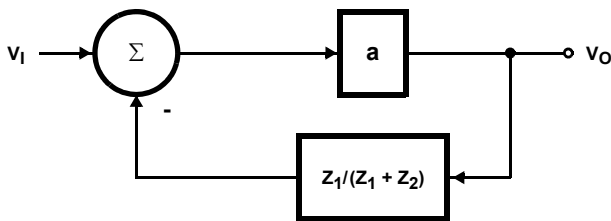


FIGURE 4B. AFTER BLOCK DIAGRAM MANIPULATION

FIGURE 4. BLOCK DIAGRAM OF THE NON-INVERTING OP AMP AS SHOWN IN EQUATION 12

$$V_O/V_I = a/(1 + aZ_1 / (Z_1 + Z_2)) \quad (\text{EQ. 13})$$

The loop gain,  $A\beta$ , is equal to  $aZ_1/(Z_1+Z_2)$ , the closed loop gain,  $1/\beta$ , is equal to  $(Z_1+Z_2)/Z_1$ , and the direct gain,  $A$ , is equal to the op amp gain,  $a$ . The loop gain can be determined from Figure 4B by inspection, or if the system block is not available the loop gain can be obtained directly from the amplifier schematic as shown in Figure 5. First set voltage sources to zero by grounding them, then open current sources, break the feedback loop at any convenient place and then calculate the loop gain. Remember, the output impedance of the op amp must be much lower than the feedback impedance so that block diagram techniques can be used. The test input is  $V_{T1}$ , and it is amplified by the op amp gain,  $a$ . The op amp output,  $aV_{T1}$  is divided by  $\beta$  before it is fed back as  $V_{T0}$ .

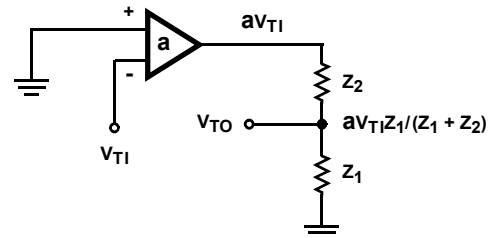


FIGURE 5. NON-INVERTING OP AMP WITH INPUT GROUNDED AND FEEDBACK LOOP BROKEN

$$\frac{V_{T0}}{V_{T1}} = \frac{aZ_1}{Z_1 + Z_2} = A\beta \quad (\text{EQ. 14})$$

Referring to the inverting op amp configuration shown in Figure 6, the analysis will be performed by working from the amplifier circuit to the block diagram. The closed loop gain equations are derived in references one and six as well as most electronic text books. The closed loop gain which is equal to  $1/\beta$  is known to be  $-Z_2/Z_1$ ; thus,  $\beta$  is calculated as  $Z_1/Z_2$  with the minus sign indicating a negative input. Referring to Figure 6, if  $V_I$  is set to zero and the loop is broken at the negative input to the op amp the circuit is identical to that shown in Figure 5.

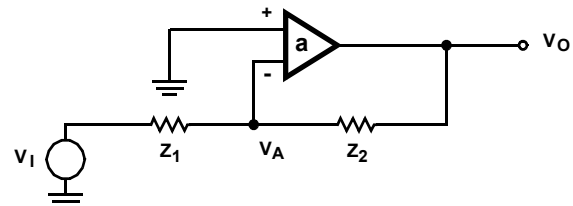


FIGURE 6. INVERTING OP AMP SCHEMATIC

An examination of Figure 5 and Figure 6 reveals that the loop gain,  $A\beta$ , is identical for both the inverting and non-inverting circuit configurations. The loop gain is the only parameter that determines stability, and it is not a function of the location of the inputs. Hence the loop gain for the inverting op amp is given to us by Equation 14. Now that  $A\beta$  and  $1/\beta$  are both known,  $A$  can be determined by multiplication to be  $aZ_2/(Z_1 + Z_2)$ . Since the direct gain and the loop gain are both known Figure 7 can be constructed from these quantities.

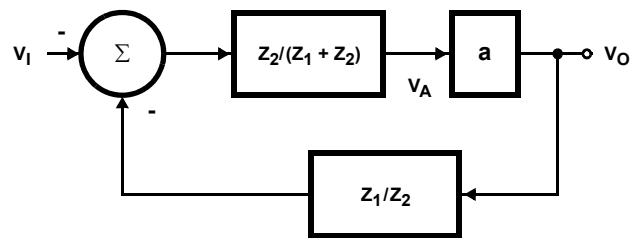


FIGURE 7. BLOCK DIAGRAM OF THE INVERTING OP AMP

Equation 15, which is the closed loop gain equation for an inverting op amp can be written directly from Figure 7. As  $(a)$  approaches infinity in Equation 15, the closed loop gain approaches  $-Z_2/Z_1$ .

(EQ. 15)

$$\frac{V_O}{V_I} = -\frac{\frac{aZ_2}{Z_1+Z_2}}{1+\frac{aZ_1}{Z_1+Z_2}}$$

The closed loop gain for the non-inverting circuit,  $V_O/V_I = (Z_1 + Z_2)/Z_1$ , is different from the closed loop gain for the inverting circuit,  $V_O/V_I = -Z_2/Z_1$ . It will always be the case that the loop gain, hence the stability, is independent of the location of the inputs, but the closed loop performance is highly dependent on the placement of the input. Many circuits take advantage of this phenomena to gain better performance as will be shown in the benefits section.

$$A_{NON-INV} = a; \text{ which is } \neq A_{INV} = aZ_2/(Z_1 + Z_2) \quad (\text{EQ. 16})$$

Comparing the block diagrams of the non-inverting and inverting circuits reveals that their direct gains are different, and this explains why there are some slight performance differences between the configurations. The non-inverting circuit with the higher direct gain has less closed loop error; at a closed loop gain of 2 for both circuits the non-inverting circuit has a 3.5dB more loop gain. The inverting circuit is more stable for the same magnitude of closed loop gain; i.e., for a closed loop gain of 2,  $A\beta_{INV} = 0.33a$  and  $A\beta_{NON-INV} = 0.5a$ . Normally these differences are minor, but they are pointed out because they may be taken advantage of or they can cause very subtle problems in unique situations.

There are many other op amp circuit configurations, but they will all reduce to these two basic forms; each of which is a variation of the basic feedback circuit shown in Figure 1. Letting  $Z_1$  and or  $Z_2$  equal various combinations of RLCs will give different closed loop performance, but the analysis techniques remain the same. More complicated circuit configurations can all be reduced to these simple circuits through block diagram reduction techniques and superposition.

**Benefits of Feedback**

The tolerances and drift coefficients of passive components are much less than those associated with active components. If the circuit transfer function can be made to be dependent only on the passive component parameters it will be a much more stable circuit; feedback accomplishes this through the direct gain as shown here. Differentiating the closed loop Equation 4, with respect to the direct gain yields Equations 17 and Equation 18 shown below. Notice that the percentage change in the closed loop gain is the percentage change in the direct gain divided by the loop gain. Thus for very high loop gains the initial accuracy and drift will be a function of the passive components rather than of the direct or amplifier gain. Although the feedback reduces the gain errors, other amplifier errors such as input voltage offset are not affected by the feedback because they occur as an input rather than within the feedback loop.

$$\frac{dV_O/V_I}{dA} = \frac{1}{(1+A\beta)^2} = \frac{1}{(1+A\beta)} \frac{V_O^3/V_I}{A} \quad (\text{EQ. 17})$$

(EQ. 18)

$$\frac{dV_O/V_I}{V_O/V_I} = \frac{dA}{A} \frac{1}{(1+A\beta)}$$

All amplifiers have noise and distortion characteristics associated with them, and low noise or low distortion amplifiers command a premium price. Very often feedback can be used at no cost increase to reduce the effects of distortion and noise. Both closed loop and open loop systems are shown in Figure 8 and Figure 9; notice that both systems have the same number of components except for the passive feedback elements.

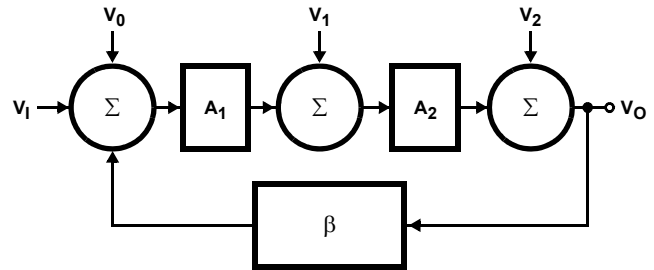


FIGURE 8. CLOSED LOOP SYSTEM

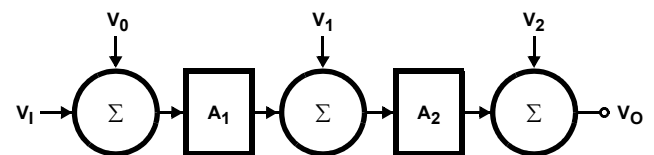


FIGURE 9. OPEN LOOP SYSTEM

Equation 19 and Equation 20 are derived from the closed loop and open loop systems shown in Figure 8 and Figure 9. If Equation 19 is rewritten as shown in Equation 21 it is obvious that Equation 22 results when the quantity  $A_1A_2$  approaches infinity as it will in an ideal system.

$$V_O = \frac{A_1A_2(V_1+V_0)}{1+A_1A_2\beta} + \frac{A_2V_1}{1+A_1A_2\beta} + \frac{V_2}{1+A_1A_2\beta} \quad (\text{EQ. 19})$$

$$V_O = A_1A_2(V_1+V_0) + A_2V_1 + V_2 \quad (\text{EQ. 20})$$

$$V_O = \frac{V_1+V_0}{1/(A_1A_2)+\beta} + \frac{V_1/A_1}{1/(A_1A_2)+\beta} + \frac{V_2/A_1A_2}{1/(A_1A_2)+\beta} \quad (\text{EQ. 21})$$

$$V_O = \frac{V_1+V_0}{\beta} + \frac{V_1/A_1}{\beta} \text{ For } A_1A_2 \text{ approaching infinity} \quad (\text{EQ. 22})$$

Now let  $V_0$  and  $V_1$  represent the amplifier's internal noise referred to the input, and let  $V_2$  represent the noise from the any other system components. Notice from Equation 22 that in the closed loop system  $V_2$  has disappeared,  $V_1$  is decreased proportional to the gain  $A_1$  and that the input noise has only been multiplied by the closed loop gain,  $1/\beta$ . Conversely, Equation 20 indicates that in the open loop system the input noise has been multiplied by  $A_1A_2$  (which would be equivalent to the closed loop gain), that  $V_1$  is multiplied by  $A_2$  and that  $V_2$  is present. The feedback in the closed loop system has dramatically reduced the noise from the sources which follow the amplifier  $A_1$  so this can become a big design advantage. In the closed loop system the amplifier  $A_1$  should be selected for its

excellent noise performance, but the amplifier  $A_2$  can be selected based on some other criteria such as cost. This option is not available in the open loop system.

Very often when driving low impedances like speakers, the output amplifiers are driven as close to the power supply rails as possible to obtain the maximum dynamic range. One result of this practice is that some distortion of the signal occurs as active device parameters are driven so that they become non-linear. This and most other sources of distortion usually occur in the output stages of the amplifier. Because the distortion occurs at the output it can be represented by  $V_2$  in Equation 19, and this quantity goes to zero as the direct gain approaches infinity, so it is essentially eliminated by feedback. The connection from the speaker driver output to the preamplifier input in audio amplifiers is there to provide the feedback which reduces the amplifier's distortion when the amplifier is driven to its limits. Some amplifiers such as guitar amplifiers purposely introduce distortion into the sound, so open loop amplifiers are used in these cases, but closed loop amplifiers are usually employed in high fidelity applications.

If the noise source,  $V_1$ , is set to zero in Equation 22, then the amplifier input noise represented by  $V_0$  is multiplied by the closed loop gain  $1/\beta$ . There is a method to further reduce the effects of  $V_0$  by using frequency discrimination methods. If  $V_0$  is examined as a function of frequency, it will be noticed that the noise is made up of many different frequency components, see Figure 10.

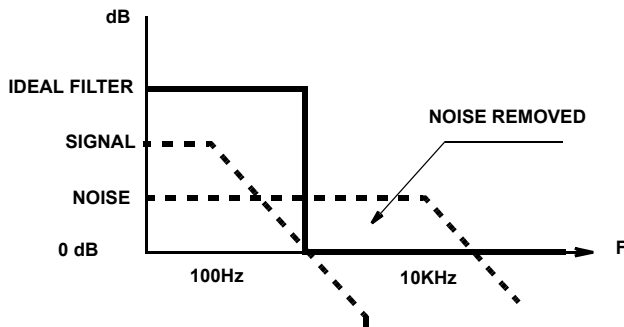


FIGURE 10. INSERTING AN IDEAL FILTER IN THE TRANSFER FUNCTION REDUCES NOISE

The signal of interest has a finite bandwidth, and if the noise bandwidth is larger than the signal bandwidth, the noise can be reduced by making the loop gain a function of frequency. Assuming that the noise bandwidth is 10KHz and that the signal bandwidth is 100Hz, the noise beyond 100Hz can be reduced to a minimum if  $1/\beta$  is reduced to zero beyond 100Hz. One method available to accomplish this bandwidth reduction is through the ideal filter inserted in the closed loop, as shown in Figure 10. This filter can be approximated with passive components.

The input and output impedance of the closed loop circuit can be controlled by the amount of feedback and by the circuit configuration [4]. Through the use of feedback it is possible for the same amplifier IC to appear to have an output impedance approaching zero or approaching infinity, depending on the circuit configuration employed.

Another interesting aspect of feedback systems is that if a function is put in the feedback loop, in a manner similar to the feedback factor,  $\beta$ , the inverse function will appear at the output.

**Graphical Representation of the Feedback Equation**

The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division; H. W. Bode [5] developed a technique called a Bode plot which simplifies the analysis through the use of graphical techniques. The Bode equations are log equations which take the form of  $20\text{LOG}(F(t)) = 20\text{LOG}(|F(t)|) + \text{phase angle}$ . Since these are log equations, the terms which were multiplied and divided can be now added and subtracted; thus, they can easily be solved graphically as will be shown. The transfer function for the integrator shown in Figure 11 is given in Equation 23.

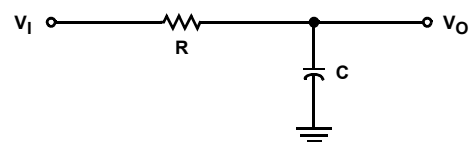


FIGURE 11. INTEGRATOR CIRCUIT

$$\frac{V_O}{V_I} = \frac{1}{(1+RCs)} \tag{EQ. 23}$$

Where  $s = j\omega$  and  $j = \sqrt{-1}$

The magnitude of the transfer function is given by the equation  $|V_O/V_I| = 1/\sqrt{(1+(RC\omega)^2)}$ . The approximate magnitude or  $|V_O/V_I| = 1$  when  $\omega = 0.1/RC$ ,  $|V_O/V_I| = 0.707$  when  $\omega = 1/RC$  and  $|V_O/V_I| = 0.1$  when  $\omega = 10/RC$ . These values are plotted in Figure 12 using straight line approximations.

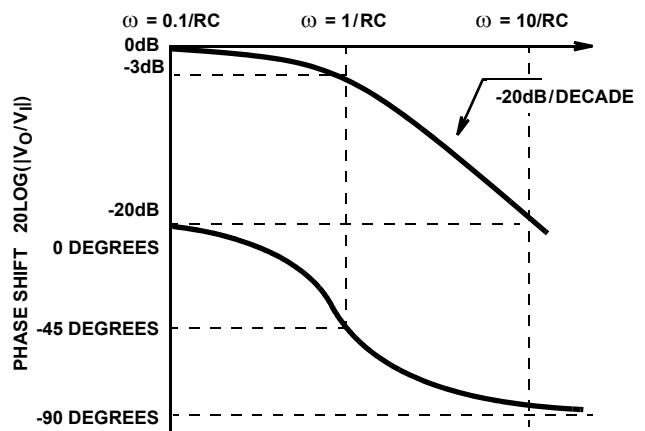


FIGURE 12. BODE PLOT OF INTEGRATING CIRCUIT TRANSFER FUNCTION

The downward slope of the amplitude curve in Figure 12 is -

20dB/decade, and the point at which the slope changes, at  $\omega = 1/RC$ , is termed the breakpoint. Reading the curve, it can be seen that gain initially is one, 0dB, at very low frequencies, falling off to 0.707, -3dB, at the break frequency and decreases at a rate of -20dB/decade for higher frequencies. The phase shift for the integrator is given in Equation 24 and plotted in Figure 12. Notice that the phase shift is -45 degrees at the breakpoint where  $\omega = 1/RC$ .

$$\phi = -\tan^{-1}(1/\omega RC) \quad (\text{EQ. 24})$$

When the breakpoint occurs in the denominator, its slope is negative and is called a pole. Conversely, when the breakpoint occurs in the numerator, its slope is positive and it is called a zero.

The band reject circuit shown in Figure 13 has two poles, two zeros and a DC gain. Each pole and zero is plotted separately in Figure 14. The DC gain component is plotted as a straight line at -6dB because it is frequency independent. The two zeros in the numerator both occur at  $\omega = 1/RC$ ; thus they are plotted on top of each other, and this results in a positive sloped line rising at 40dB/decade. The two poles in the denominator occur at  $\omega = 0.44/RC$  and  $\omega = 4.56/RC$ , and they are each plotted with a negative slope of -20dB/decade.

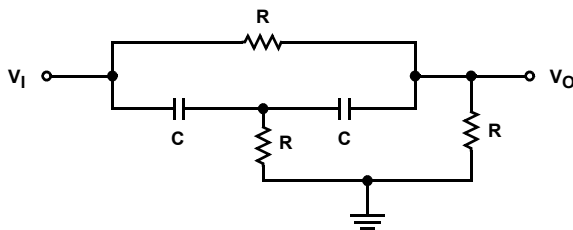


FIGURE 13. BAND REJECT FILTER CIRCUIT

$$\frac{V_O}{V_I} = \frac{(1 + RCs)(1 + RCs)}{2(1 + RCs/0.44)(1 + RCs/4.56)} \quad (\text{EQ. 25})$$

Where  $s = j\omega$ .

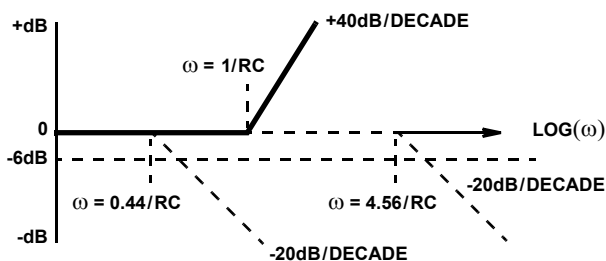


FIGURE 14. BODE PLOT OF THE INDIVIDUAL COMPONENTS OF THE BAND REJECT FILTER

Each of the separate Bode plots shown in Figure 14 are combined into one composite plot in Figure 15. The phase plots are treated much like the amplitude plots because the separate phase responses from the poles and zeros can be combined into one plot such as is shown in Figure 15. Now the complete amplitude or phase response of the circuit can be observed by looking at Figure 15. Although the phase shift at a pole is -45 degrees, the plot indicates -5 degrees at  $\omega = 0.44/RC$  because the double zero located at  $\omega = 1/RC$  has already accumulated

significant positive phase shift at the pole frequency. The non-linearity of the phase plot, a result of the tangent function, makes it hard to approximate accurately when several poles and zeros congregate in the same vicinity.

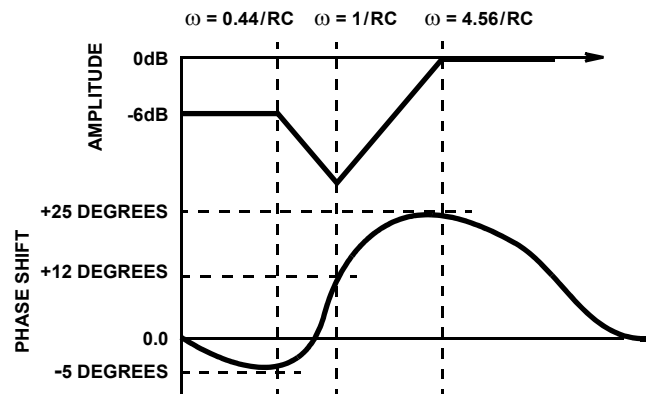


FIGURE 15. COMPOSITE BODE PLOT FOR THE BAND REJECT FILTER

Spacing the poles and zeros by a decade enables an accurate phase plot using approximate methods, but the circuit performance criteria usually will not allow this luxury. The amplitude plot also becomes smeared by the close proximity of the poles and zeros, but the exact values are not usually plotted because the approximate values usually suffice for analysis [6]. The demand for the phase accuracy stems from the oscillation or stability criteria which is dependent on phase.

Applying logarithms to the system equations will enable a quick and rather complete analysis. Equation 4 is repeated in Equation 26 in log form; i.e., both sides of the equation have been operated on by the function  $20\text{LOG}_{10}(F(t))$ .

$$20\text{LOG}(V_O/V_I) = 20\text{LOG}(A) - 20\text{LOG}(1 + A\beta) \quad (\text{EQ. 26})$$

As would be expected from the preceding analysis, the shape of the plot will be determined by the breakpoints, if any, contained in A or  $\beta$ . The magnitude portion of the closed loop system equation is plotted in Figure 16 for the case where A and  $\beta$  are not a function of frequency. Notice that both plots are flat lines, and there is no phase plot. Obviously this case is trivial and of no interest to the circuit designer because it does not represent the real world since the gain of all amplifiers is a function of frequency [7].

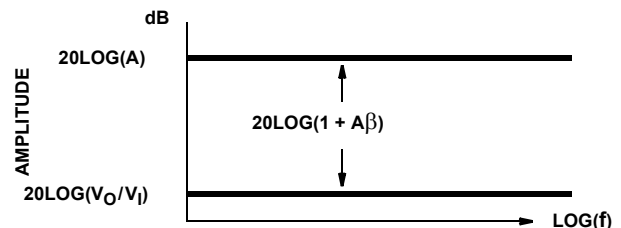


FIGURE 16. PLOT OF EQUATION 4 WHEN A AND  $\beta$  ARE NOT FREQUENCY DEPENDENT

Most high gain amplifiers such as operational amplifiers have multiple poles, two per transistor, with the amplifier having as many as 20 transistors leading to a potential of 40 or more poles. Normally only a few poles are important because the other poles occur at very high frequencies where the gain is less than one so that they

can not cause oscillation. In many amplifiers the manufacturer compensates the amplifier with a single pole usually called a dominant pole ( $f_{AMP}$ ), and the amplifier's performance can be approximated by the transfer function  $A = a/(1 + j(f/f_{AMP}))$ . Equation 4 is plotted in Figure 17 with the assumption that A is frequency dependent and  $\beta$  is resistive or frequency independent.

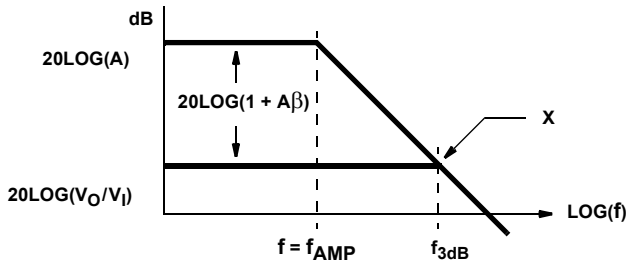


FIGURE 17. PLOT OF EQUATION 4 WHEN  $A = a/(1 + j(f/f_{AMP}))$  AND  $\beta$  IS FREQUENCY INDEPENDENT

The closed loop gain graphical approximation is constant until its projection intersects the amplifier gain at point X. The actual closed loop gain starts rolling off prior to point X, and it is down -3dB at point X. If  $20\text{LOG}(V_O/V_I) - 20\text{LOG}(A) = -3\text{dB}$  then  $-20\text{LOG}(1 + A\beta) = -3\text{dB}$ , and if the magnitude of  $(1 + A\beta)^2 = 1.414$  resulting in  $A\beta = 1$ . In other words,  $A = 1/\beta$  at the intersection of the two curves. There is a method [8] of relating the phase shift, and thus the stability, to the slope of the curves at the intersect point, but this method will not be covered here in favor of the Bode  $A\beta$  method.

The dominant pole causes the open loop gain to have a breakpoint at the frequency  $f_{AMP}$ . The internally compensated op amp acts like a dominant pole characteristic so its AC parameters can be determined by referring to the "Open-Loop Frequency Response" curve contained in the data sheet. Although the curve is called "Open-Loop Frequency Response", it really is the direct gain (A). Notice that the CA158 op amp as shown in the Intersil Corporation catalog [9] has a breakpoint which occurs at  $f_{AMP} = 5\text{Hz.}$ , and the DC gain is 110dB. If the transfer function shown in Figure 17 was for the CA158 then the direct gain would be  $A = a/(1 + j(f/f_{AMP}))$ , or  $A = 316,227/(1 + j(f/5))$ . Consider for a moment the difficulty and hence the probable error associated with measuring the DC gain and the break point. A popular method of measuring the op amp gain and phase is to configure the op amp in the inverting mode and then measure the error voltage; i.e., the voltage from the inverting input to ground. Then Equation 3,  $E = V_O/A$ , is employed to calculate the op amp gain from the measured error. Assume that the op amp is configured in a gain of -100; then the direct gain is  $A = 100/101$  times the op amp gain so a small offset must be accounted for because the measurement is not a direct measurement in the inverting circuit configuration. If the output voltage,  $V_O$ , is kept small to guarantee small signal accuracy, say one volt, then for the CA158,  $V_{ERROR} = 1/316,217 = 3.16\mu\text{V}$ . Measuring this small voltage especially considering that noise may be present is a formidable task so designers must assume that there may be a considerable tolerance associated with these measurements. The numbers given in this paper are for explanation purposes; professional test engineers will often configure the op amp with a gain of  $A = -10,000$  and then be measuring errors in the nano-volt range. These measurements require considerable skill, and even then there may be

a 24dB difference between the minimum specification point and the typical value such as in the HA5177 data sheet.

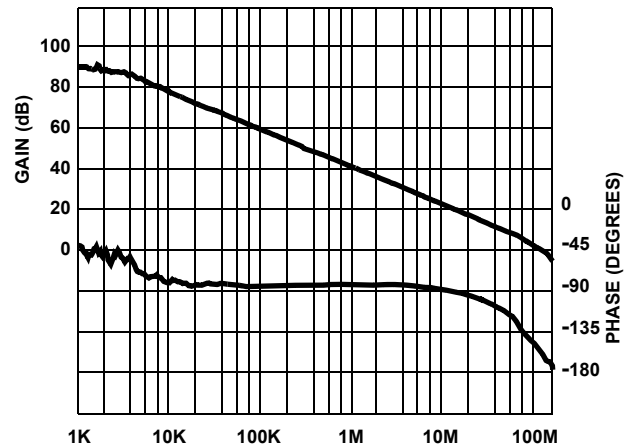


FIGURE 18. OPEN LOOP FREQUENCY RESPONSE OF THE HA2842C

Figure 18 is a plot of the gain phase relationship for a high frequency op amp, the HA2842C. The DC gain is 90dB, and since the phase shift reaches -45 degrees at 1200Hz the first pole must occur at approximately 1200Hz. This is a high frequency op amp so the internal compensation capacitor has been reduced significantly to increase the bandwidth available to the designer, and it is apparent that a second pole exists because the phase shift approaches -135 degrees at 70MHz. Looking closely at the point where the gain crosses the 0dB axis, and then following that constant frequency line, 120MHz, down to the phase curve indicates that the phase shift is about -165 degrees. This op amp is marginally stable, and the op amp is susceptible to stability problems unless external compensation techniques are employed. The HA2842C can be modeled with a DC gain of 31,623, the first break point at 1200Hz and the second breakpoint at 145MHz. The equation for the HA2842C is then  $A = 31,623/(1 + j(f/1200))(1 + j(f/145E6))$ .

#### Stability as Determined from Loop Plots

$$A\beta = -1 = |1| \angle -180 \quad (\text{EQ. 27})$$

Equation 8 has been repeated above as Equation 27. If the magnitude of the gain is greater than one in Equation 27, the equation will be satisfied because the non-linear effects of the active devices as they enter saturation will reduce the gain to one. This is demonstrated in oscillator design where the designer must design for a worse case gain of at least one, so the circuit will oscillate under all conditions, and the nominal gain usually is much greater than one. The oscillator designers are caught in a trap, for if they design for a worse case low gain greater than one, then the worse case high gain will be much greater than one. In the low gain case, the circuit barely oscillates, but the sinewave is very pure. In the high gain case, the circuit always oscillates, but there is significant distortion in the sinewave. Just as the oscillator designer must make compromises for the sake of instability, so, the analog designer make compromises for the sake of stability. In the case of amplifier design, the phase shift must never become -180 degrees, at a gain greater than one, or oscillation will occur. The compromise

occurs when the amplifier designer trades off gain and/or bandwidth for positive phase shift because the methods which produce a safe phase shift tend to reduce gain or bandwidth, as will be shown later. In many cases oscillation is not the limiting factor because as the phase shift gets much greater than -135 degrees, the amplifier output will have increasing overshoot and ringing. Plotting the loop gain gives great insight into both the stability and closed loop performance; stability will be discussed in this section and closed loop performance predictions from open loop plots will be discussed in the next section.

$$A\beta = \frac{K}{(1 + R_1 C_1 s)(1 + R_2 C_2 s)} \quad (\text{EQ. 28})$$

where K = DC gain.

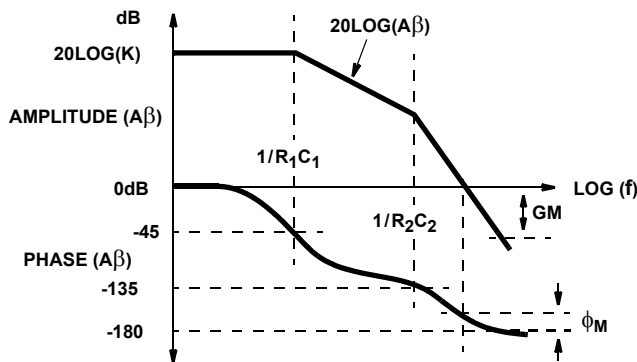


FIGURE 19. LOOP PHASE AND GAIN PLOT OF EQUATION 27

Figure 19 is used to help define the industry standard terms, phase margin,  $\phi_M$ , and gain margin, GM. Phase margin is a measure of relative stability, and it is defined as the amount of phase shift between the point where the loop gain equals 0dB and -180 degrees. Equation 29 defines the phase margin mathematically.

$$\phi_M = 180 - \text{tangent}^{-1}(A\beta) \quad (\text{EQ. 29})$$

Gain margin is defined as the gain at the point where the phase equals -180 degrees. Gain margin is always a negative (dB), or less than one, in a stable system, and it does not contain much information about stability or closed loop performance. The phase margin shown in Figure 19 is approximately 16 degrees; attempting to measure the phase margin in Figure 19 points out how important it is to plot phase margin accurately. This circuit will be stable since the phase margin is positive; the phase shift cannot ever reach the -180 degrees required for oscillation if the circuit is to remain stable. Because the phase margin is very small, the overshoot will be very large, and the output will exhibit a damped oscillation commonly known as ringing. If the gain, K, were increased in the loop transfer function until it crossed the 0dB axis at -180 degrees phase shift, then the circuit would oscillate; thus, there is a definite limit on the loop gain. The loop transfer function, shown as Figure 19, is repeated in Figure 20 with the gain increased by a factor of C. Notice that indeed the -180 degree phase crossover point occurs prior to the 0dB crossover point, so the phase margin is negative and the circuit will oscillate. Conversely, the transfer function shown in Figure 20 does not even have enough gain at the -180 degree point to ensure oscillation under production tolerances, so the circuit is good for nothing in its present condition.

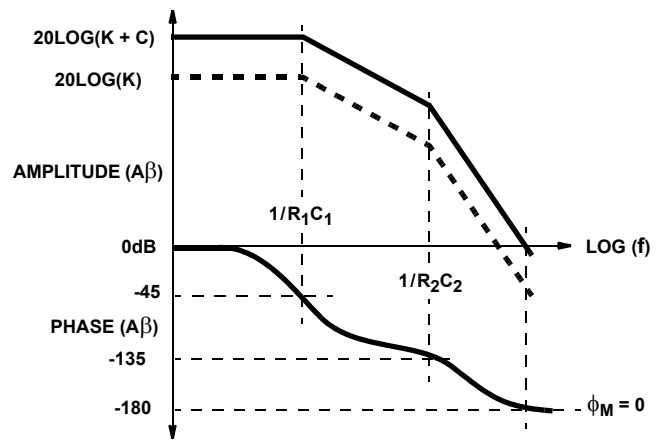


FIGURE 20. LOOP PHASE AND GAIN PLOT OF EQUATION 27 WITH ADDED GAIN C

Extremely high gain systems have very low errors, but they are limited in the bandwidth they can obtain without oscillating, so designers resort to other techniques such as non-linear transfer functions. An example of a high gain, accurate system which employs non-linear techniques to achieve stability, is a gyro stabilization platform which would go into a limit cycle if the gain was not reduced upon start-up.

If the second breakpoint,  $1/R_2 C_2$ , were moved closer to the first breakpoint, then the circuit would accumulate phase shift from the breakpoint earlier and it may become unstable. Figure 19 is repeated as Figure 21, where the second breakpoint has been moved closer to the first breakpoint. Notice that the -45 degree phase point is not affected, the -135 degree phase point has moved in towards the -45 degree phase point, and that the -180 degree phase point occurs prior to the 0dB crossover point. Generally, moving the two poles closer together can cause instability.

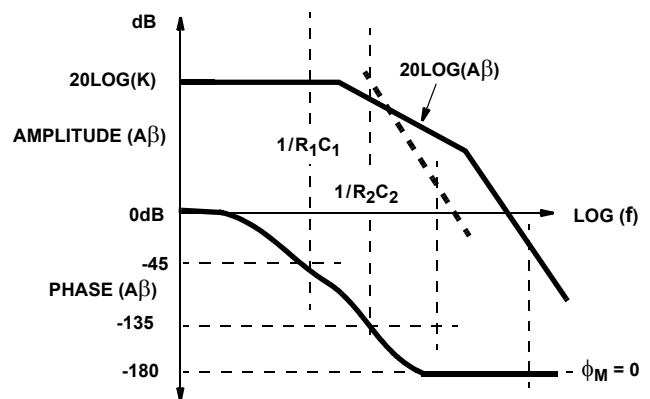


FIGURE 21. LOOP PHASE AND GAIN PLOT OF EQUATION 27 WITH  $1/R_2 C_2$  CLOSER TO  $1/R_1 C_1$

The single pole system cannot accumulate more than -90 degrees of phase shift so it cannot become unstable; thus single pole systems will not be discussed here. This does not mean that an internally compensated op amp, which acts like a dominant pole, cannot become unstable because all op amps have more than one pole. The proof of this is the data sheet, consider the HA2500 [10] which is internally compensated for unity gain, where the Open Loop Frequency and Phase Response curve

shows phase shifts beyond -90 degrees. Lots of good data can be gathered from these curves; i.e., the phase margin for the HA2500 is approximately 30 degrees so there will be some overshoot, and there is a second pole at about 3MHz. There is no such thing as an unconditionally stable op amp unless it lies on the table with power disconnected, because all op amps are multiple pole devices especially when stray capacitances are considered. This conclusion may lead someone to wonder where to draw the line when doing an analysis, and most engineers draw the line at two poles because the mathematics are easy to handle. If required, they obtain a solution for larger systems through the use of superposition, but usually the poles are separated far enough for some of them to be ignored or the circuit is modified to achieve the separation. The next section will delve into the second order stability analysis more deeply. Poles and zeros always occur in pairs, although sometimes either the pole or zero may be at the origin or infinity, thus they will not always appear in the transfer function. Whenever a pole is referred to, its corresponding zero is also considered.

**Predicting Stability and Performance from Closed Loop Plots**

The closed loop AC performance of a feedback circuit is dependent on the order of the denominator equation which is often considered equivalent to the number of poles contained in the circuit. If the circuit has no poles then its AC performance does not vary with frequency. If the circuit has one pole then the closed loop AC performance is rather easy to describe; the gain on a Bode plot will be 20LOG(K) and the amplitude response will start falling off at the breakpoint with a -20dB/decade slope. If the circuit has two or more poles the closed loop AC response is much more complicated, the circuit can overshoot, then ring and finally oscillate. The second order circuit, which contains two poles, is so popular that it is described extensively in the literature [11], and it is the one that will be dwelled on here. Higher order circuits can usually be reduced to second order for closed loop performance analysis, so this analysis will be restricted to stability and closed loop performance for second order circuits. Equation 7 is written here as Equation 30 with a second order loop transfer function substituted for Aβ. Equation 31 is obtained from Equation 30 through algebraic manipulation.

$$1 + A\beta(s) = 1 + \frac{K}{(1 + s\tau_1)(1 + s\tau_2)} = 0 \tag{EQ. 30}$$

where  $\tau = RC$

$$s^2 + \frac{\tau_1 + \tau_2}{\tau_1\tau_2}s + \frac{1+K}{\tau_1\tau_2} = 0 \tag{EQ. 31}$$

Equation 32 is the standard second order control equation, and it is compared to Equation 31 to obtain Equation 33 and Equation 34 which define the damping ratio,  $\zeta$ , and undamped natural frequency,  $\omega_N$ .

$$s^2 + 2\zeta\omega_N s + \omega_N^2 = 0 \tag{EQ. 32}$$

$$\omega = 2\pi f$$

$$\omega_N^2 = \frac{1+K}{\tau_1\tau_2} \tag{EQ. 33}$$

$$2\zeta\omega_N = \frac{\tau_1 + \tau_2}{\tau_1\tau_2} \tag{EQ. 34}$$

The frequency where the magnitude of the loop transfer function, Aβ, is equal to one is defined as the crossover frequency,  $\omega_C$ ; this is expressed in Equation 35 with  $\omega_C$  substituted for  $\omega$ . Then Equation 35 is algebraically manipulated to obtain Equation 36 from which the phase functions shown in Equation 37 and Equation 38 are obtained.

$$\frac{K}{\sqrt{(1 + \omega_C^2 \tau_1^2)} \sqrt{(1 + \omega_C^2 \tau_2^2)}} = 1 \tag{EQ. 35}$$

$$\omega_C^4 + 2\zeta\omega_N^2\omega_C^2 - \omega_N^4 = 0 \tag{EQ. 36}$$

$$\phi_M = \text{TAN}^{-1} \left| \frac{\omega_C(\tau_1 + \tau_2)}{1 - \omega_C^2 \tau_1\tau_2} \right| \tag{EQ. 37}$$

$$\phi_M = \text{TAN}^{-1} |2\zeta\omega_N/\omega_C| \tag{EQ. 38}$$

Considering the transfer function shown in Figure 22, if the 0dB crossover frequency,  $\omega = \omega_C$ , occurs well after the break frequency,  $1/\tau_2$ , then Equation 39 can be simplified to Equation 40. Solving Equation 40 for  $\omega_C$  yields Equation 41.

$$20\text{LOG}(A\beta) = 20\text{LOG}(K) - 20\text{LOG}(1 + \omega^2\tau_1^2)^{1/2} - 20\text{LOG}(1 + \omega^2\tau_2^2)^{1/2} \tag{EQ. 39}$$

$$20\text{LOG}(A\beta) = 20\text{LOG}(K) - 20\text{LOG}(\omega\tau_1) - 20\text{LOG}(\omega\tau_2) \text{ for } \omega \gg 1/\tau_2 \tag{EQ. 40}$$

$$\omega_C = \sqrt{\frac{K}{\tau_1\tau_2}} \approx \omega_N \text{ for } \omega \gg 1/\tau_2 \tag{EQ. 41}$$

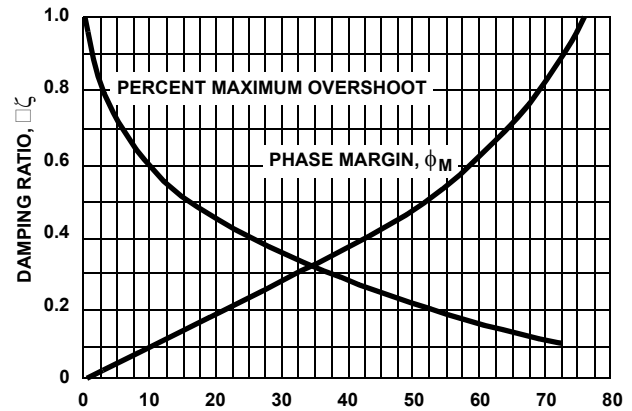


FIGURE 22. PHASE MARGIN AND PERCENT OVERSHOOT AS A FUNCTION OF DAMPING RATIO

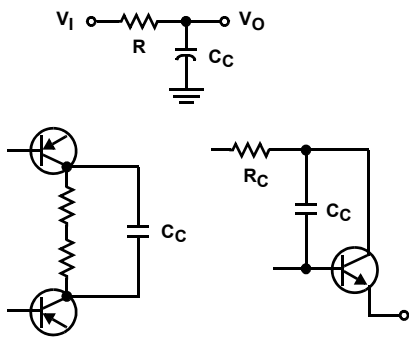
Figure 22 is a plot of Equation 38; now the phase margin is expressed in terms of known quantities so it can be calculated from a knowledge of the pole locations. The estimation procedure is to determine the pole locations from knowing the op amp pole locations and from the external circuitry. Once the pole locations and the gain are known or estimated the phase margin, damping ratio and cutoff frequency can be calculated. Then using Figure 22 yields the percent overshoot. The pole locations and gain can be varied to obtain different solutions to the problem. After all of this data is satisfactory, then the loop transfer function should be plotted to determine stability. While only the poles were used in the estimation procedure, both the poles and zeros must be used to plot the open transfer function. After several iterations a workable solution should pop out



if one exists. Remember that this procedure is an approximation, thus it must always be verified in the laboratory.

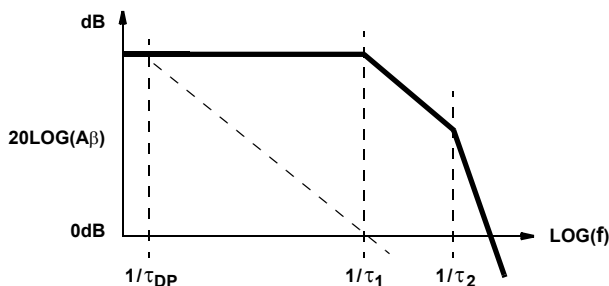
**Compensation Schemes**

All op amps are compensated; some are compensated with internal components thus saving the designer time and money. Many op amps are not compensated internally because leaving out the compensation gives the designer an extra degree of freedom, and these op amps must have some kind of external compensation or they will oscillate. The internally compensated op amps are usually compensated with a method called 'dominant pole' or 'lag' compensation several forms of which are shown in Figure 23.



**FIGURE 23. EXAMPLES OF DOMINANT POLE COMPENSATION**

Dominant pole compensation circuits tend to be associated with the op amp, and they usually are not part of the feedback circuit. The loop transfer function for an op amp is shown in Figure 24 in solid lines. There are two poles accumulating phase shift prior to the 0dB crossover point; thus this circuit may very well be unstable. The first pole,  $1/\tau_1$ , is the low frequency break point of the op amp, and the second pole,  $1/\tau_2$ , is the high frequency break point. Since these pole locations are inherent in the op amp design, the circuit designer must live with them, but the effects of these poles can be modified with external feedback components. Locating the dominant pole,  $1/\tau_{DP}$ , so that the 0dB crossover point coincides with the first op amp pole,  $\tau_1$ , yields a phase margin of 45 degrees. By locating the dominant pole zero crossing at  $1/\tau_1$  the circuit sacrifices significant bandwidth which can be regained by moving the pole further out. The exact pole placement will be a function of the circuit specifications such as the allowed overshoot or the bandwidth required.

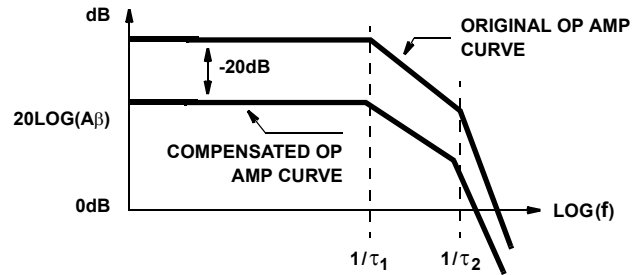


**FIGURE 24. DOMINANT POLE COMPENSATION PLOT**

Because of the loop gain loss and the bandwidth loss dominant

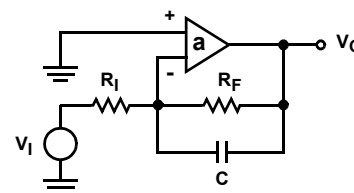
pole compensation is only used inside the op amp, when the closed loop bandwidth requirements are not great, or if noise reduction is desired. A simpler method of compensating the op amp is with gain compensation. Consider Equation 14 which is repeated here as Equation 42; this equation is for the loop gain and it is valid for both inverting and non-inverting op amps. If the closed loop inverting gain is increased to 9, then Equation 42 becomes  $A/10$  a decrease of 20dB in the DC intercept. Plotting these results in Figure 25 reveals that the circuit has become stable without much of a bandwidth reduction.

$$\frac{V_{\tau O}}{V_{\tau I}} = \frac{aZ_1}{Z_1 + Z_2} = A\beta \tag{EQ. 42}$$



**FIGURE 25. GAIN COMPENSATION**

The occasion always arises where the closed loop gain must be one or less, thereby precluding the use of gain compensation; thus the designer must resort to other techniques to achieve the circuit performance. An alternate method of compensation is called lead compensation, and it consists of putting a zero in the loop transfer function to cancel out one of the poles. The best place to locate the zero is on top of the second pole, since this cancels the negative phase shift caused by the second pole. The schematic of a circuit which employs lead compensation is shown in Figure 26, and Equation 43 is for the loop transfer function.



**FIGURE 26. LEAD COMPENSATION**

The zero in Equation 43 occurs before the pole, so it can be used to cancel out the pole at  $1/\tau_2$  by placing the zero on top of the pole. Now the 135 degree phase shift point has moved out to  $1/R_F || R_I C_S$  yielding better phase margin. There are always compromises to be made when designing a feedback circuit, and the one made here is to add external components. If the op amp has additional poles close to  $1/\tau_2$ , and many op amps do, then the pole placement is critical. Some op amps have so many poles in the area of  $1/\tau_2$  that this method of compensation cannot be used.

$$A\beta = \frac{aR_I (R_F C_S + 1)}{R_I + R_F (R_I || R_F C_S + 1)} \tag{EQ. 43}$$

Unless specified otherwise, the amplifier gain (a) will be

assumed to have the form  $a = K/(1 + \tau_1s)(1 + \tau_2s)$ .

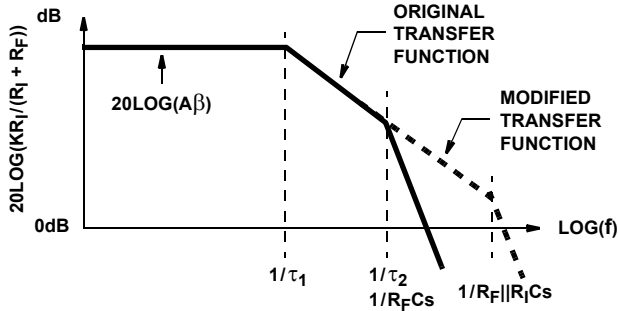


FIGURE 27. LEAD COMPENSATION PLOT

Sometimes a good look at the problem reveals a potential solution, so the case of stray input capacitance will be investigated. An inverting amplifier with a stray input capacitance,  $C_I$ , is shown in Figure 28. Looking at Equation 44 for the open loop transfer function, it is obvious that the stray capacitance adds a pole to the transfer function, and if the added pole is close to  $1/\tau_2$  the circuit will become unstable. The capacitor,  $C_F$  shown in dotted lines, is added to the circuit to yield the transfer function shown in Equation 45. Inspection of Equation 45 reveals that if  $R_I C_I = R_F C_F$ , then the poles and zeros in the transfer function will cancel each other, and the transfer function will appear to be independent of frequency. This type of compensation is named after the same idea used in the compensated attenuator, which is an old instrument design trick. Which just proves that little in circuit design is really new.

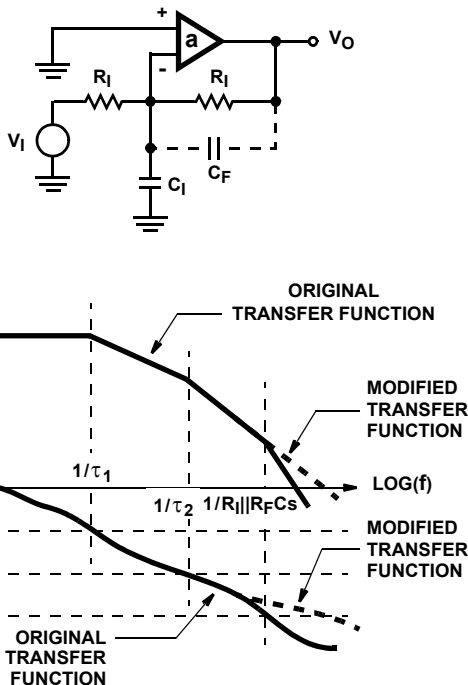


FIGURE 28. COMPENSATED ATTENUATOR CIRCUIT SCHEMATIC, GAIN PLOT AND PHASE PLOT

No  $C_F$ :

$$A\beta = \frac{aR_I}{R_I + R_F} \frac{1}{1 + R_I || R_F C_s} \quad (\text{EQ. 44})$$

$C_F$  in circuit:

$$A\beta = \frac{\frac{aR_I}{(R_I C_I s + 1)}}{\frac{R_I}{(R_I C_I s + 1)} + \frac{R_F}{(R_F C_F s + 1)}} \quad (\text{EQ. 45})$$

There are times when an extra degree of freedom is required and the lead-lag, sometimes called the feed-forward, form of compensation yields this freedom. This method of compensation puts a pole and a zero in the loop transfer function. If the pole and zero locations must be independent of each other, then separate compensation networks need to be used. An example of this would be to use a lag circuit similar to that shown in Figure 24, and a lead circuit similar to that shown in Figure 26. The lead and lag would then be independent in the example so they could be placed conveniently for compensation purposes. The circuit shown in Figure 29 has both a pole and a zero, but their placement is not independent.

$$A\beta = \frac{aR_I}{R_I + R_F} \frac{(RCs + 1)}{\frac{RR_I + R_F R + R_F R_I}{R_F + R_I} Cs + 1} \quad (\text{EQ. 46})$$

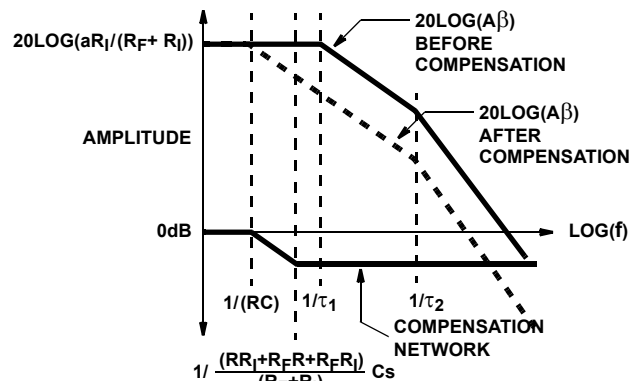
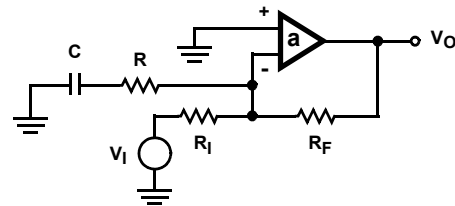


FIGURE 29. LEAD-LAG COMPENSATION SCHEMATIC AND  $A\beta$  AMPLITUDE PLOT

Referring to Figure 29, it can be seen that the lead-lag compensated circuit crosses 0dB at a lower frequency than the uncompensated circuit, thus the compensation has made the circuit more stable. Also, the transfer function of the compensation has been shown in Figure 29 for clarity. There is an additional advantage to lead-lag compensation in that it yields higher gain at high frequencies. The closed loop gain plots, Figure 30, show that the zero precedes the pole; the poles and zeros interchange when the plot changes from the loop gain to the closed loop gain. Also, the high frequency gain is emphasized with lead-lag compensation. The high frequency empha-

sis may be desirable when a high overall gain is needed, but some unwanted effects, such as DC offset, must be minimized. The lead-lag method of compensation usually requires the precise placement of the poles and zeros so a detailed and accurate [12] phase plot is generally constructed for this case.

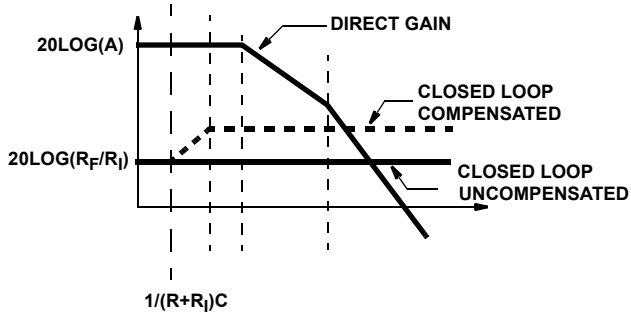


FIGURE 30. LEAD-LAG CLOSED LOOP GAIN PLOTS FOR COMPENSATED AND UNCOMPENSATED CIRCUITS

### Comparison of Compensation Results

Dominant pole compensation is the easiest method of compensation to implement within an IC, but it rolls off the closed loop gain so quickly that it is seldom used except in op amp design. The circuit resulting from dominant pole design is very well behaved because the phase margin is usually about 45 degrees, but the frequency response is very poor. If the transfer function for the HA2842C shown in Figure 18 is compensated by dominant pole compensation, the pole would be placed at 1200Hz; the loop gain when moving to a lower frequency would then rise at a rate of 20dB/decade until it hit the 90dB point at 0.06Hz. This is an effective bandwidth reduction of 4.5 decades, from 120MHz to 1200Hz, so this method is only used when no other type of compensation is available, noise reduction is more important than bandwidth or bandwidth is not important.

Gain compensation is always the preferred method of compensation if the resulting higher closed loop gain meets the performance criteria, but many times the design specifications call for a buffer or an inverter both with a gain of one, which precludes gain compensation. Gain compensation does not require any additional external components beyond the gain setting resistors, it preserves the op amp bandwidth and it is easy to implement. In a single pole system, increasing gain will reduce the bandwidth by the same factor.

Lead compensation offers an AC compensation which can function for any DC gain, and it has a much higher frequency response than dominant pole compensation. One deficiency with lead compensation is that the DC gain, the zero and the pole are all tied together tightly. For example if the HA2842C shown in Figure 18 is lead compensated for a closed loop gain of -1 then  $R_1 = R_F$ . This means that the pole and zero are only separated by an octave so the compensation must be done in an area of the loop gain plot which is very close to 0dB. Observing Figure 18, it can be seen that the best place that lead compensation can improve stability significantly is at the second pole where the phase equals -135 degrees phase shift and the frequency is 75MHz. Placing the zero at 75MHz yields a phase margin of about 60 degrees resulting a nice stable circuit with 10% overshoot per Figure 22. The closed loop response equation is  $V_1/V_F = R/R_1 1/(R_F C_s + 1)$ , and the closed loop gain is -1 until it reaches the frequency  $f = 1/2\pi R_F C$ , 150MHz, where it is down by -3dB. Lead compensation rolls off the closed loop frequency response dramatically.

The compensated attenuator approach works well for negating the effects of an input capacitance because both the open loop and closed loop transfer functions have a flat frequency response. Also, the compensation required is very small. When the output resistance of an op amp gets very high, the stray capacitance seen across the resistor acts like a lead circuit and rolls off the high frequency gain. Adding an input capacitor, the reverse of attenuator compensation, serves to restore the high frequency performance. Both digital-to-analog converters and optical receiving diodes have large associated capacitances, so when they are put into the input circuit of an op amp, often in an I-to-V converter configuration, the circuit oscillates. The compensated attenuator tames these circuits, but beware, the compensation must consider the worst case especially for current DACs which have a wide range of output capacitance.

The lead-lag compensation scheme is very similar to the lead compensation scheme but it has two advantages. First, setting the DC gain does not fix the pole zero separation, so for low gains the pole and zero could be separated by more than an octave. Second, a zero shows up in the closed loop transfer function where it increases the gain at high frequencies. The combination of these two advantages are great enough to outweigh the cost of the extra components added to the circuit.

The compensation techniques demonstrated here serve as a good foundation for feedback circuit design, but like all foundations it is meant to be built on [13]. There are other methods of treating compensation such as closed loop stability plots, Nichols charts, root locus plots and Nyquist analysis. Each technique offers some advantages and disadvantages; the Bode method simply is the author's personal choice so the other techniques deserve investigation.

## References

- [1] Areocentric, Sol, Feedback Amplifier Principles, Macmillan Publishing Company, 1986.
- [2] Del Toro, Vincent and Parker, Sydney, Principles of Control Systems Engineering, McGraw-Hill Book Company, 1960.
- [3] Del Toro, Vincent and Parker, Sydney, Principles of Control Systems Engineering, McGraw-Hill Book Company, 1960.
- [4] DiStefano, Joseph, Stubberud, Allen and Williams, Ivan, Theory and Problems of Feedback and Control Systems, Schaum's Outline Series, McGraw-Hill Book Company, 1967.
- [5] Bode H. W., Network Analysis and Feedback Amplifier Design, D. Van Nostrand, Inc., 1945.
- [6] D'Azzo, John and Houpis, Constantine, Feedback Control System Analysis and Synthesis, McGraw-Hill Book Company, 1966.
- [7] Frederiksen, Thomas, Intuitive Operational Amplifiers, McGraw-Hill Book Company, 1988.
- [8] Bower, J. L. and Schultheis, P. M., Introduction to the Design of Servomechanisms, Wiley, 1961.
- [9] Intersil Corporation, Linear and Telecom ICS for Analog Signal Processing Applications, 1993-94.
- [10] Same as above.
- [11] Del Toro, Vincent and Parker Sydney, Principles of Control Systems Engineering, McGraw-Hill Book Company, 1960.
- [12] Kuo, Benjamin, Automatic Control Systems, Prentice-Hall, Inc., 1975.
- [13] Bell, Ken, Conversations about feedback circuits while at Charles Stark Draper Labs, 1971.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.  
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.  
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics America Inc.**  
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852-2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338