

## Introduction

This application note provides guidance on the thermal considerations and preferred layout practices for using Zilker Labs' Digital-DC power management and conversion ICs. Intended applications for these parts are primarily synchronous buck embedded regulators powering high density logic devices in a multiple voltage, space-constrained environment.

### Overview

The Zilker Labs integrated power control and management products provide world-class power conversion with flexible power management functions to embedded regulator applications. The members of this product family contain a mixed-signal controller for a synchronous buck power converter along with functional blocks for monitoring and reporting output voltage and current, input voltage and both internal and external temperatures. Coordination among multiple Zilker Labs devices and a power system host is provided by an integrated PMBus™ communications port. The resulting power system architecture is simple to manage yet flexible in all aspects of power system performance.

For converters using external FETs, the ZL2005 and ZL2006 have internal drivers. The ZL2105 and ZL2106 parts use a similar architecture to the ZL2005 and ZL2006 and further simplify the power system implementation by incorporating the switching FETs in the IC for applications requiring lower output currents. Figures 4 and 5 show typical application circuits.

### Package

The Digital-DC products are available in 36 terminal 6 × 6 mm Micro Leadframe® (MLF)® surface mount technology (SMT) packages. This package, also known as a quad flatpack no-lead (QFN), has nine terminals

per side and a central exposed leadframe paddle used to mount die and connect the signal ground (SGND). This central paddle allows heat generated within the part to be dissipated into the printed circuit board (PCB) if the PCB patterns are constructed appropriately.

The Zilker Labs parts use the saw-singulated version of the package with full leads. The terminals of this package are on 0.5 mm centers around the periphery of the part. Since the terminals of the MLF package are almost entirely under the part body, the pad pattern must be given careful attention to prevent solder bridges and opens during processing. See Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages (Reference 1) for more details. Also refer to the respective Zilker Labs product data sheets (see [www.zilkerlabs.com](http://www.zilkerlabs.com)).



Figure 1. 6 × 6 mm MLF



Figure 2. Cross Section of MLF Package

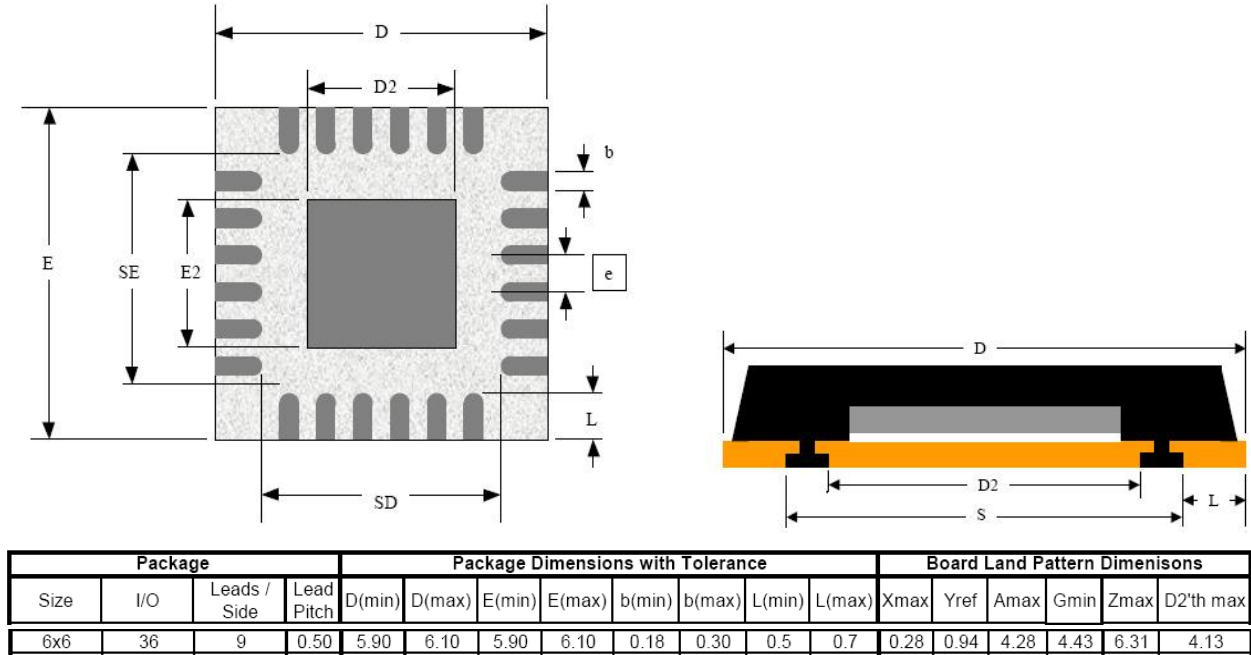


Figure 3. Dimensions of MLF Package

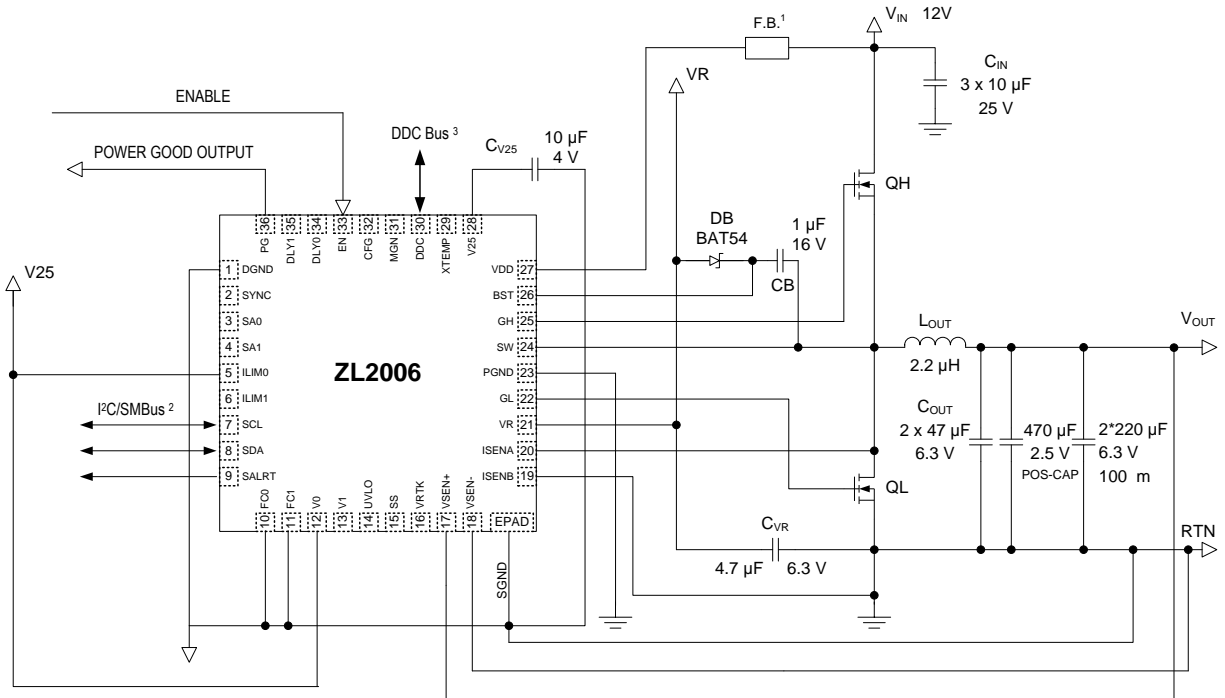


Figure 4. Application Circuit for the ZL2006

## Power Dissipation

### Power Dissipation with External Switches

The ZL2005 and ZL2006 controllers contain internal gate drivers for use with external FETs as power switches. The power dissipation of these controllers depends strongly on the particular application and components used. Since the gate drive current is normally supplied by the on-chip bias voltage regulator ( $V_R$ ), the part dissipation is greatest for driving large FETs at high frequencies and operated from high input voltages (near 14 V). The supply current ( $I_{DD}$ ) seen at the supply voltage ( $V_{DD}$ ) pin on the controllers using external switches can be divided into two currents: bias current for the controller chip and gate drive current for the external FETs. The bias current for these controllers in full operation varies with the frequency as shown in Figure 6 on page 4.

A good approximation for the  $I_{DD}$  is about 15 mA at low switching frequency. Since all of this current flows within the package to Digital Ground (DGND) and Signal Ground (SGND), the max power dissipation resulting from it is:

$$P_{chip} = V_{DDmax} \times I_{DD} = 14 \text{ V} \times 15 \text{ mA} = 210 \text{ mW}$$

The gate drive current depends entirely on the total gate charge  $Q_g$  of the FETs used and the switching frequency. The design allocation for gate drive is  $I_g = 85 \text{ mA}$ . The allocation of this current to QH and QL depends on the desired input and output voltages and the allowable partition of conduction loss between QH and QL. For combinations of frequency and gate charge that result in more drive current than 85 mA, either the frequency or the FET gate charge must be decreased.

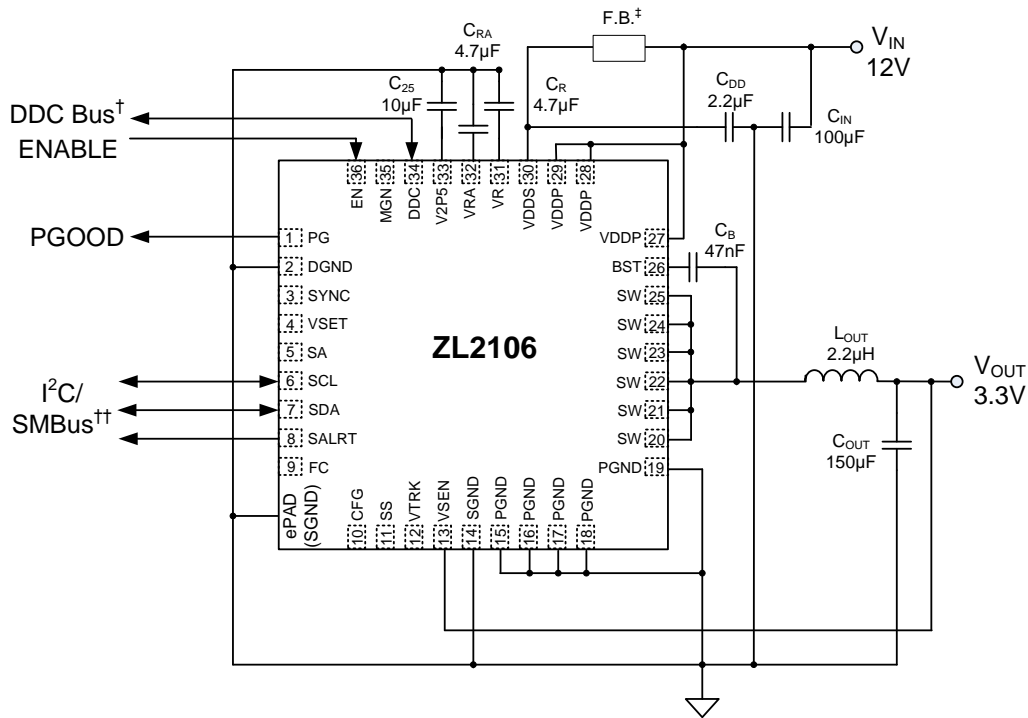


Figure 5. Application Circuit for the ZL2106

Since the drivers are within the ZL2005 and ZL2006, the power dissipated in driving the FETs also remains within the controller package. Thus, the allocated max power dissipation for the gate drive is:

$$P_g = V_{DDmax} \times I_g = 14 \text{ V} \times 85 \text{ mA} = 1.19 \text{ W}$$

when driving the power FETs directly.

For designs using external drivers, this is not a limitation. The dead-time optimization method used by these parts supports the use of external drivers without any penalty to converter efficiency resulting from FET timing. Thus, using external drivers gives additional flexibility in managing the controller package temperatures.

The maximum package dissipation is, therefore:

$$P_t = P_{chip} + P_g = 0.21 \text{ W} + 1.19 \text{ W} = 1.4 \text{ W}$$

This dissipation can be reduced by operating at a smaller input voltage, using a lower frequency, decreasing  $Q_g$  of the FETs, or using external drivers or series gate resistors.

### Power Dissipation with Internal Switches

Since the ZL2105 and ZL2106 provide internal switching MOSFETs, the primary package power dissipation is due to conduction and switching losses proportional to load current. Although there are still

bias and drive currents which contribute to power dissipation, these currents are nearly constant over different applications.

The current into the  $V_{DD}$  terminal supplies the load current and also current for bias and drive functions within the chip. The bias current  $I_{DD}$  results in power dissipation of

$$P_b = V_{DD} \times I_{DD}$$

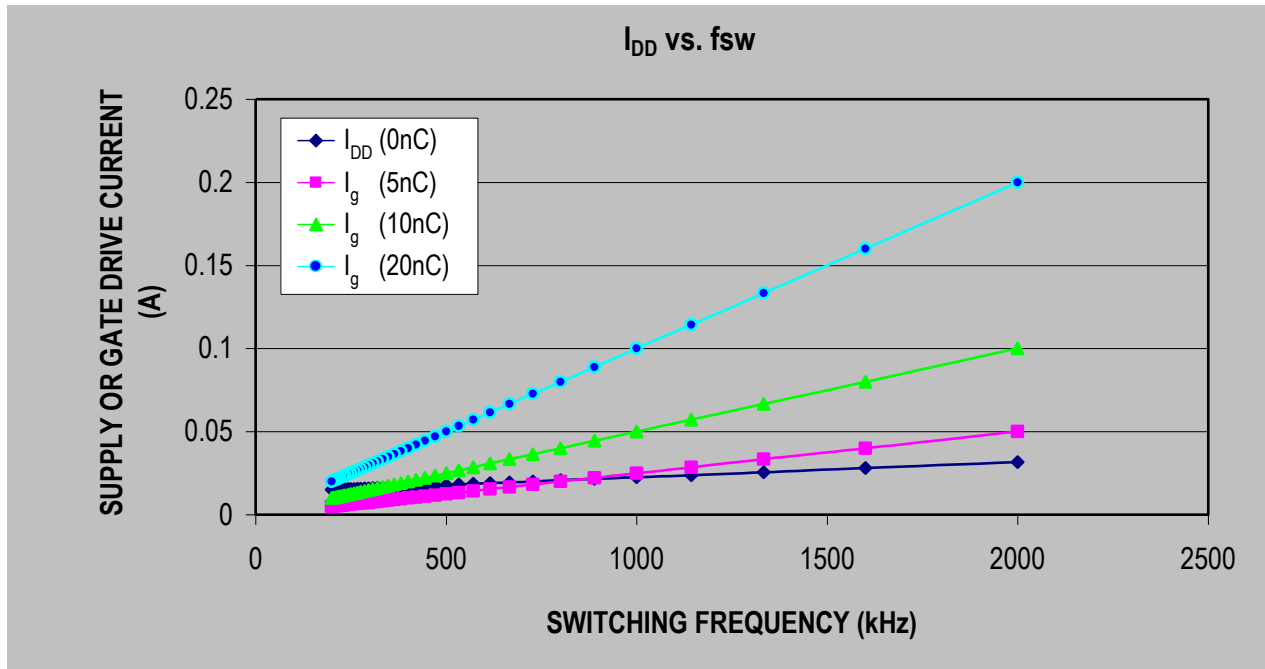


Figure 6. Derating Graph of Current vs. Frequency for Various Gate Charges

Losses in the internal switching MOSFETs can be estimated using the equations in Zilker Labs' Application Note AN2011 (Reference 3). Table 1 lists some of the parameters useful for calculating the dissipation in these parts.

**Table 1. Regulator Dissipation Parameters** (nominal, 25°C, VDD=12V, Fsw=400kHz)

	ZL2105	ZL2106
I <sub>DD(bias)</sub>	14.3 mA	13.8 mA
Q <sub>H</sub> R <sub>DS(on)</sub>	125 mΩ	60 mΩ
Q <sub>L</sub> R <sub>DS(on)</sub>	114 mΩ <sup>1</sup> 123 mΩ <sup>2</sup>	43 mΩ
α <sub>RDS</sub>	0.34mΩ/°C	0.2mΩ/°C
Q <sub>G(H)</sub>	0.7 nC	2.7 nC
Q <sub>G(L)</sub>	2.7 nC	5.07 nC
T <sub>r</sub> , T <sub>f</sub>	5 ns	2 ns

- Notes: 1. VDR = +12V.  
2. VDR = +8.5V (charge pump)

For example, consider a ZL2106 application with 3 A average current and 4 A peak current operating from 12 V to 1.2 V at a switching frequency of 500 kHz. For this voltage ratio, the operating duty ratio will be approximately

$$D = \frac{1.2 \text{ V}}{12 \text{ V}} = 10\%$$

From Eq. [15] in AN2011, I<sub>botrms</sub> = 2.90 A<sub>rms</sub>. This results in dissipation of:

$$P_{bot} = I_{botrms}^2 \times R_{ds} = 2.9^2 \times 43 \text{ m}\Omega = 362 \text{ mW}$$

in the bottom switch. For the top switch, Eq. [19] in AN2011 gives I<sub>toprms</sub> = 966 mA<sub>rms</sub>. The resulting conduction loss in the top switch is

$P_{ctop} = I_{toprms}^2 \times R_{ds} = 0.966^2 \times 60 \text{ m}\Omega = 56 \text{ mW}$  The switching losses in the top switch can be estimated from Eq. [23] in AN2011 as

$$P_{swtop} = V_{INM} \times t_{SW} \times I_{out} \times f_s$$

$$= (12 \text{ V}) (2 \text{ ns}) (3 \text{ A}) (500 \text{ kHz}) = 36 \text{ mW}$$

Taking these losses together with the chip bias power (calculated from Table 1), the package dissipation for this example is:

$$P_d = 166 \text{ mW} + 56 \text{ mW} + 362 \text{ mW} + 36 \text{ mW}$$

$$= 620 \text{ mW}.$$

## Thermal Guidelines

### Ratings

The Digital-DC parts are specified for operating in the industrial temperature range between -40°C and +125°C junction temperature (T<sub>j</sub>). The upper temperature limit is established by the characterization information available for the semiconductor process used in this part. In a typical power module application, the controller is mounted on a board subassembly with the other power supply components. On this subassembly, the primary generators of heat are typically the power FETs, the power-averaging inductor, and the controller IC. The part that reaches its temperature limit first is determined by the thermal characteristics of the module subassembly. Table 2 lists typical limiting temperatures for key components in this case.

**Table 2. Limiting Temperature for Key Components**

Component	Maximum Temperature
External Control FET	150°C junction temperature
External Synchronous FET	150°C junction temperature
PCB	95–110°C (FR-4)
PCB	150°C (Insulated Metal Substrate)
ZL2xxx die junctions	125°C

As shown in this table, the limiting temperature is usually the PCB material. To keep the board material at a temperature that will not cause long-term degradation, the thermal shutdown limit of the Zilker Labs controllers can be set to a value that protects the assembly, using either the temperature sensor within the controller package or an external temperature sensor placed near one of the power devices.

### Environment

When the power supply is not on a subassembly, the primary generator of heat may be the load itself, usually a high density digital or mixed-signal IC. Because the power converter is typically about 90% efficient, the load typically dissipates about 9 times the power dissipated in the power supply components. In many cases, the load has additional cooling in the form of a heatsink and additional airflow.

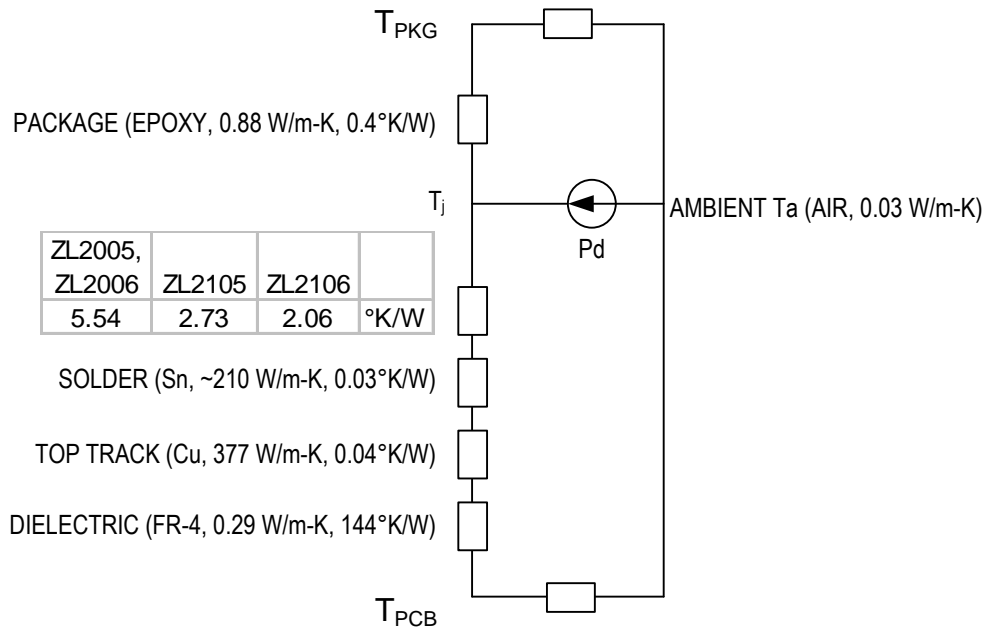


Figure 7. Thermal Model (assumes no spreading vias or planes)

### Thermal Circuit

The thermal model of the controller in its environment can be treated as an equivalent electrical model (see

). This model applies to both the controllers with external FETs and the regulators with internal FETs; however, the model must be modified according to the geometries of the layout patterns discussed next.

### PCB Layer Structures

The thermal model can be modified by the choices and patterns made on the PCB layers. Since the MLF package has an exposed leadframe paddle, the majority of the heat dissipated in the controller package can be transferred effectively to the PCB through a via pattern under the controller package [1].

Table 3. Recommendations for single-sided PCB mounting (Tamb=50°C, VDD=12V, Fsw=400kHz)

ZL	2005	2006	2105	2106
Max I <sub>out</sub> (avg)	Q <sub>GL</sub> +Q <sub>GH</sub> =70nC	Q <sub>GL</sub> +Q <sub>GH</sub> =70nC	1.25A	1.85A
Max I <sub>ripple</sub> (p-p)			1.25A	1.85A

shows the recommendations for each part on a single-sided PCB. The only thermal options for a single-sided PCB are the tracks leaving the part and a top-mounted heatsink. No significant supplemental track can be attached to the leadframe paddle and escape the terminal ring to facilitate heat spreading in a single-sided layout. The best scenario for this layout is to pass the connection for SGND through the terminal for Digital Ground (DGND) on its way to termination at

For a two-sided PCB, the mounting layer layout design should follow the recommendations for a single-sided PCB (consider the mounting layer as the topside for discussion purposes). The opposite (bottom) layer should be a copper pour at least 25 mm square wherever allowed by other connections. This plane should be tied to the topside package paddle pad with thermal vias. Thus, the plane also becomes the SGND electrical connection. For a thermal plane, the layout connections should be arranged so that the plane is cut only in radial patterns from the part so that the heat flow through the copper plane layer is not interrupted.

The recommendations in [1] show that a via pattern of 1.0 mm centered in a 5 × 5 array of 0.3 mm vias embedded in a leadframe paddle yields a thermal resistance of ~ 25.5°C/W on a PCB using one signal layer and two ground plane layers under the part. The two-sided PCB would have approximately 20% higher thermal resistance for the same patterns.

the output return. The best thermal performance would be achieved with tracks that widen to the terminal pitch (~0.5 mm) as soon as possible after leaving the PCB pad on each terminal. These wide tracks should extend ~25 mm away from the package, if possible, to allow the best heat spreading into the PCB. A top-mounted heatsink helps substantially, especially if there is some airflow. The junction-to-top surface thermal resistance is about 0.4°C/W.

For a PCB that has four or more layers, inner layers can be used to spread the thermal energy dissipated in the controller. Since the MLF package is a surface-mount part, all connections to the part are on the mounting (top) layer. Some of these connections must jump through a via to another layer (usually the opposite outside layer) to run to their respective connections. In most applications, one of the inner layers will be a ground plane, which can be used as the SGND plane. Another inner layer can be used for a V<sub>R</sub> plane. Choosing the dimensions and connections to these planes can maximize the thermal environment around the part.

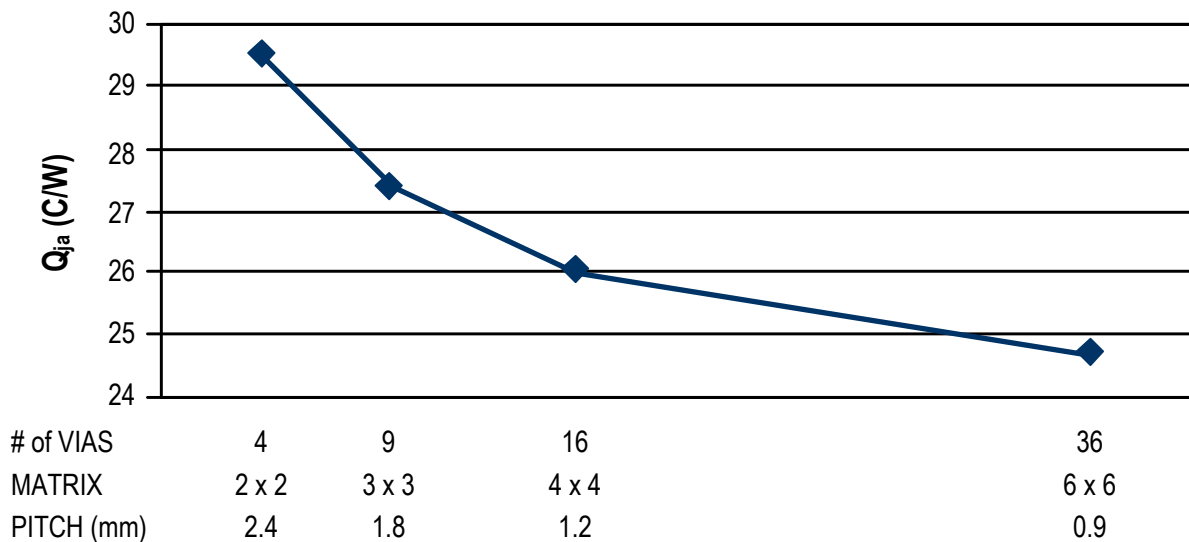


Figure 8. Effect of Number of Thermal Vias on Package Thermal Performance

### Thermal Pattern Design

To design an appropriate thermal pattern, the layer usage of all available layers, the number and size of vias under the controller package, the solder stencil pattern for depositing solder on the paddle pad, and treatment of the vias to prevent voids must be considered.

The via pattern used under the controller part depends on many factors, such as the copper thickness of the board, the cost of drilling small holes, and the thickness of the solder stencil for depositing sufficient solder. Information on the thermal performance of different via patterns is shown in Figure 8.

Based on Figure 8 and similar thermal simulations, an array of thermal vias should be incorporated at 1.0 – 1.2 mm pitch with a via diameter of 0.3 – 0.33 mm. An example is shown in Figure 9.

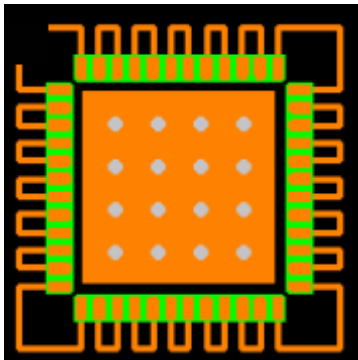


Figure 9. Thermal Via Pattern Example (4 × 4 array)

Other guidelines can enhance the thermal environment. For example, using more plated copper will enhance the conductivity of planes and vias to transfer heat away from the part more effectively. Where possible, depending on the electrical coupling, overlapping multiple planes with the SGND plane can provide a more conductive matrix to spread the heat. If the ZL2005 or ZL2105 is mounted on a module, placing the device and its planes near surface-mount standoffs will help transfer heat to the host board. All available area should be filled with copper to enhance the thermal spreading.

To properly solder the MLF package in automated assembly processes, the deposition of solder paste on the paddle pad should be controlled by a grid pattern. As shown in [1], a rectangular array provides good solder coverage while still allowing outgassing during reflow. If a 5 × 5 array of vias on 1.0 mm centers is used, then a 5 × 5 grid of 0.7 mm rectangles centered on the vias should provide a good compromise between solder coverage and assembly flaws

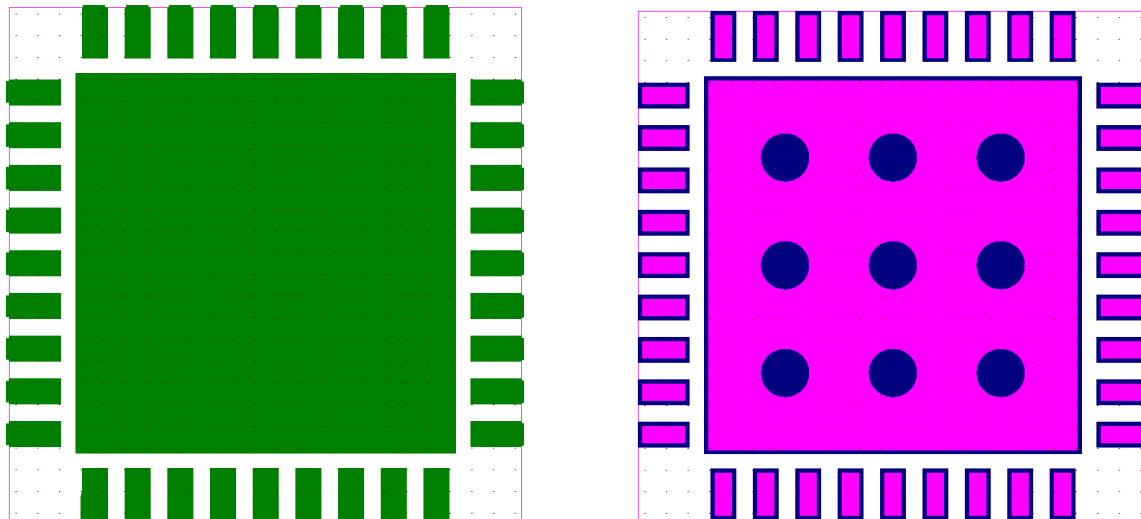


Figure 10. Mounting Pattern for the MLF Package



To prevent solder flow into the thermal vias, soldermask can be used to cover the vias. The recommendations in ref. [1] provide four methods of covering vias. For most boards, tenting (covering) the thermal vias (with soldermask) on the bottom (opposite the part) will provide the desired solder retention.

**PCB Pattern**

In keeping with the package manufacturer’s recommendations, Figure 10 shows the mounting pattern for this package.

**Layout Guidelines for External Switch Products**

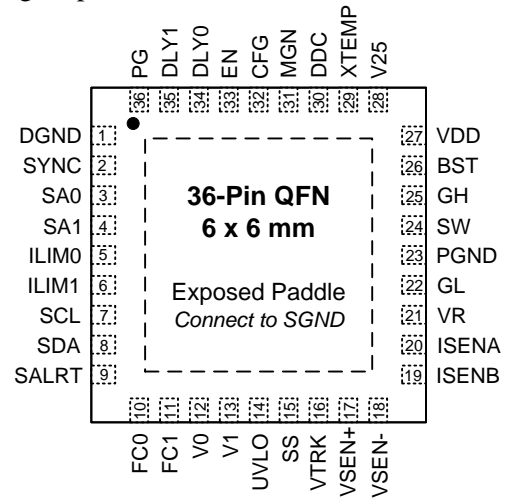
**PCB Layer Usage**

The connections to the controller IC can be divided into five classes (see Figure 11). The recommended layer usage assumes the controller is mounted on the topside of the PCB. If mounted on the bottom, the layer order can be reversed.

This assignment of layers accomplishes several purposes. First, the SGND plane allows low-level signals and decoupling to be separated from high-level signals and power waveforms. It also allows a short thermal connection to the leadframe paddle with thermal vias to enhance heat spreading from the part. The low-level signals are immediately adjacent to the

SGND plane so that minimal capacitive crosstalk is induced. The SGND plane should not underlie the drive signals, power components, and related parts.

Second, the high amplitude drive signals are on the same layer as the low-level analog signals. In fact, all the drive signals are on one edge of the package and conveniently can be isolated from the low-level signals without inserting the extra impedance of vias into the drive signal path.



**Figure 11. ZL2006 Terminal Assignment (top view)**

Third, the assignment of high speed digital signals to the side of the board opposite the analog signals ensures that a return plane lies between the digital signals and the low level signals to minimize coupling and disturbances between them. The drivers connected to the digital signals generally return to the same power stage output return connection as the power ground (PGND) plane, thus minimizing the loop area of the digital signals.

## Critical Loops

In the synchronous buck circuit, certain critical circuit loops should have a minimal loop area to ensure the best operation of the circuit. These loops are the gate drive source and sink loops, the power transistor decoupling loop, and the output current sense loop (see Figure 12). Each gate driver has two loops associated with it that should be kept short for best switching function. For the low-side driver GL, the path discharging the FET gate capacitance includes the connection from the FET gate terminal to the GL terminal and the connection from PGND back to the

FET source terminal. The charging loop involves the  $V_R$  decoupling capacitor and ground connection, the GL connection to the FET gate, and the return from the FET source to the  $V_R$  decoupling capacitor.

The loops for the high side FET driver are similar, with driver signals BST, GH, and SW replacing  $V_R$ , GL, and PGND.

The power FET bypass loop involves the drain and source of the control MOSFET, the drain and source of the synchronous MOSFET and the bypass capacitors across the input voltage to the buck regulator. This loop must provide the short-term current to transition the switching node SW from PGND to  $V_{IN}$  and charge parasitic capacitances on SW when the control FET is turned ON. This loop also determines the magnitude of voltage overshoot on SW and thus the maximum input voltage to the buck regulator before one of the semiconductor breakdown ratings is reached.

**Table 4. Pin Usage Description for the ZL2005 and ZL2006**

Class	Examples	Characteristics	Layer	Recommendations
Digital Signals	SYNC, SCL, SDA, SALRT, DDC	High speed transitions	4 (Bottom)	Do not run parallel to analog signals or close to drive signals.
Analog Signals	VSEN, ISENA, ISENB, VTRK, XTEMP	Low amplitude signals (mV)	1 (Top)	Do not run parallel to digital signals or close to drive signals. Run signals paired with return tracks to minimize loop area.
Drive Signals	GH, GL, SW, BST	High amplitude signals (5–20 V, 2–5 A) with fast transitions and significant parasitic disturbances	1 (Top)	Run signals paired with source and return tracks to minimize loop area. Since these carry higher currents, the track width should be ~0.5mm or larger.
Signal Ground	SGND	Reference surface for low-amplitude signals	2	Run as a plane or wide track to the negative terminal of the load (ZL2005) or negative terminal of the output capacitors (ZL2006).
Power	PGND, VR	Return and source paths for high currents	3	Separate from all other connections unless part of a well-decoupled plane structure.

The output current sensing function of the ZL2005 and ZL2006 can be configured at least four ways for current protection and reporting. In all of these configurations, the current sense signal is a small amplitude (100 mV full-scale or less) to maintain a low parasitic power loss on the current-sensing device. Thus, the current signal ISENA–ISENB must carry the signal to the controller with minimal distortions from coupled noise or voltage offsets. The best way to do this is to run the tracks side by side at minimum spacing, away from high-level and power tracks and adjacent to the SGND layer from the current sensing element (FET, shunt, or capacitor) to the controller

terminals. Any loop area in these tracks, especially near output or input filter inductors, can cause undesirable magnetically-induced voltage disturbances.

Two signals used in the controllers measure the output voltage and current of the power supply. For best performance and accuracy, these signals should employ four-terminal (Kelvin) connections. These output voltage signal is sensed by the connection pairs VSEN, SGND (ZL2005, ZL2105, ZL2106). For the ZL2006, the voltage measurement is made with the true differential sense connections VSEN+ and VSEN-. The load current signal is sensed by ISENA and ISENB for the ZL2005 and ZL2006.

### Four-Terminal Connections

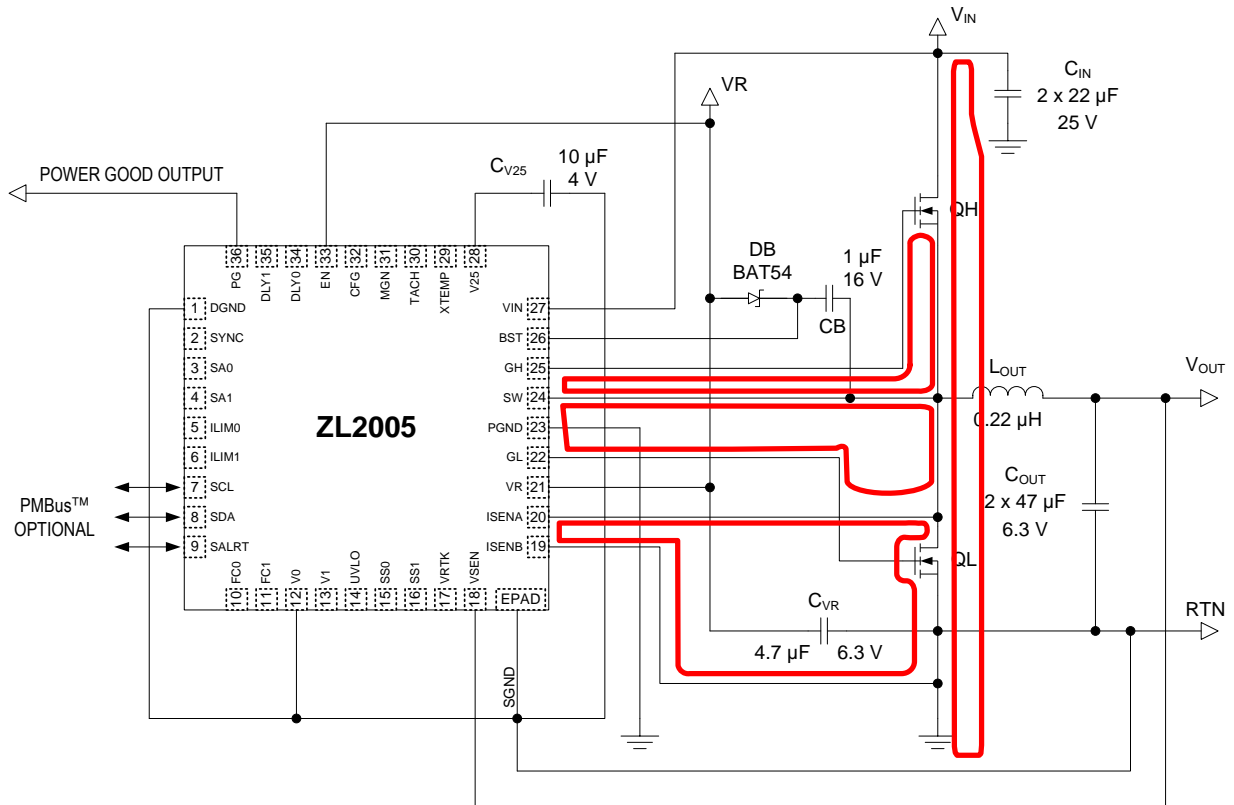


Figure 12. ZL2005 Critical Loops

Voltage regulation should typically be most accurate at one point, usually at the connections to the load. Although the ZL2005 does not have true differential voltage sense inputs, the VSEN and SGND connections can be treated like sense lines for point-of-load (POL) applications. The VSEN terminal should be connected to the positive load terminal at the load. This connection prevents the current-carrying track from influencing the regulated voltage due to ohmic drops. Since very little current is in this input, the track width can be the minimum line width for the PCB processing.

The SGND terminal should be run as a wide track or cut-off plane segment from the controller to the negative terminal of the load before joining the negative current-carrying conductor. Since this terminal is also the  $I_{DD}$  current return for the controller, the impedance of the SGND conductor should be kept as small as possible. The SGND supply current for the ZL2005 is about 5-15 mA (depending on frequency); therefore, the output voltage regulation error is about 5-15 mV per ohm of SGND resistance. Voltage drops in the power conductors should be limited to no more than 150 mV per leg.

In most PoL applications, the distances from the controller to the regulated load will be very short and massive planes will carry the currents. If an open connection on either VSEN or SGND (such as a connector, a wire, or SMT solder joints) is possible, then the user should consider placing “default” resistors near the controller IC from VSEN to the positive power output or SGND to the negative power output. If the voltage sense connection opens, these resistors will maintain the connection to the output and keep the supplied voltage under control. These resistor values should be in the 1 to 4.7  $\Omega$  range.

The ZL2006 differential sense connections allow for additional flexibility in planning the Kelvin connections. For this part, the “default” resistors can be higher impedance, on the order of 20  $\Omega$  to 50  $\Omega$ . The return sensing connection for this resistor would be from VSEN- to PGND. The SGND plane for the ZL2006 should connect to the PGND plane at only one point, typically the negative terminal of the output capacitors.

The current sense connections ISENA and ISENB should connect directly to the current sensing element (FET, resistor shunt, or averaging capacitor), without touching any current-carrying tracks [2]. When sensing across a MOSFET, the current sense connections should be as close as possible to the solder connections to the FET, because the tracks and vias are carrying large currents and may have greater voltage drops than the expected current sense signal. Some low-value resistors used for current sensing have four terminals intended for Kelvin connections.

A similar dedicated connection should be used for analog signal XTEMP, which must provide signals in the few millivolt (mV) range. The return path for the external temperature-sensing element (usually a diode junction) is SGND. Like ISENA and ISENB, the tracks for XTEMP and SGND should run as a pair from the sensor device to the controller terminals.

## Layout Guidelines for Internal Switch Products

### PCB Layer Usage

Like the ZL2006, the connections to the ZL2105 and ZL2106 can be divided into classes according to the characteristics of each connection. But since more of the circuit is integrated in the IC, there are only four classes of external connections (see Table 5). Here also, the recommended layer usage assumes the integrated regulator is mounted on the topside of the PCB. If mounted on the bottom, the layer order can be reversed. Please refer to the sections for external switches for the motivation for these classes.

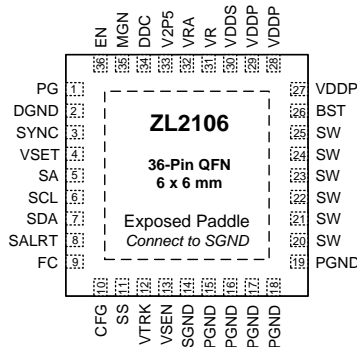


Figure 13. ZL2106 Terminal Assignment (top view)

### Critical Loops

Since the drivers and load switching FETs are integrated into the ZL2105 and ZL2106, the only loop which is critical external to the part is the  $C_{IN}$ , VDDP, and PGND decoupling loop for the power FETs as shown in the typical application circuit (Figure 5). The capacitors for this loop should ideally remain on the same side of the PCB as the IC, and should be physically very close to the IC to minimize inductances.

### Four-Terminal Connections

Since current sensing is integrated into the internal switch regulators, the only connections requiring attention to four-terminal (Kelvin) connections are the output voltage sensing (VSEN and SGND or VSEN+ and VSEN-). The earlier recommendations for the external switch parts apply also to the integrated switch parts for these terminals.

Table 5. Pin Usage Description for the Integrated Regulators

Class	Examples	Characteristics	Layer	Recommendations
Digital Signals	SYNC, SCL, SDA, SALRT, CP1, CP2	High speed transitions	4 (Bottom)	Do not run parallel to analog signals or close to drive signals.
Analog Signals	VSEN, VTRK, XTEMP, VRA	Low amplitude signals (mV)	1 (Top)	Do not run parallel to digital signals or close to drive signals. Run signals paired with return tracks to minimize loop area.
Signal Ground	SGND	Reference surface for low-amplitude signals	2	Run as a plane or wide track to the negative terminal of the load.
Power	VDDP, PGND, VR, SW, BST	Return and source paths for high currents. May have fast transitions and significant parasitic disturbances	3	Separate from all other connections unless part of a well-decoupled plane structure. Switching signals (SW, BST) should have only enough track width to carry the required current with acceptable voltage drop.

## Appendix A

### ZL2005 Circuit Examples

Figure 15–Figure 16 show some representative examples of recommended layout practices for the connections to the ZL2005 in different assembly configurations. The examples are for two PCB layers with one-sided mounting of (major) components, four PCB layers with one-sided mounting, and four PCB layers with two-sided mounting of (major) components.

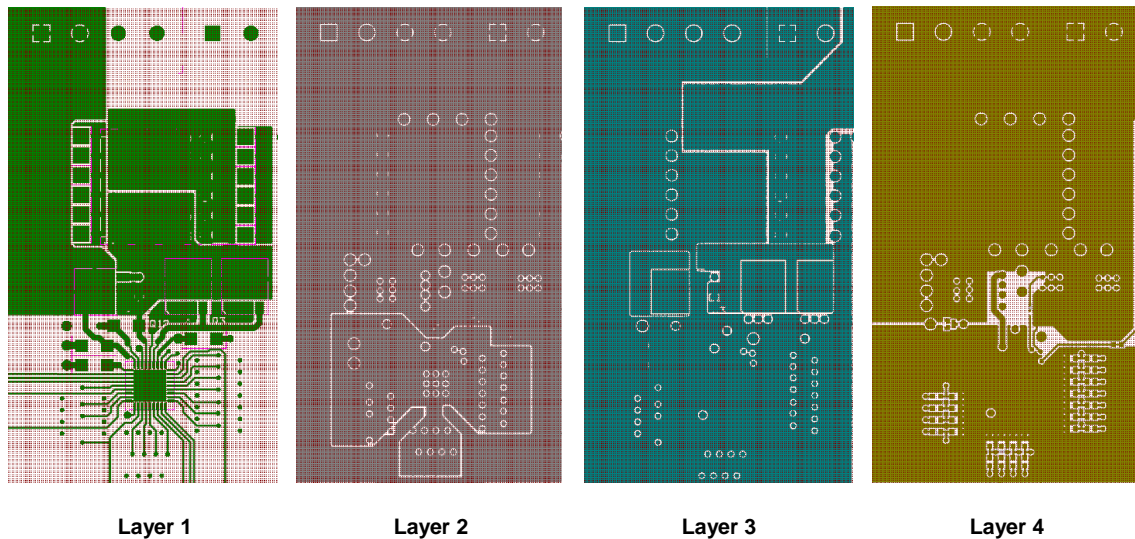


Figure 15. Example Layout – Four-layer PCB with One-Sided Mounting (Except Small Discretes)

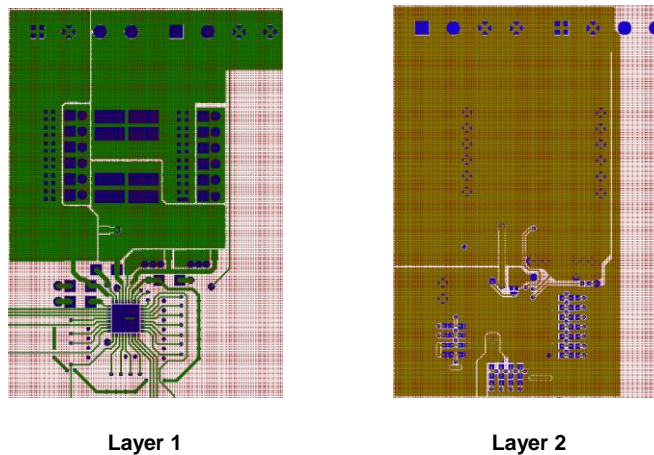


Figure 14. Example Layout – Two-layer PCB with One-Sided Mounting (Except Small Discretes)

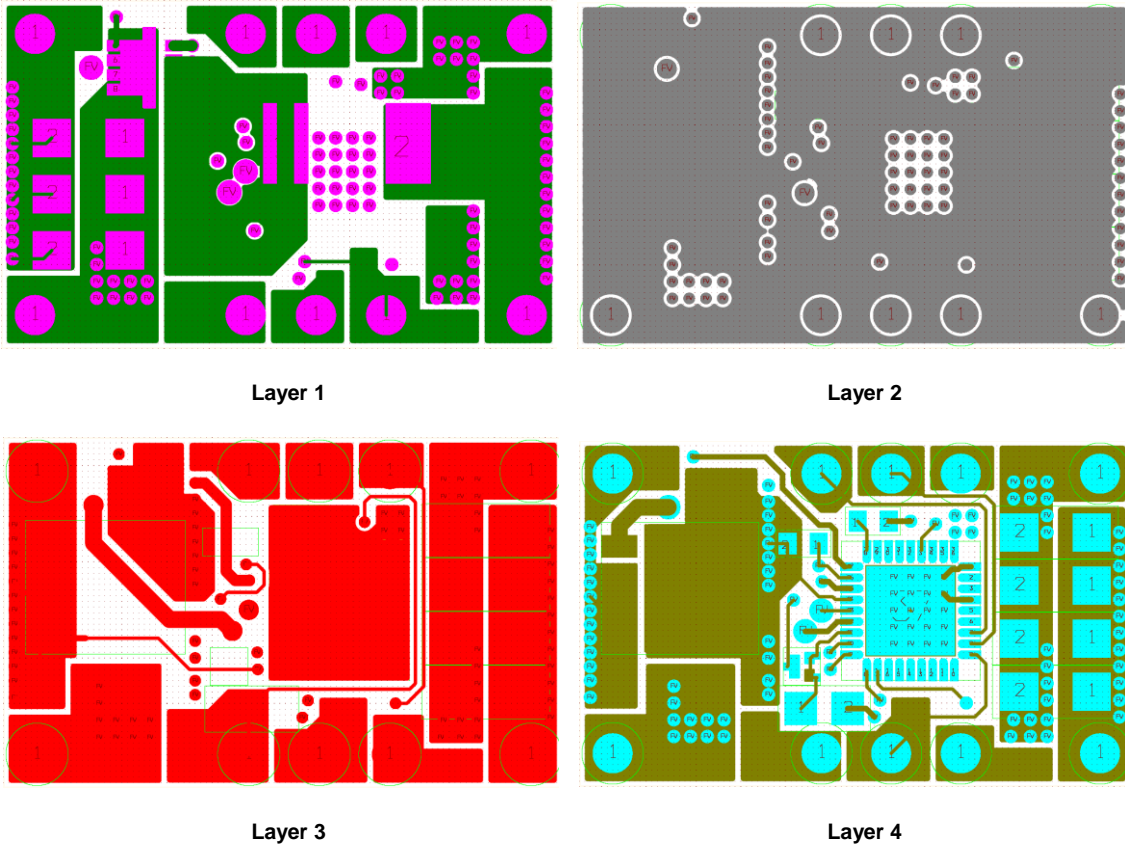
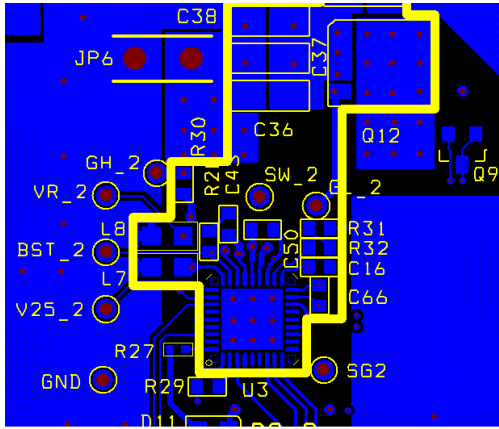


Figure 16. Example Layout – Four-layer PCB with Two-Sided Mounting

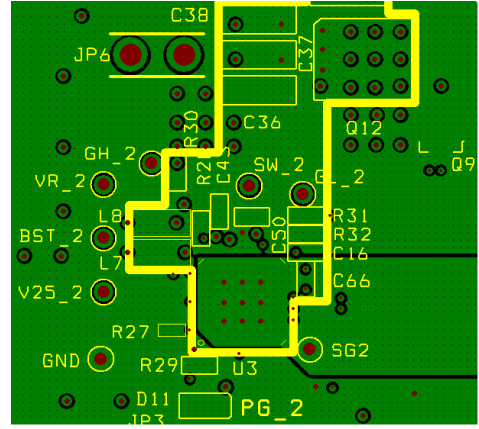
## Appendix B

### ZL2006 Circuit Examples

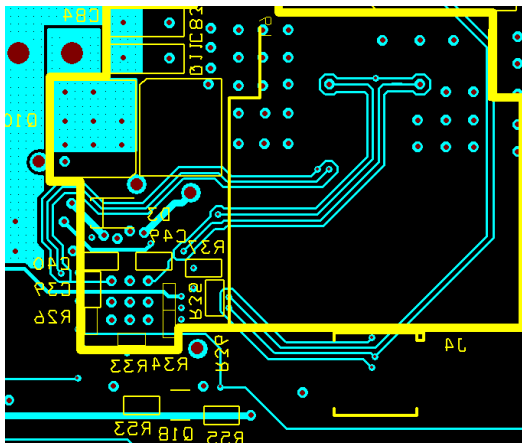
Figure 17 shows a representative example of recommended layout practices for the connections to the ZL2006. The example shows a six layer PCB with two-sided mounting of (major) components.



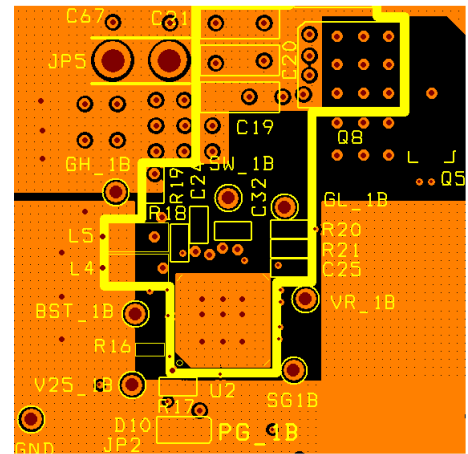
Top Layer



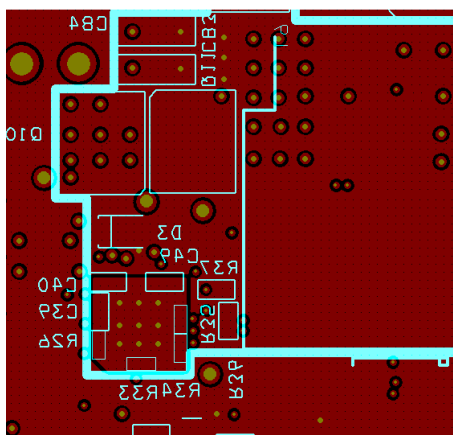
Inner Layer 1



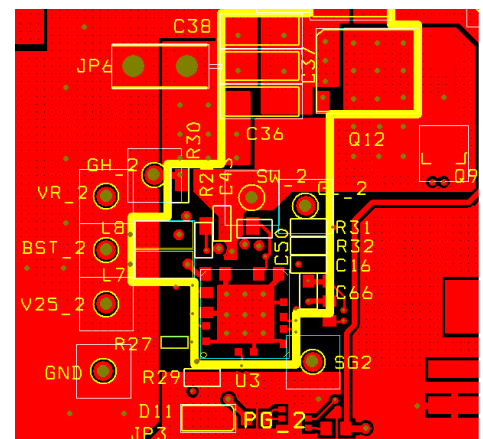
Inner Layer 2



Inner Layer 3



Inner Layer 4



Bottom Layer

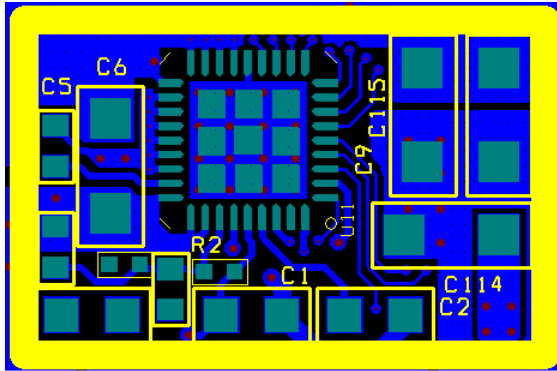
Figure 17. ZL2006 Example Layout - Six Layer PCB



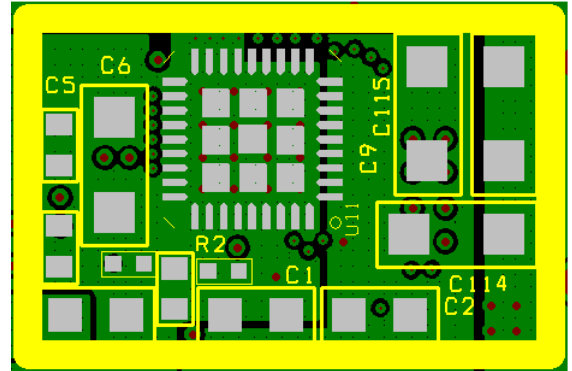
## Appendix C

### ZL2106 Circuit Examples

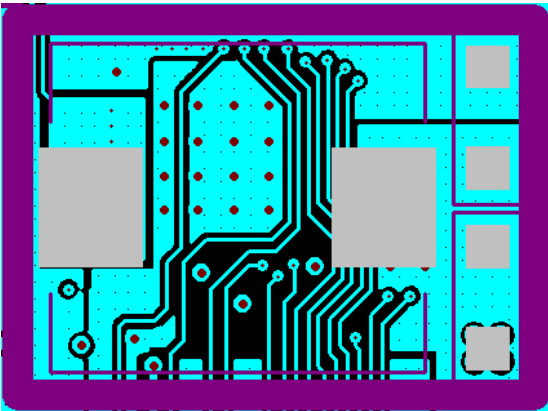
Figure 18 show a representative example of recommended layout practices for the connections to the ZL2106. The example shows a four layer PCB with two-sided mounting of (major) components.



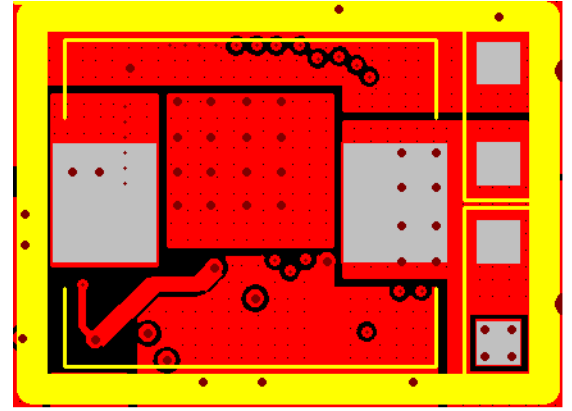
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 18. ZL2106 Example Layout - Four Layer PCB

## References

- [1] *Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame® (MLF®) Packages, Rev. E*, Amkor Technology, Inc., December 2003.
- [2] AN2015 – *ZL2005 Current Sensing Techniques*, Zilker Labs, Inc., 2005.
- [3] AN2011 – *Component Selection*, Zilker Labs, Inc., 2005.
- [4] *ZL2005 Data Sheet*, Zilker Labs, Inc., 2006
- [5] *ZL2006 Data Sheet*, Zilker Labs, Inc., 2008
- [6] *ZL2106 Data Sheet*, Zilker Labs, Inc., 2008
- [7] *ZL2105 Data Sheet*, Zilker Labs, Inc., 2006

## Revision History

Date	Rev. #	
10/20/05	1.0	Initial release
9/7/06	2.0	Added ZL2105 sections, revised thermal circuit
6/17/08	2.5	Added ZL2006 and ZL2106.
6/24/08	2.6	Minor text edits
5/01/09	AN2010.0	Assigned file number AN2010 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read "Intersil and it's subsidiaries including Zilker Labs, Inc." No changes to datasheet content.

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