Introduction

This application note presents the method of achieving a defined phase relationship between the input reference clock and output clock for IDT UFT3G Zero-Delay Buffers. Outputs can be selectively divided, multiplied or inverted while still maintaining very low input to output skew.

The UFT3G family consists of the six devices with the properties pertinent to zero delay buffers, as summarized in Table 1 below.

Table 1: Summary of UFT 3G Family

Part Number	Number of Inputs	Number of Outputs	Number of APLLs	Max Number of ZDB	Jitter Performance
8T49N281	2	8	1	1	Standard UFT3G
8T49N282	4	8	2	2	Standard UFT3G
8T49N283	2	8	2	1	Standard UFT3G
8T49N285	2	8	1	1	Improved UFT3G
8T49N286	4	8	2	2	Improved UFT3G
8T49N287	2	8	2	1	Improved UFT3G

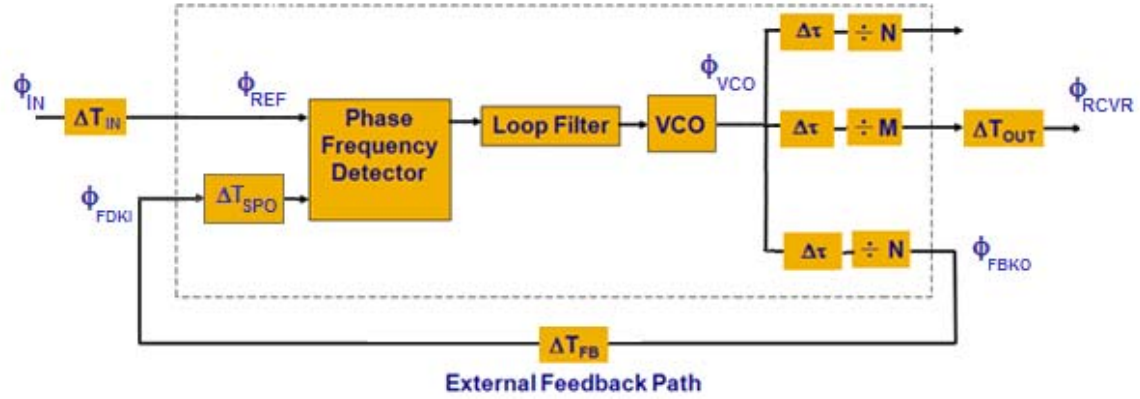
Note: Fully hitless switching is not supported when external loopback is being used, so only the phase-slope limiting is selected for the switches between input references or enters/leaves the holdover state in this ZDB application.

Zero Delay Buffer Architecture

A zero-delay buffer is a device that can fan out one clock signal into multiple clock signals with zero delay between the input reference to the buffer and the inputs of the downstream clock receivers driven by the zero delay buffer. The device is well suited for a variety of clock distribution application requiring tight input-output and output-output skew relationship. A simplified block diagram of a ZDB is shown in Figure 1 below where ΔT_{SPO} is called the Static Phase Offset and is due to internal input and feedback clock Pre-divider and Phase/Frequency Detector delays. Since this is usually frequency independent, it is has units of time delay and is shown as such in the block diagram.

A feature of the UFT3G PLLs is that a clock input can be specified as the feedback input to the PLL phase detector rather than an internal connection. Board-level trace-length mismatches can be compensated for in order to achieve a defined skew relationship between the input and output clock as shown in Figure 1 below. “$\Delta\tau$” in the part can fine tune delay line to manage the clock skew and the delay variations in the other six output clocks.

Figure 1. UFT3G Architecture Applied to a Single Zero-Delay Buffer



The relationship between the reference phase ϕIN and the phase at the inputs to the downstream clock receivers, ϕRCVR is developed below. In principle, the delay of the feedback path is shown to allow any skew between ϕIN and ϕRCVR.

Working back from the phase detector inputs, the input phase can be related to the output phase of the feedback path as below where f is the frequency of the input phase reference.

$$\phi_{REF} = \phi_{FBKI} + 2\pi f \Delta T_{SPO}$$
$$\phi_{IN} + 2\pi f \Delta T_{REF} = \phi_{FBKI} + 2\pi f \Delta T_{SPO}$$

From the external feedback path;

$$\phi_{FBKI} = \phi_{FBKO} + 2\pi f \Delta T_{FB}$$

The input phase can be related to the feedback output phase as follows:

$$\phi_{IN} + 2\pi f \Delta T_{REF} = \phi_{FBKO} + 2\pi f \left(\Delta T_{FB} + \Delta T_{SPO}\right)$$

At the clock receiver, the phase at the receiver can be related back to the phase of the VCO:

$$\frac{\phi_{VCO}}{M} + 2\pi f \Delta T_{OUT} = \phi_{RCVR}$$
$$\phi_{VCO} = M\left(\phi_{RCVR} - 2\pi f \Delta T_{OUT}\right)$$

These relationships are put together for the dependence of the clock receiver input phase to the UFT3G input phase.

$$\phi_{IN} + 2\pi f \Delta T_{REF} = \phi_{FBKO} + 2\pi f \left(\Delta T_{FB} + \Delta T_{SPO}\right)$$
$$\phi_{IN} = \frac{\phi_{VCO}}{N} + 2\pi f \left[\Delta T_{FB} + \Delta T_{SPO} - \Delta T_{REF}\right]$$
$$= \frac{M}{N}\left(\phi_{RCVR} - 2\pi f \Delta T_{OUT}\right) + 2\pi f \left[\Delta T_{FB} + \Delta T_{SPO} - \Delta T_{REF}\right]$$
$$= \frac{M}{N}\phi_{RCVR} - 2\pi f \left[\Delta T_{REF} - \Delta T_{SPO} + \frac{M}{N}\Delta T_{OUT} - \Delta T_{FB}\right]$$
$$\phi_{RCVR} = \frac{N}{M}\phi_{IN} + 2\pi f \left[\left(\Delta T_{REF} - \Delta T_{SPO} + \frac{M}{N}\Delta T_{OUT}\right) - \Delta T_{FB}\right]$$

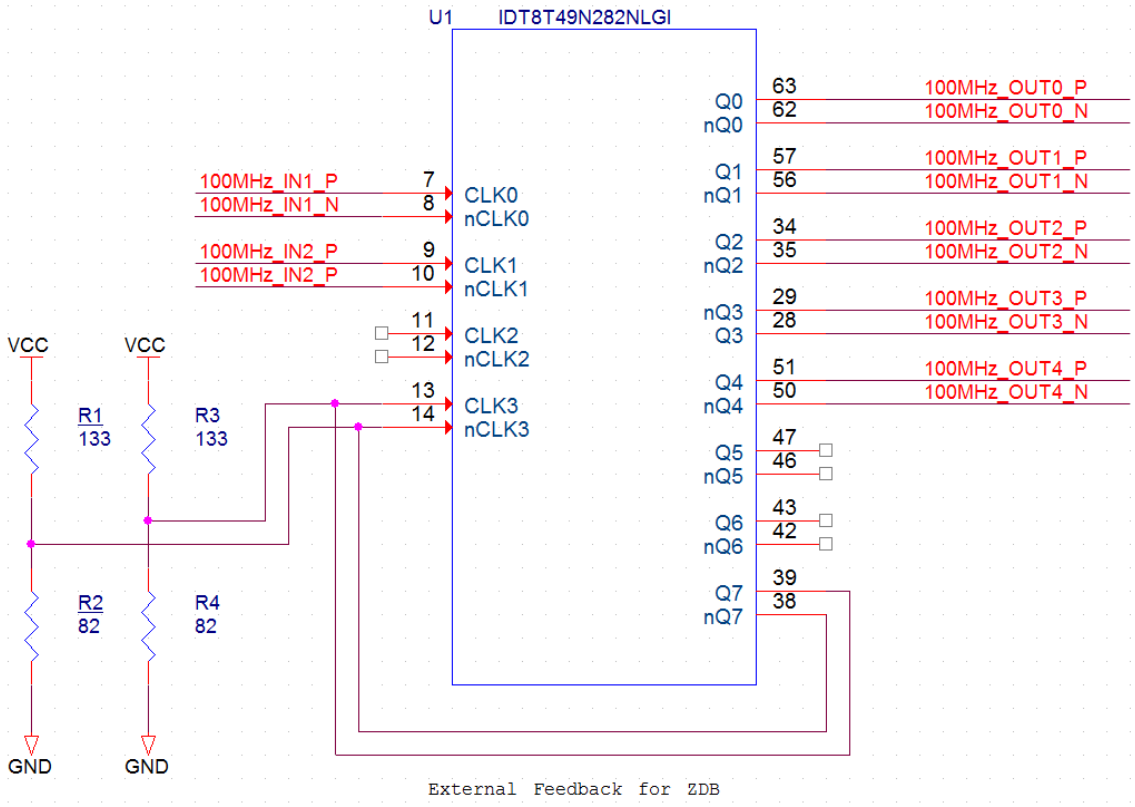
By adjusting the external path length, ΔT_{FB}, on the printed wiring board to cancel the cumulative effect of ΔT_{OUT}, ΔT_{REF} and ΔT_{SPO}, the output clock can be timed to arrive at the receiver phase-aligned with the input clock. That is when ϕ_{IN} equals zero, ϕ_{RCVR} equals zero. In general, ΔT_{SPO} depends on the particular settings of the internal dividers and the phase/frequency detector comparison frequency.

In general, phase advance or a smaller phase delay is also possible, but there is a practical limit to the maximum delay achievable with a length of a circuit board trace due to the propagation velocity of the feedback transmission line (165ps/in typically). The effective ΔT_{FB} can also be increased by inverting the feedback output. In cases where inversion of the feedback clock does not generate enough additional delay, an RC network can be used to increase the effective ΔT_{FB}.

Procedure

The user must first connect the 8T49N282 as a Zero Delay Buffer as shown schematically in Figure 2.

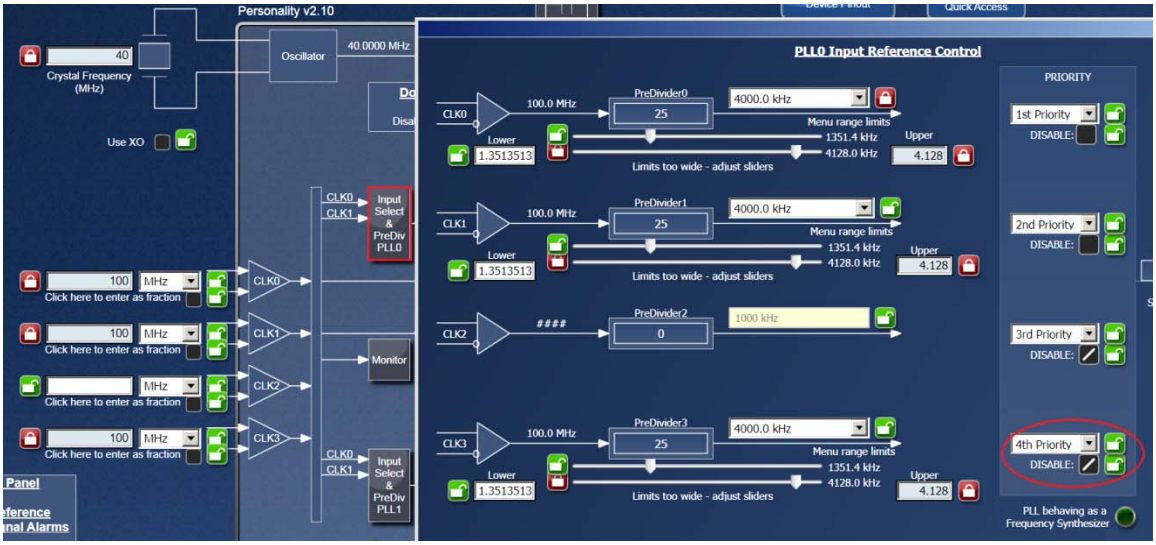
Figure 2. Schematic for Zero Delay Buffer Application



After the 8T49N282 is connected as a ZDB, the device must be configured as a ZBD in Timing Commander as shown in the following steps.

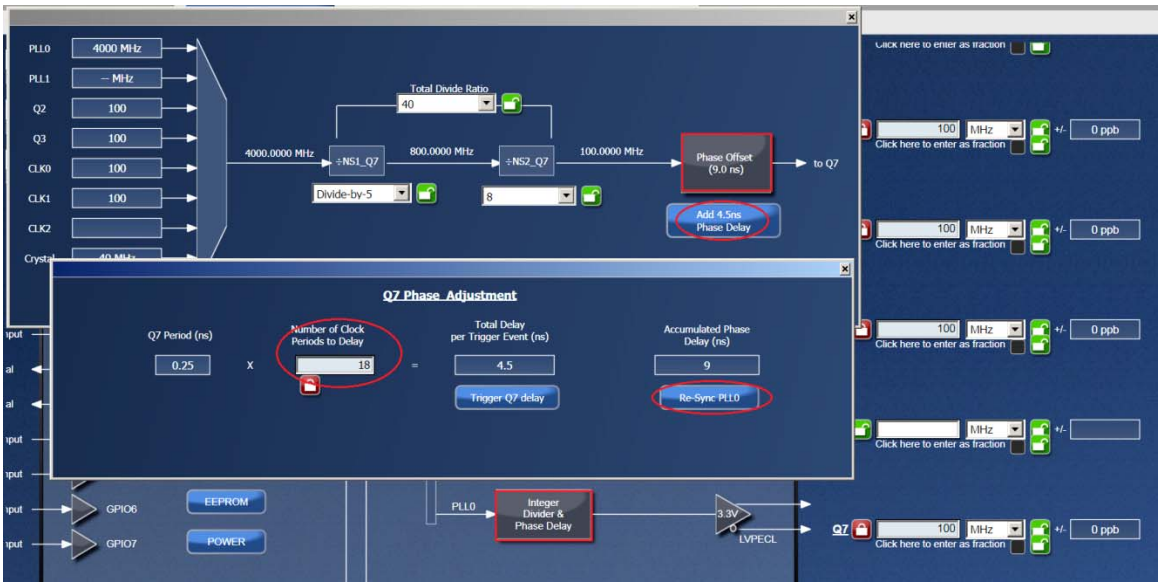
1. Click “Input Select & PreDiv PLL0”, select the PFD frequency and disable the selection for the feedback input as shown in Figure 3.

Figure 3. PLL0 Input Reference Control



2. Click on “Integer Divider & Phase Delay”, then select “Phase Offset” box and click “Re-Sync PLL0” to trigger all outputs synchronization from PLL0, and entering desired phase offset in the feedback path for the external trace compensated as in Figure 4. Generally the trace lengths for all outputs to their respective clock receivers should be the same length as the external feedback path, otherwise, the phase offset of each output need to be individually adjusted for the different trace length to the corresponding clock receiver.

Figure 4. Setting the Phase Offset



The description in the datasheet, shown in Table 1, lists the steps in detail.

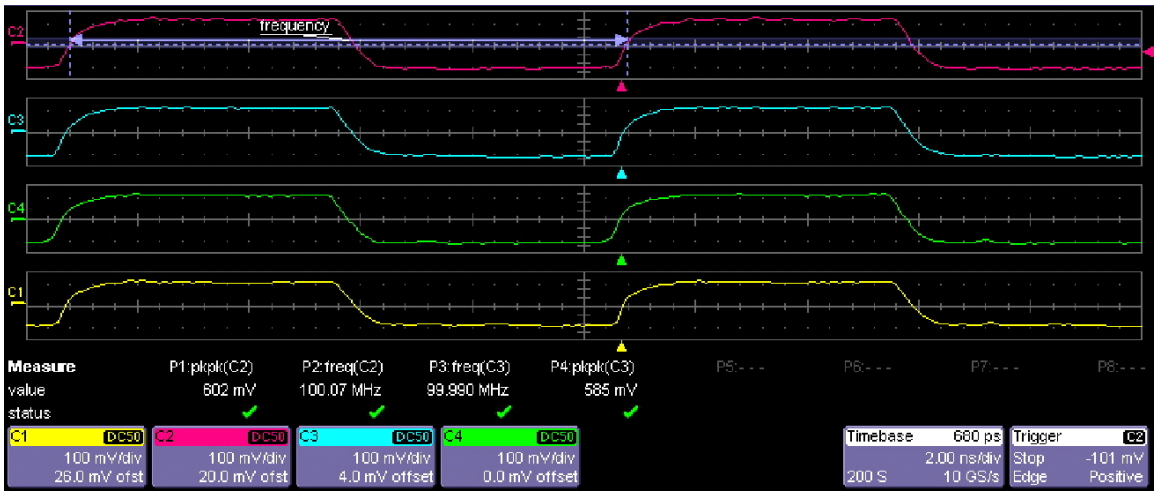
Table 2: Output Clock Control Register

Output Clock Source Control Register Block Field Locations								
Address (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00A8	Rsvd		PLL1_SYN	PLL0_SYN	CLK_SEL3	CLK_SEL2	CLK_SEL1	CLK_SEL0
00A9	Rsvd	CLK_SEL5[2:0]			Rsvd	CLK_SEL4[2:0]		
00AA	Rsvd	CLK_SEL7[2:0]			Rsvd	CLK_SEL6[2:0]		
00AB	11		11		Rsvd		Rsvd	

Output Clock Source Control Register Block Field Descriptions			
Bit Field Name	**Field Type**	**Default Value**	**Description**
PLL1_SYN	R/W	0b	Output Synchronization Control for Outputs Derived from PLL1. Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0.
PLL0_SYN	R/W	0b	Output Synchronization Control for Outputs Derived from PLL0. Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0.

3. If the external feedback path can't fully compensate the delay of the clock between the reference and the Buffer output, the user can adjust the Number of Clock Period Delay through COARSE7[4:0] of register 0xA5, then set CRSE_TRG7 of register 0x9D to trigger Coarse phase adjustment for OUT7, a 4GHz VCO gives a step size of 250ps (For Q2/Q3, the step size is 16ps). By the method adjusting, the user can observe the waveform by the scope as shown in Figure 5.

Figure 5. UFT3GT Input and Output Waveform Plots



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