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April 1st, 2010
Renesas Electronics Corporation

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7548/7549 Group

Serial I/O (Asynchronous Serial I/O (UART) Mode)

1. Abstract

The following article introduces and shows an example of how to use the Serial I/O (Clock Asynchronous Serial I/O (UART) Mode) on the 7548/7549 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):
Applicable MCU: 7548/7549 Group
Oscillation frequency: 4.9152 MHz

Function set ROM data 0 to 2 are areas used to set peripheral functions by data written to the QzROM and can not be set by program. Data set to these areas are valid after a reset of the MCU is released. Make sure to set values according to the user system regardless of the use of peripheral functions. Set values used in this sample program are as follows.

Function set ROM data 0 FSROM0 (address FFD8h): 10000000b
Function set ROM data 1 FSROM1 (address FFD9h): 10000001b
Function set ROM data 2 FSROM2 (address FFDAh): 00001011b

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Communication Using Asynchronous Serial I/O (UART) (Transmit/Receive)

Outline: 2-byte data is transmitted and received using UART.
The port P01 is used for communication control.

Specifications:

- Serial I/O (UART mode) is used.
- Transfer bit rate: 9600 bps (f(XIN) = 4.9152 MHz divided by 512)
- Communication is controlled by the port P01 (output level of P01 is controlled by program).
- 2-byte data is transferred from the transmit side to the receive side at 10 ms intervals (generated by a timer).

Figure 3.1 shows the Connection Diagram, Figure 3.2 shows the Timing Chart.

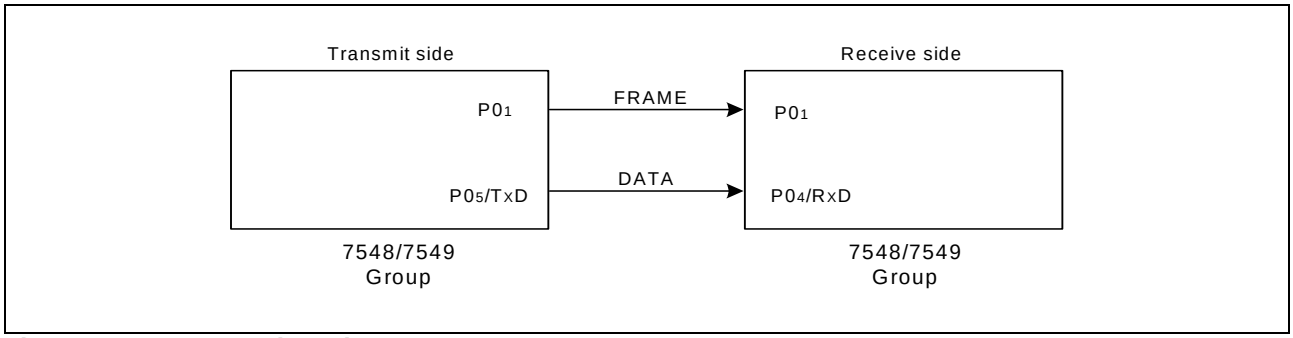


Figure 3.1 Connection Diagram

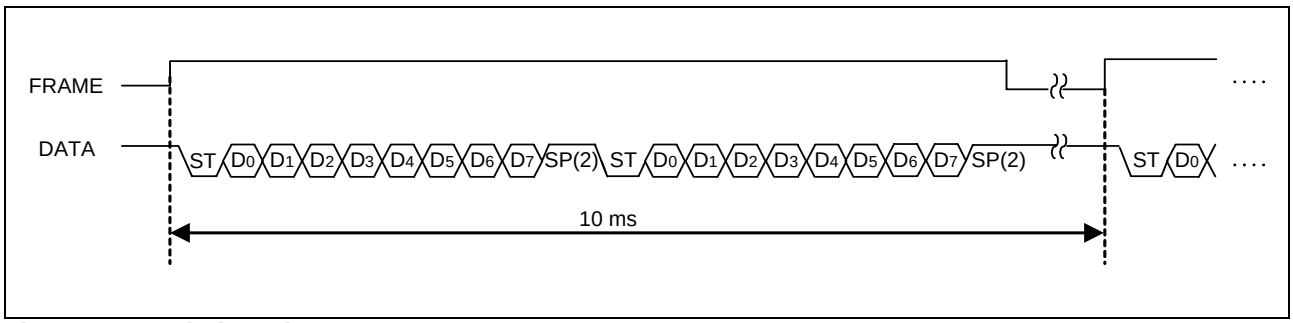


Figure 3.2 Timing Chart

Table 3.1 lists an Example of Baud Rate Generator (BRG) Set Value and Transfer Bit Rate Selection, Figure 3.3 shows the Register Settings Relevant to the Transmit Side, Figure 3.4 shows the Register Settings of Receive Side, Figure 3.5 shows the Control Procedure of Transmit Side, and Figure 3.6 shows the Control Procedure of Receive Side.

Table 3.1 Example of Baud Rate Generator (BRG) Set Value and Transfer Bit Rate Selection

BRG Count Source (Note 1)	BRG Set Value	Transfer Bit Rate (bps) (Note 2)	
		f(XIN) = 4.9152MHz	f(XIN) = 8MHz
f(XIN)/4	255(FFh)	300	488.28125
f(XIN)/4	127(7Fh)	600	976.5625
f(XIN)/4	63(3Fh)	1200	1953.125
f(XIN)/4	31(1Fh)	2400	3906.25
f(XIN)/4	15(0Fh)	4800	7812.5
f(XIN)/4	7(07h)	9600	15625
f(XIN)/4	3(03h)	19200	31250
f(XIN)/4	1(01h)	38400	62500
f(XIN)	3(03h)	76800	125000
f(XIN)	1(01h)	153600	250000
f(XIN)	0(00h)	307200	500000

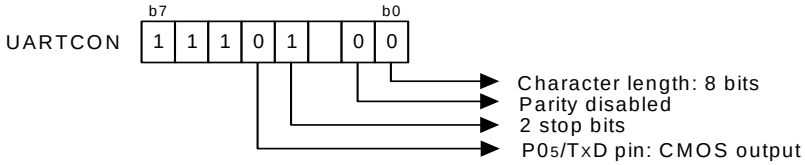
Notes:
1. The BRG count source is selected at the BRG count source selection bit (bit 0 in the serial I/O control register (address: 001Ah)).
2. Calculating formula of the transfer bit rate

$$\text{Transfer bit rate (bps)} = \frac{f(X_{IN})}{(\text{BRG set value} + 1) \times 16 \times m}$$

m: When BRG count source selection bit 0 = 0, m = 1
When BRG count source selection bit 0 = 1, m = 4

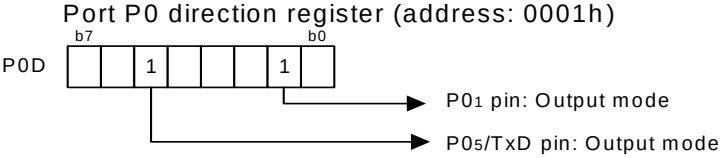
Transmit Side

UART control register (address: 001Bh)

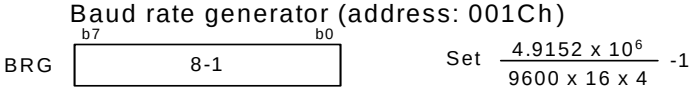


Port P0 register (address: 0000h)

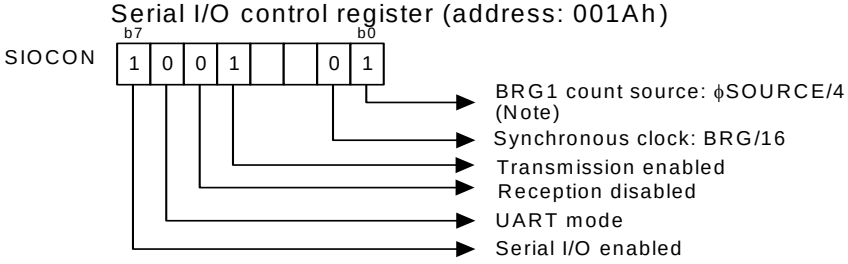
Port P0 direction register (address: 0001h)



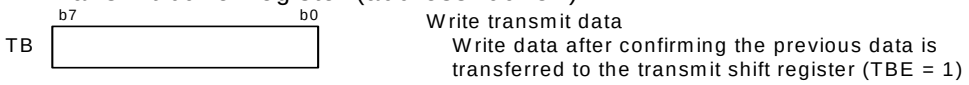
Baud rate generator (address: 001Ch)



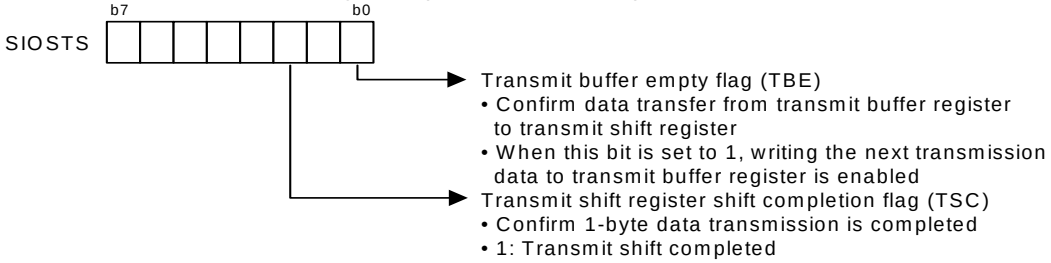
Serial I/O control register (address: 001Ah)



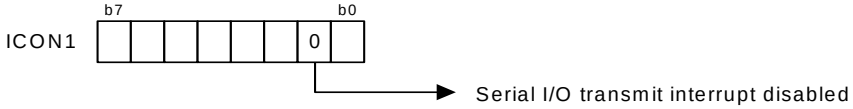
Transmit buffer register (address: 0018h)



Serial I/O status register (address: 0019h)



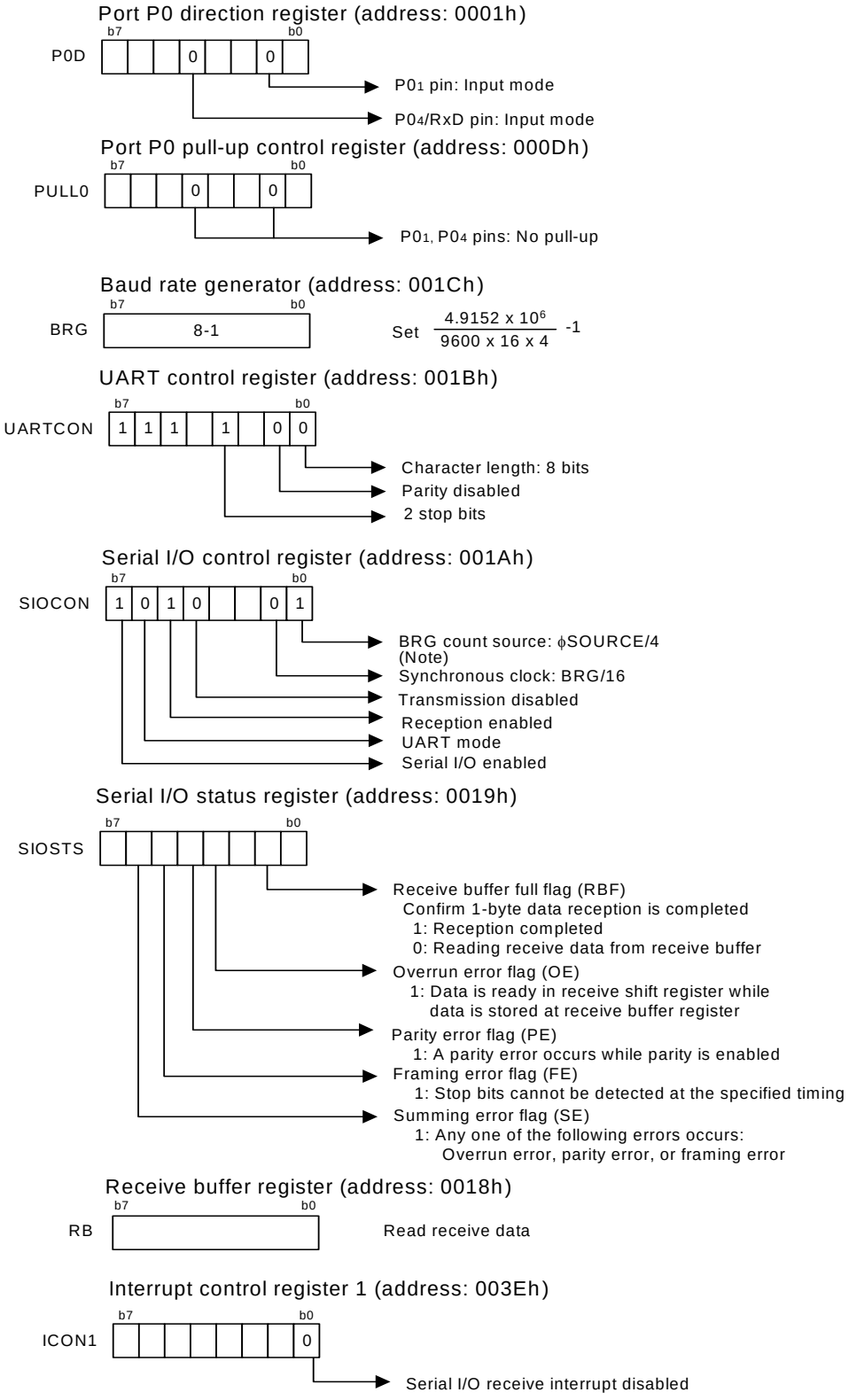
Interrupt control register 1 (address: 003Eh)



Note: ϕSOURCE is the clock selected by bits 5 and 4 at the clock mode register (address 0037h).
Timer count sources are not affected by bits 7 and 6 (clock dividing ratio selection bits).

Figure 3.3 Register Settings Relevant to the Transmit Side

Receive Side



Note: ϕSOURCE is the clock selected by bits 5 and 4 at the clock mode register (address 0037h). Timer count sources are not affected by bits 7 and 6 (clock dividing ratio selection bits).

Figure 3.4 Register Settings of Receive Side

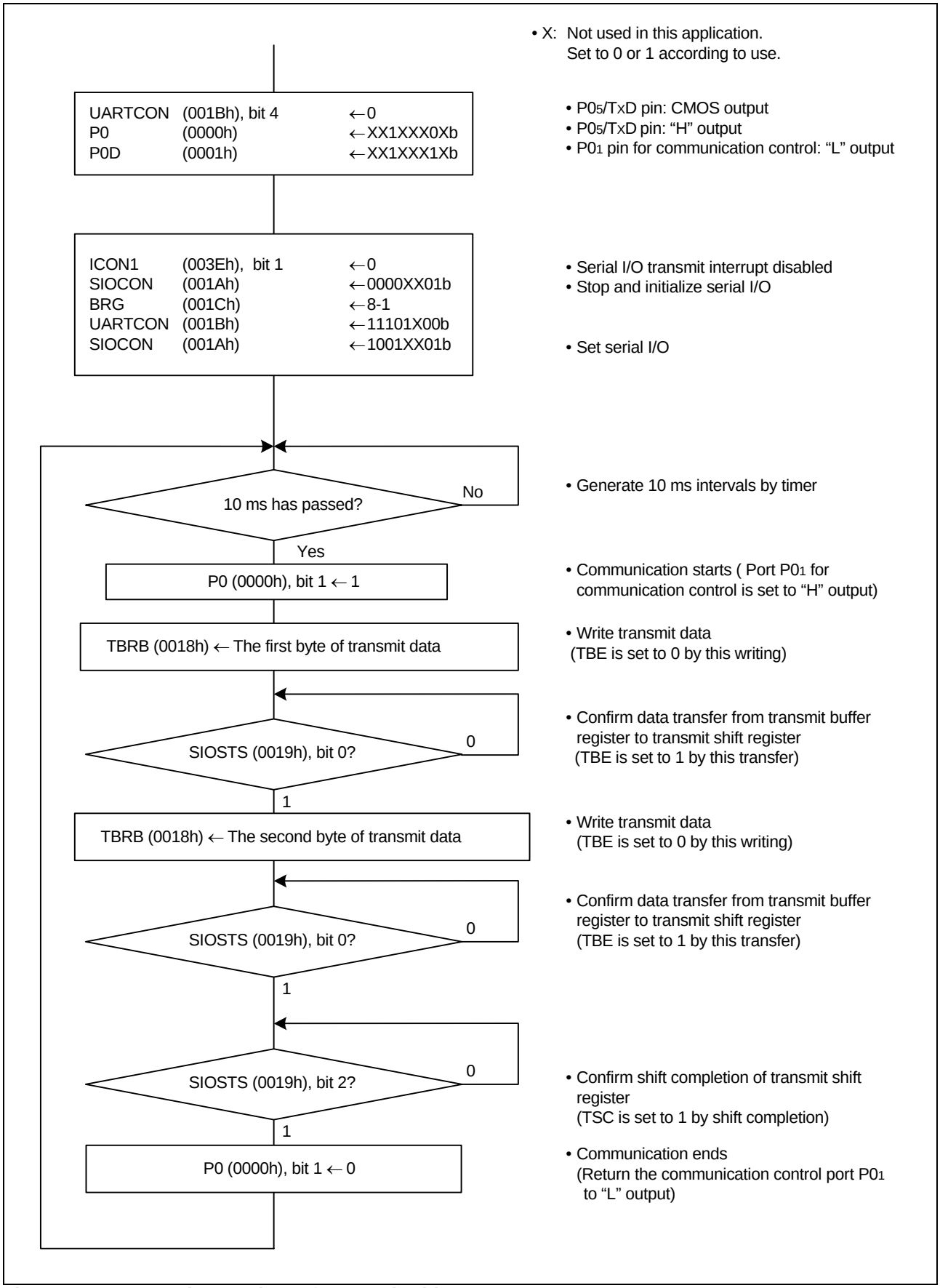


Figure 3.5 Control Procedure of Transmit Side

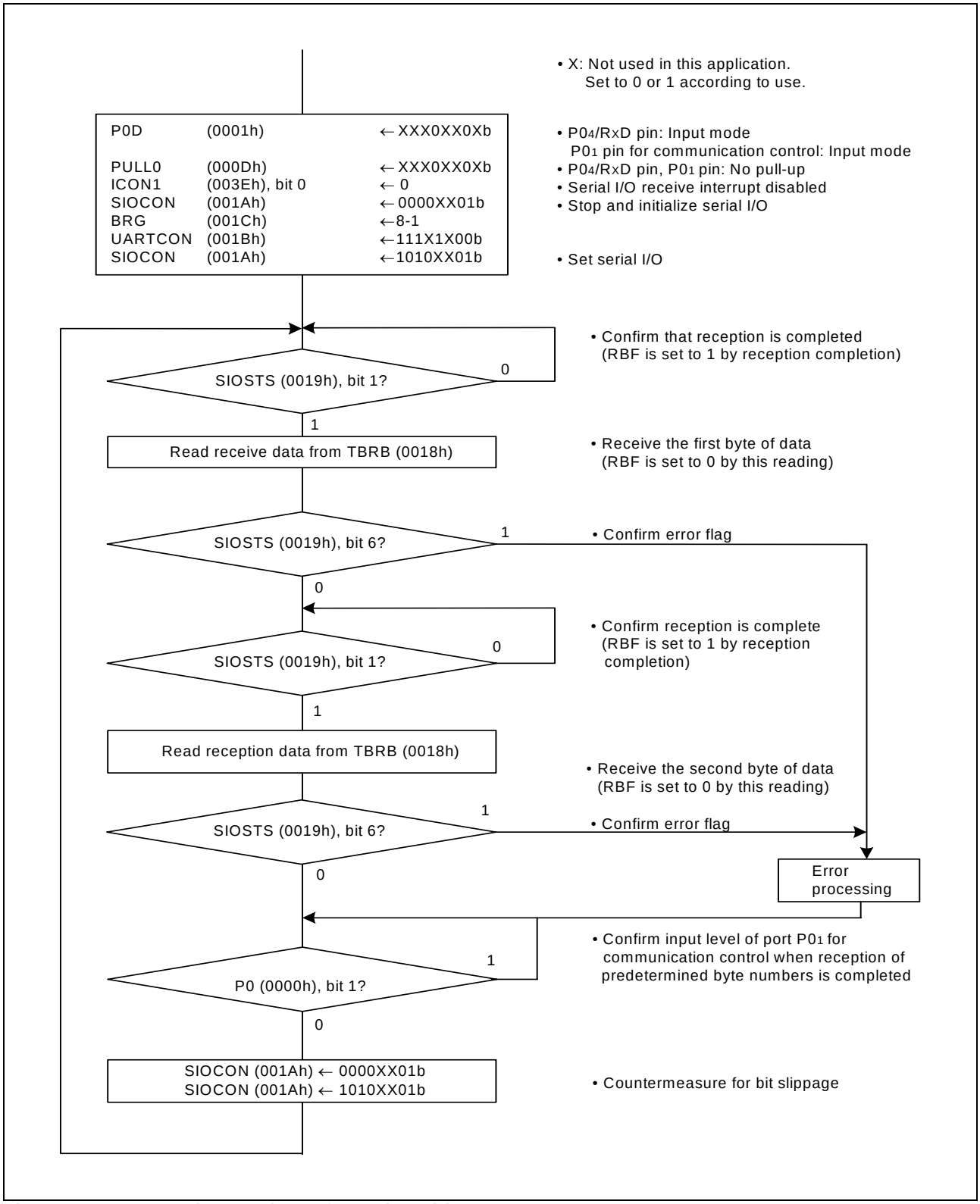


Figure 3.6 Control Procedure of Receive Side

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click “Application Notes” in the left side menu on the page of the 7548/7549 Group.

5. Reference Document

Datasheet
7548/7549 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
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