Renesas RA Family

24-Bit Sigma-Delta A/D Converter Performance for RA2A1

Introduction

This application note describes the performance and calibration functions of the 24-bit sigma-delta A/D converter integrated into RA2A1.

Target Device

RA2A1 MCU Group

Conditions

Unless otherwise specified, typical data are based on VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, Ta = 25 °C

Contents

1. Overview

A 24-bit sigma-delta A/D converter with a programmable gain instrumentation amplifier is built into the RA2A1 MCU Group. The input mode can be selected as differential input mode or single-ended input mode for each channel. Signals from the input multiplexers pass through the programmable gain instrumentation amplifier (PGA) and enter the sigma-delta A/D converter. The A/D conversion results are filtered through the SINC3 digital filter and stored in an output register.

The 24-bit Sigma-Delta A/D Converter has a calibration function. Calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use. Calibration must be performed when using the differential input mode of the 24-bit sigma-delta A/D converter for the first time after reset.

This application note explains the 24-bit sigma-delta A/D converter analog input and timing parameters, SNR and SINAD characteristics, AD conversion current consumption, and how to perform calibration.

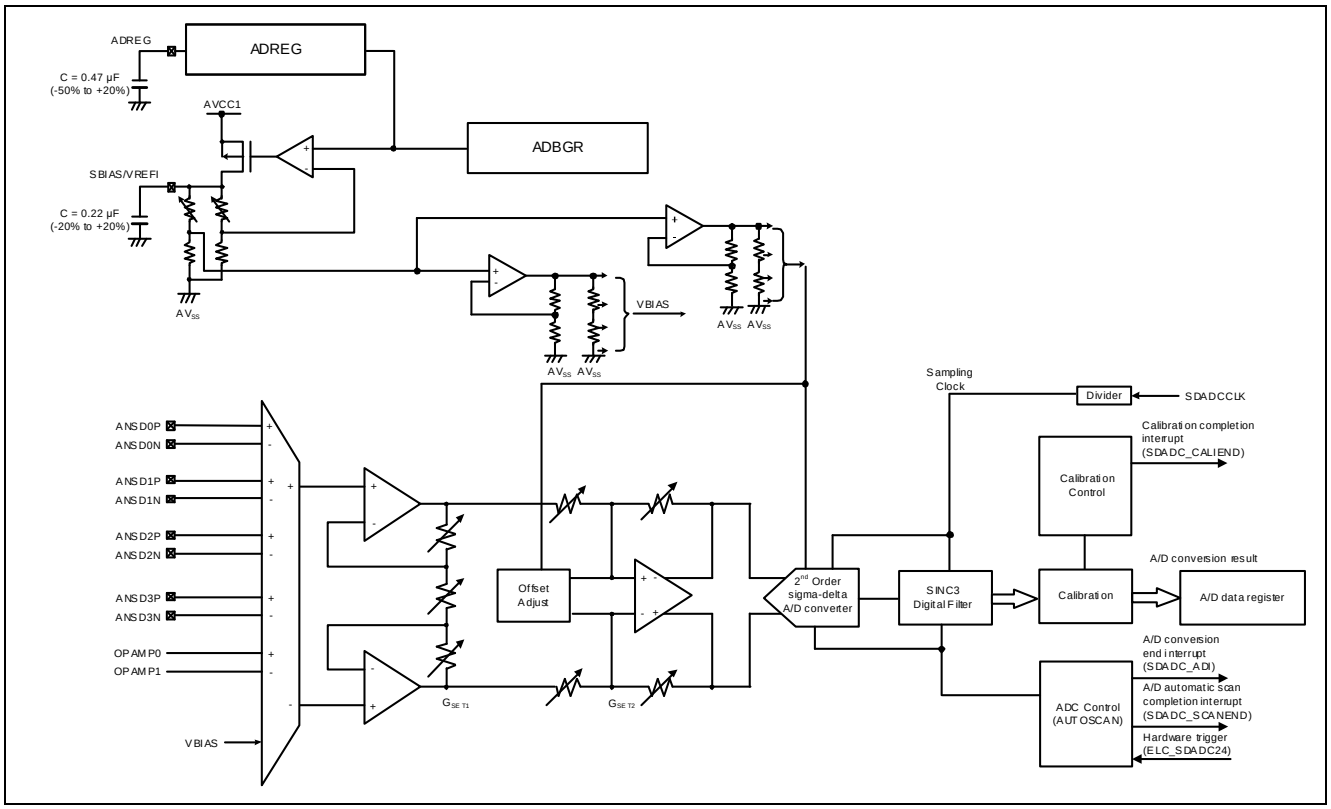

Figure 1. SDADC24 Block Diagram

Table 1. SDADC24 I/O Pins

Pin name	I/O	Function
AVCC1	Input	Analog block power supply pin
AVSS1	Input	Analog block power supply ground pin
ADREG	I/O	Power supply pins for PGA and the sigma-delta A/D converter
SBIAS/VREFI	Input	External reference voltage input pin (VREFI)
	Output	Sensor Power supply pin (SBIAS)
ANSD0P to ANSD3P, ANSD0N to ANSD3N	Input	Analog input pins

2. Utilizing Data Sheet Parametric Values

This chapter describes the electrical characteristics of the 24-Bit Sigma-Delta A/D Converter.

2.1 Analog Inputs Parameters

This section describes analog inputs. Sections 2.1.1 and 2.1.2 show the ranges of input voltage in differential input mode and single-ended input mode.

2.1.1 Range of Input Voltage in Differential Input Mode

Table 2 shows analog input characteristics in differential input mode.

Table 2. Analog Input Characteristics in Differential Input Mode

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Full-scale range		F_{SR}	-	± 0.8 /G_{TOTAL}	-	V	-
Analog input in differential input mode	Differential input voltage range	V_{ID}	-0.8/G_{TOTAL}	-	0.8/G_{TOTAL}	V	V_{ID} = ANSDnP - ANSDnN, or AMP0O - AMP1O (n = 0 to 3), d_{OFR} = 0 mV
	Input voltage range	V_I	0.2	-	1.8	V	V_I = ANSDnP, ANSDnN, AMP0O, or AMP1O (n = 0 to 3)
	Common mode Input voltage range	V_{COM}	0.2+(|V_{ID}|× G_{SET1})/2	1.0	1.8-(|V_{ID}|×G_{SET1})/2	V	d_{OFR} = 0 mV
Input absolute current		I_{IN}	-	2	-	nA	V_I = 1 V
Input offset current		I_{INOFR}	-	1	-	nA	V_{ID} = 0 V, V_{COM} = 1 V
Input impedance		Z_{IN}	-	500	-	Mohm	V_{ID} = 1 V, V_{COM} = 1 V

In differential input mode, the multiplication factor of gain (G_{TOTAL}) can be changed from ×1 to ×32 by a combination of the gain of the previous-stage amplifier (G_{SET1}) and the gain of the next-stage amplifier (G_{SET2}).

In the expressions that follow, V_{SIG} is the differential voltage amplitude, V_{COM} is the in-phase input voltage, and d_{OFR} is the value calculated by converting the output voltage of the D/A converter for offset voltage adjustment into input voltage. The range of input voltage for one amplifier stage is from 0.2 V to 1.8 V. Therefore, signals that pass through the previous-stage amplifier of the instrumentation amplifier and enter to the next-stage amplifier must satisfy the condition indicated by Expression 1.

In addition, signals that pass through the previous-stage amplifier of the instrumentation amplifier and exit from the next stage amplifier must satisfy the condition indicated by Expression 2.

Expression 1:

$$0.2\,\mathrm{V} + \frac{|V_{SIG}| \times G_{SET1}}{2} \leq V_{COM} \leq 1.8\,\mathrm{V} - \frac{|V_{SIG}| \times G_{SET1}}{2}$$

Expression 2:

$$-0.8\ \mathrm{V} \leq (V_{SIG} + d_{OFR}) \times G_{TOTAL} \leq 0.8\ \mathrm{V}$$

When d_{OFR} = 0 mV, the input signal can be equal to the full-scale differential input voltage at full scale. When $V_{SIG} = V_{ID}$ (full-scale differential input voltage), V_{COM} can be represented using Expression 3.

Expression 3:

$$0.2\ \mathrm{V} + \frac{|V_{ID}| \times G_{SET1}}{2} \leq V_{COM} \leq 1.8\ \mathrm{V} - \frac{|V_{ID}| \times G_{SET1}}{2}$$

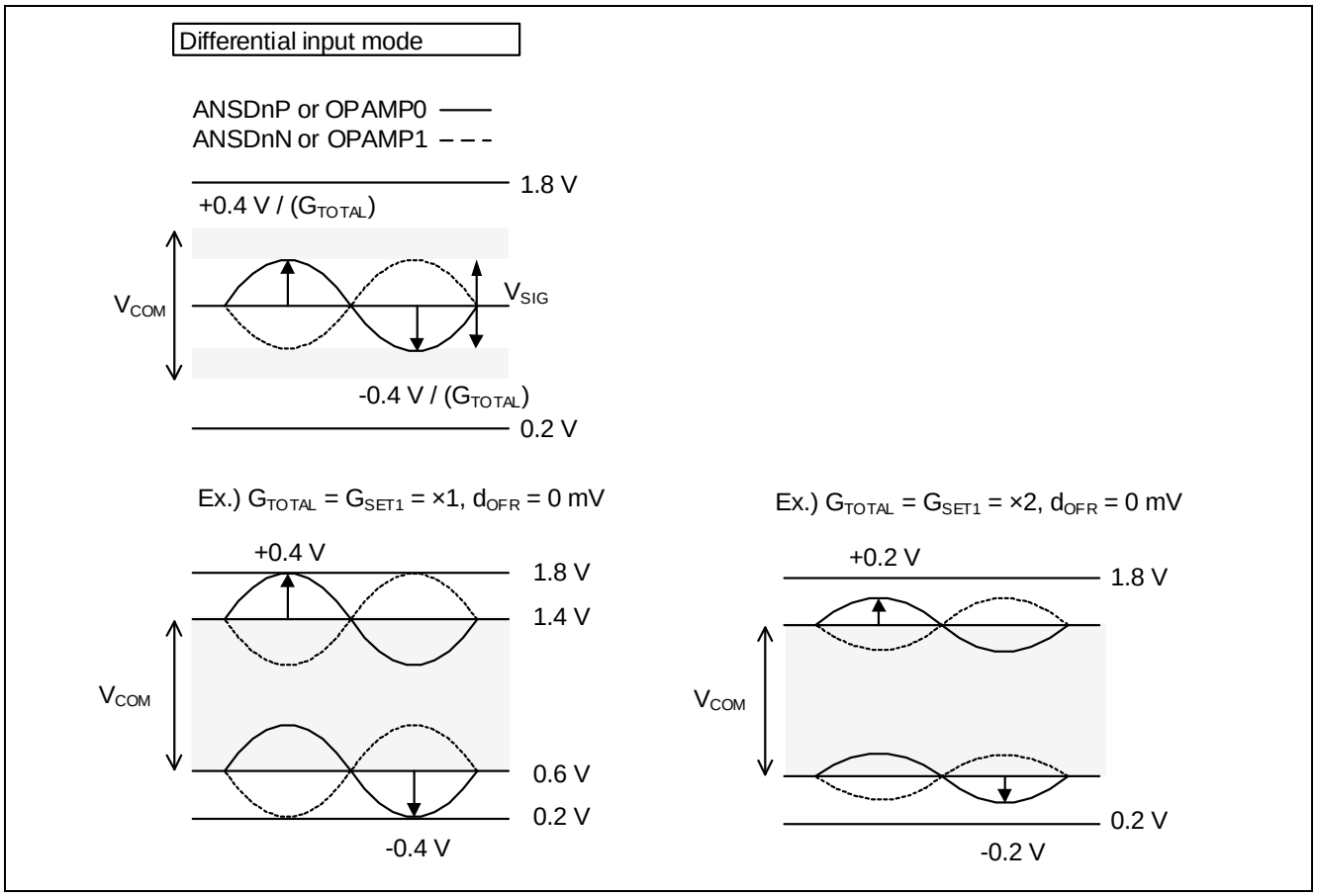

Figure 2. Range of Input Voltage in Differential Input Mode

Figure 3 shows the transition of the amplitude of differential input voltage for each channel of the programmable gain instrumentation amplifier (PGA).

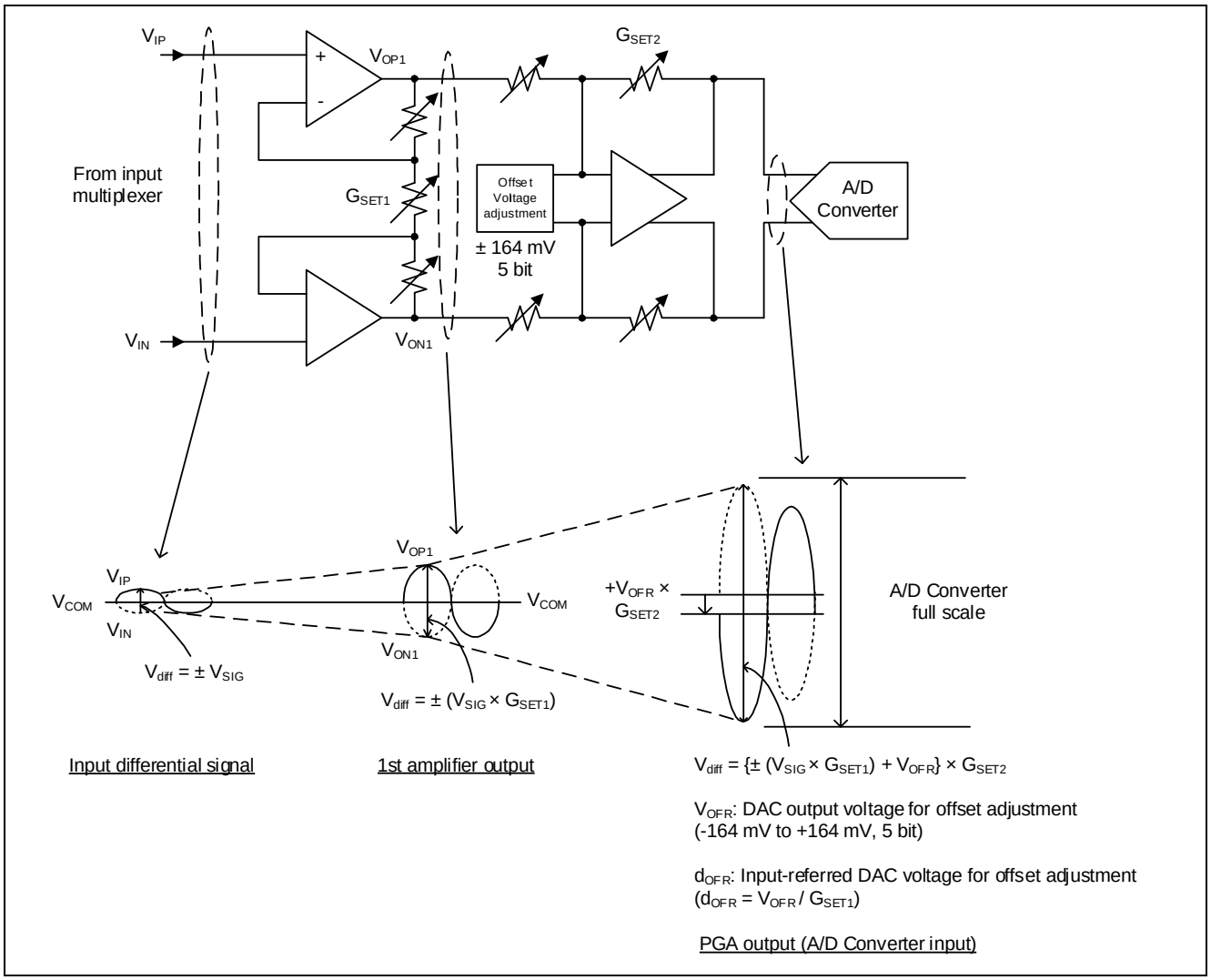

Figure 3. Transition of Differential Input Voltage for Each Channel of the PGA

2.1.2 Range of Input Voltage in Single-ended Input Mode

Table 3 shows the analog input characteristics in single-ended input mode.

Table 3. Analog Input Characteristics in Single-ended Input Mode

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog Input in single-ended input mode	Input voltage range	V_I	0.2	-	1.8	V	V_I = ANSDnP, ANSDnN, AMP0O, or AMP1O (n = 0 to 3), V_{COM} = 1.0 V, d_{OFR} = 0 mV, G_{SET1} = 1, G_{SET2} = 1, OSR = 256
Input absolute current		I_{IN}	-	2	-	nA	V_I = 1 V

The single-ended input mode supports only d_{OFR} = 0 mV, G_{SET1} = 1, G_{SET2} = 1, and Oversampling Ratio (OSR) = 256.

In positive-side single-ended input mode, the signal from the input multiplexer is connected to the non-inverting input of the PGA. The bias voltage (V_{BIAS} = 1.0 V (typical)) is connected to the inverting input of the PGA to provide a reference voltage. In negative-side single-ended input mode, the signal from the input multiplexer is connected to the inverting input of the PGA, and the internal bias voltage is connected to the non-inverting input of the PGA. The differential signal output is in the range from 0.2 V to 1.8 V.

Range of the input voltage (V_I) must satisfy the following expression:

$0.2\ V \leq V_I \leq 1.8\ V$

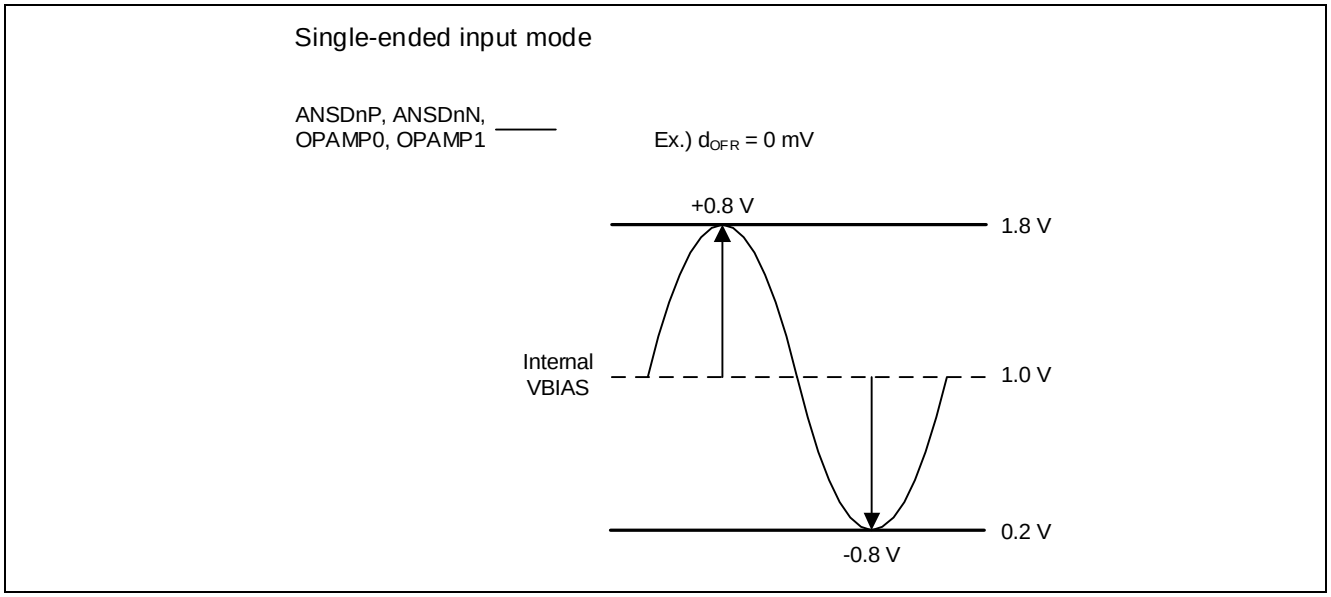

Figure 4. Range of Input Voltage in Single-ended Input Mode

2.2 Timing Parameters

Table 4 shows the timing parameters of the 24-Bit Sigma-Delta A/D Converter.

Table 4. Timing Parameters of 24-Bit Sigma-Delta A/D Converter

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Over sampling frequency	F_{OS}	-	1	-	MHz	Normal A/D conversion mode
		-	0.125	-		Low-power A/D conversion mode
Output data rate	f_{DATA1}	0.48828	-	15.625	ksps	Normal A/D conversion mode
	f_{DATA2}	61.03615	-	1953.125	sps	Low-power A/D conversion mode

A/D conversion is performed by the SDADC24 reference clock generated by the SDADCCLK. Set the SDADC24.STC1.CLKDIV[3:0] bits so that the SDADC24 reference clock is output at 4 MHz. In normal A/D conversion mode, the oversampling frequency is 1 MHz. In low-power A/D conversion mode, the oversampling frequency is 0.125 MHz.

The oversampling ratio can be selected from 64, 128, 256, 512, 1024, or 2048 by SDADC24.PGACn.PGAOSR[2:0] bits (n = 0 to 4).

The equation for calculating the output data rate is as follows:
Output data rate (sps) = Over sampling frequency / Oversampling ratio

Down sampling of the A/D conversion result is performed by the SINC3 digital filter.

Figure 5 shows a block diagram of the digital filter. Three accumulators and three differentiators are connected in a cascade format. For the A/D converter to become stable, the required settling time must be satisfied. Table 5 shows settling time 1 and settling time 2, which are defined as follows:

- Settling time 1 — The time from ADC2.SDADST bit rising to A/D conversion end interrupt. See settling time 1 in Figure 6.
- Settling time 2 — The time from the last A/D conversion end interrupt before channel switching to the first A/D conversion end interrupt after channel switching. See settling time 2 in Figure 6.

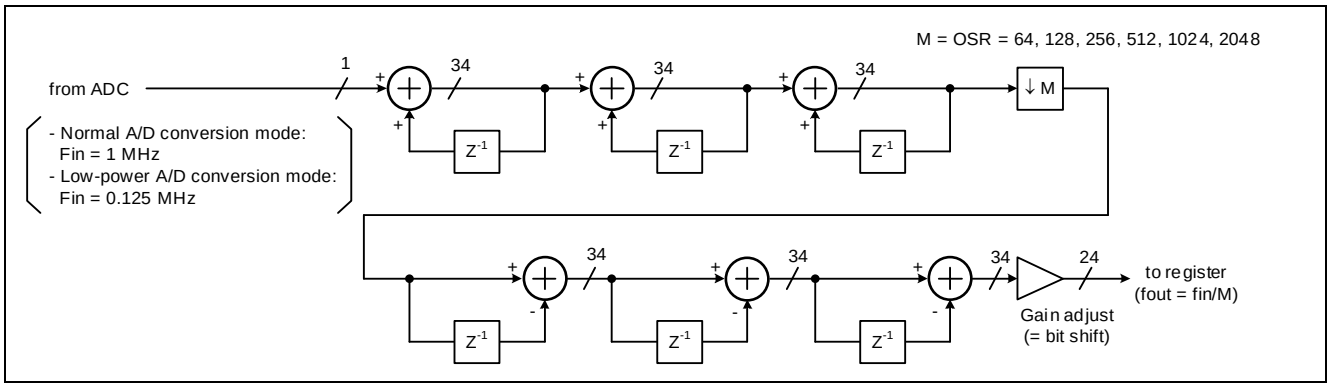

Figure 5. Digital Filter Block Diagram

Table 5. Settling Time for Each Operation Mode

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Item		Normal A/D Conversion Mode	Low-power A/D Conversion Mode
Setting time 1	Min	3T + 129 µs + 2PCLKB + 9 ADC reference clock*1	3T + 1032 µs + 2PCLKB + 9 ADC reference clock*1
	Max	3T + 129 µs + 3PCLKB + 10 ADC reference clock*1	3T + 1032 µs + 3PCLKB + 10 ADC reference clock*1
Setting time 2*2	Min	3T + 129 µs - 1PCLKB	3T + 1032 µs - 1PCLKB
	Max	3T + 129 µs + 1PCLKB	3T + 1032 µs + 1PCLKB

Note: The settling time is automatically generated by the AUTOSCAN built-in sequencer.
3T is the time that is 3 times as long as the sampling time (3 × 1 / fout).

Notes: 1. Normal A/D conversion mode: 4 MHz, low-power A/D conversion mode: 500 kHz.
2. Since the A/D converter and the control circuit are asynchronous, a variation of ± 1PCLKB occurs at the interrupt output timing. There is no variation in the A/D conversion interval, and it is executed at equal intervals.

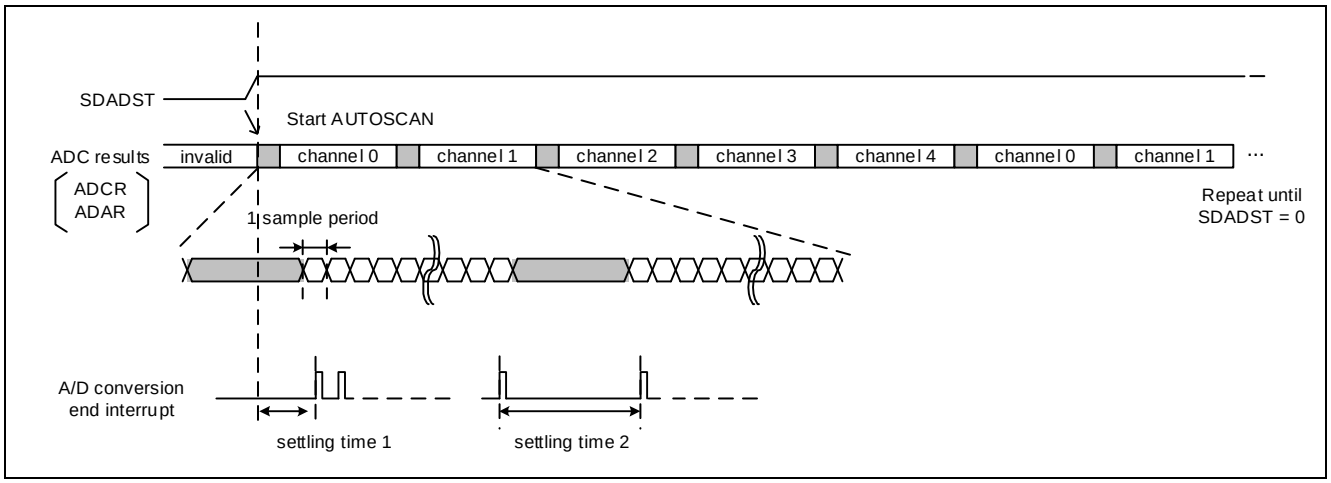

Figure 6. AUTOSCAN Sequence

2.3 24-Bit Sigma-Delta A/D Converter Characteristics

Table 6 shows SNR, SINAD, and ENOB characteristics evaluation results of the 24-Bit Sigma-Delta A/D Converter.

The SNR and SINAD are very important in many applications because they describe the smallest input signal that the converter can resolve. In closed loop systems, detecting small changes in input signals allows better control loop performance.

SNR: Signa-to-noise ratio (dB)
The RMS signal level to the total RMS noise

SINAD: Signal-to-noise and distortion (dB)
The RMS level of input signal/sum RMS value of all noise and distortion excluding DC

ENOB: Effective number of bits
ENOB = (SINAD – 1.76 dB) / 6.02 dB

ENOB (RMS): Effective Resolution
ENOB (RMS) = log2 ($V_{Fullscale}$ / $Noise\_{RMS}$)
$Noise\_{RMS}$ is input-referred noise at V_{ID} = 0 V. $V_{Fullscale}$ is peak-to-peak value of F_{SR}.

Table 6. SNR, SINAD, and ENOB Evaluation Results of 24-Bit Sigma-Delta A/D Converter

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, V_{COM} = 1.0V. The electrical specifications are applied at differential input mode, external clock input used, F_{OS} = 1 MHz, d_{OFR} = 0 mV, unless otherwise specified.

Parameter	Symbol	Typ	Unit	Test Conditions	
Signal to Noise Ratio V_{ID} = 0 V	SNR	76.0	dB	G_{SET1} = 1, G_{SET2} = 1, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		85.1			OSR = 128
		89.1			OSR = 256
		92.2			OSR = 512
		95.2			OSR = 1024
		98.2			OSR = 2048
		73.1	dB	G_{SET1} = 8, G_{SET2} = 4, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		78.2			OSR = 128
		81.3			OSR = 256
		84.2			OSR = 512
		87.2			OSR = 1024
		89.8			OSR = 2048
Signal to Noise and Distortion Ratio fin = 83 Hz	SINAD	74.4	dB	G_{SET1} = 1, G_{SET2} = 1, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		84.1			OSR = 128
		87.8			OSR = 256
		90.1			OSR = 512
		91.7			OSR = 1024
		93.0			OSR = 2048
		72.2	dB	G_{SET1} = 8, G_{SET2} = 4, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		77.9			OSR = 128
		81.0			OSR = 256
		83.7			OSR = 512
		86.1			OSR = 1024
		87.7			OSR = 2048

Parameter	Symbol	Typ	Unit	Test Conditions	
Effective number of bits fin = 83 Hz	ENOB	12.1	bit	G_{SET1} = 1, G_{SET2} = 1, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		13.7			OSR = 128
		14.3			OSR = 256
		14.7			OSR = 512
		14.9			OSR = 1024
		15.2			OSR = 2048
		11.7	bit	G_{SET1} = 8, G_{SET2} = 4, PGACn.PGAAVE[1:0] = 00b or 01b	OSR = 64
		12.6			OSR = 128
		13.2			OSR = 256
		13.6			OSR = 512
		14.0			OSR = 1024
		14.3			OSR = 2048
Effective Resolution	ENOB (RMS)	14.1	bit	G_{SET1} = 1, G_{SET2} = 1, PGACn.PGAAVE[1:0] = 00b or 01b, $V_{fullscale}$ = 1.6 V	OSR = 64
		15.6			OSR = 128
		16.3			OSR = 256
		16.8			OSR = 512
		17.3			OSR = 1024
		17.8			OSR = 2048
		13.6	bit	G_{SET1} = 8, G_{SET2} = 4, PGACn.PGAAVE[1:0] = 00b or 01b, $V_{fullscale}$ = 0.05 V	OSR = 64
		14.5			OSR = 128
		15.0			OSR = 256
		15.5			OSR = 512
		16.0			OSR = 1024
		16.4			OSR = 2048

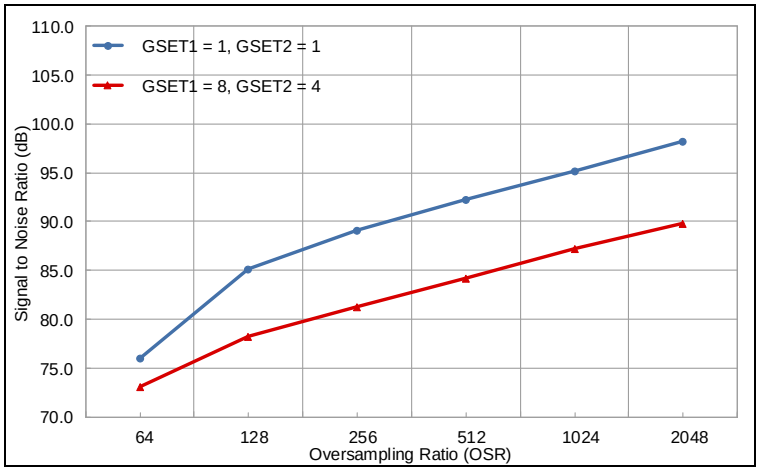

Figure 7. SNR versus OSR

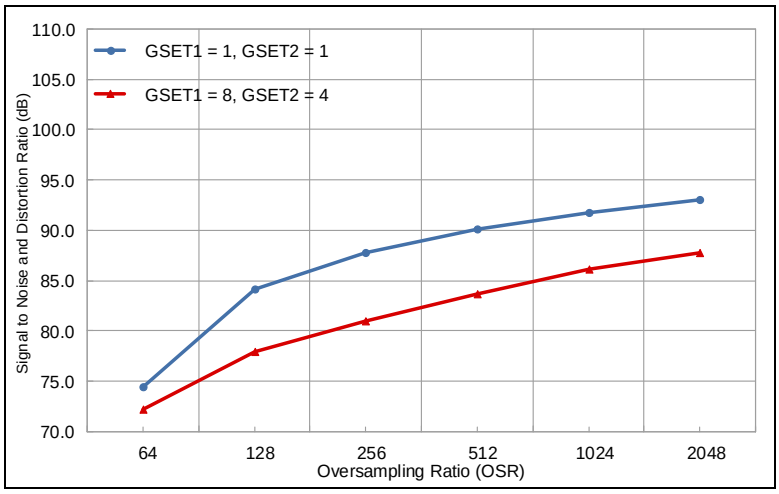

Figure 8. SINAD versus OSR

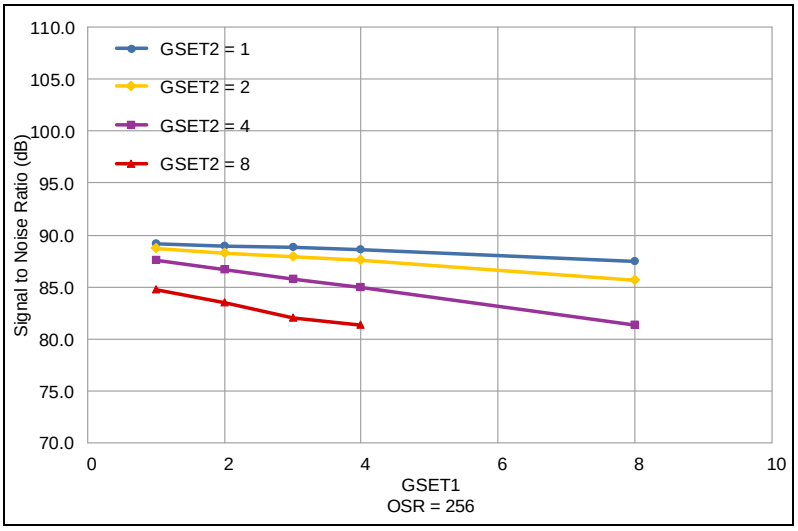

Figure 9. Dependence of SNR on G_{SET1}

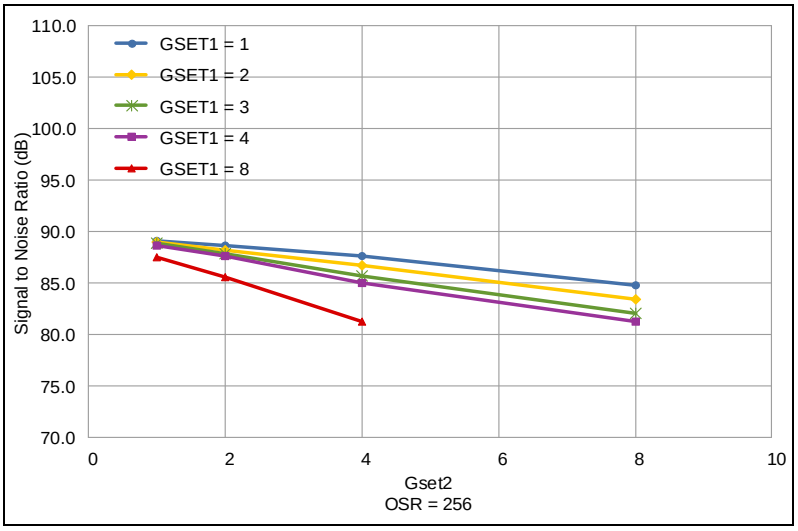

Figure 10. Dependence of SNR on G_{SET2}

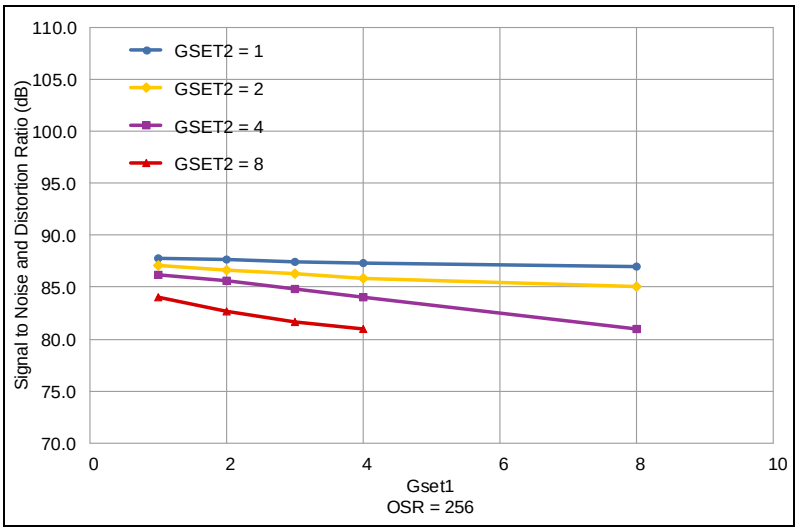

Figure 11. Dependence of SINAD on G_{SET1}

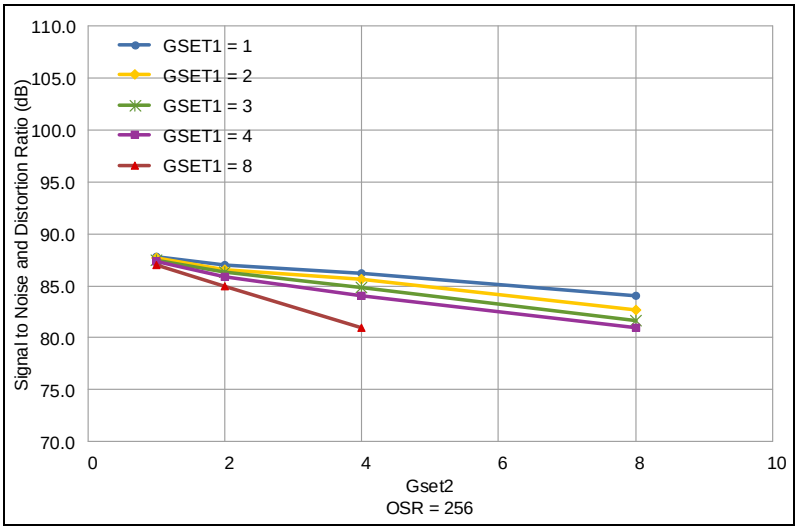

Figure 12. Dependence of SINAD on G_{SET2}

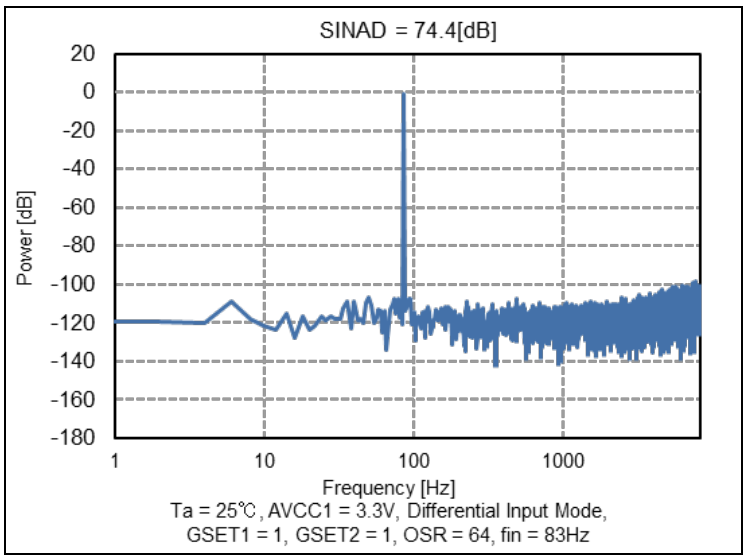

Figure 13. Power versus Frequency (G_{SET1} = 1, G_{SET2} = 1, OSR = 64)

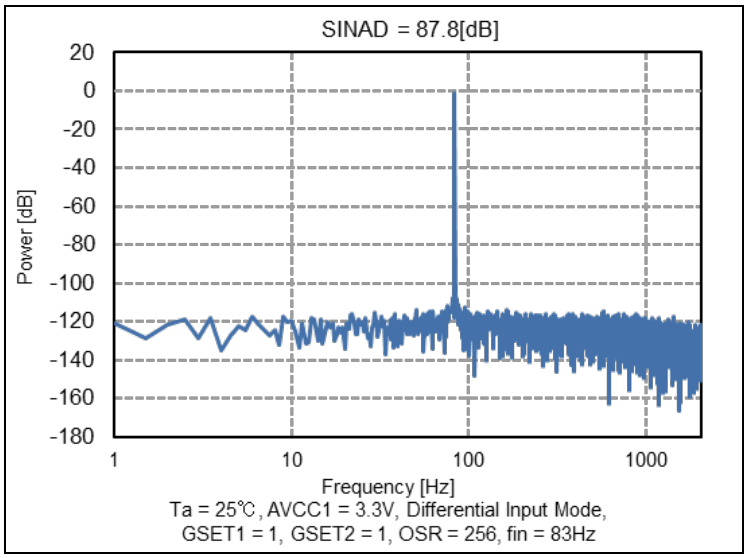

Figure 14. Power versus Frequency (G_{SET1} = 1, G_{SET2} = 1, OSR = 256)

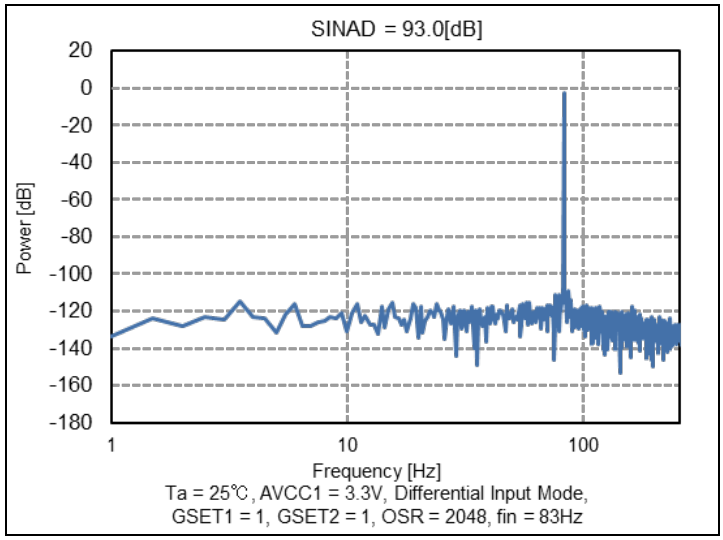

Figure 15. Power versus Frequency (G_{SET1} = 1, G_{SET2} = 1, OSR = 2048)

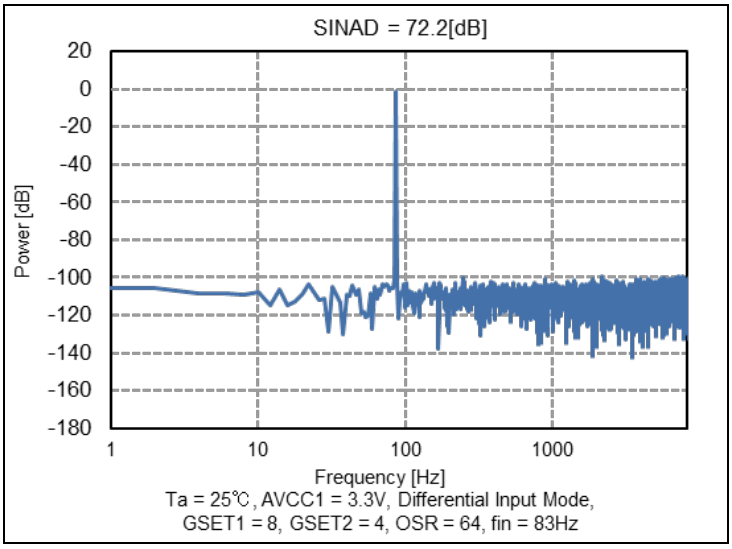

Figure 16. Power versus Frequency (G_{SET1} = 8, G_{SET2} = 4, OSR = 64)

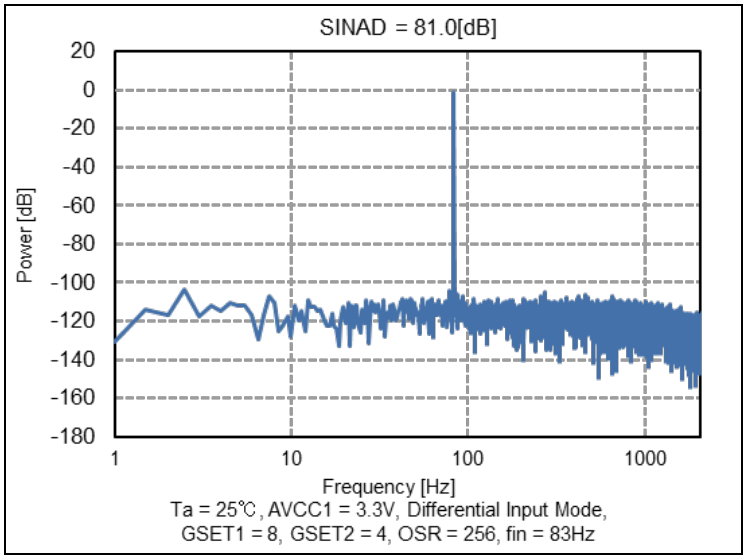

Figure 17. Power versus Frequency (G_{SET1} = 8, G_{SET2} = 4, OSR = 256)

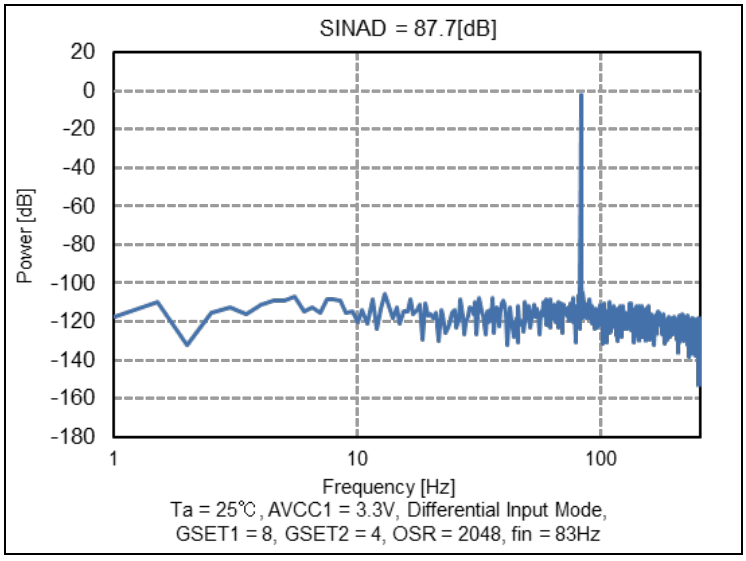

Figure 18. Power versus Frequency (G_{SET1} = 8, G_{SET2} = 4, OSR = 2048)

2.3.1 Improve Accuracy by Averaging A/D Conversion Result

The 24-Bit Sigma-Delta A/D Converter has an averaging function. When averaging is used, multiple conversions are performed and the results are averaged. The output data can be averaged 8, 16, 32, or 64 times. This can suppress the influence of sudden noise and improve the accuracy of the conversion result.

Table 7. Performance Evaluation Result by Averaging A/D Conversion Result

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, V_{COM} = 1.0 V. The electrical specifications are applied at differential input mode, external clock input used, F_{OS} = 1 MHz, d_{OFR} = 0 mV, unless otherwise specified.

Parameter	Symbol	Typ	Unit	Test Conditions	
Signal to Noise Ratio V_{ID} = 0 V	SNR	89.1	dB	G_{SET1} = 1, G_{SET2} = 1, OSR = 256	No averaging
		95.9			8 times average
		98.8			16 times average
		101.5			32 times average
		104.3			64 times average
	SINAD	88.1	dB	G_{SET1} = 1, G_{SET2} = 1, OSR = 256	No averaging
		91.8			8 times average

Parameter	Symbol	Typ	Unit	Test Conditions	
Signal to Noise and Distortion Ratio fin = 10 Hz		92.9			16 times average
		94.1			32 times average
		95.4			64 times average
Effective number of bits fin = 10 Hz	ENOB	14.3	bit	G_{SET1} = 1, G_{SET2} = 1, OSR = 256	No averaging
		15.0			8 times average
		15.1			16 times average
		15.3			32 times average
		15.6			64 times average
Effective Resolution	ENOB (RMS)	16.3	bit	G_{SET1} = 1, G_{SET2} = 1, OSR = 256, $V_{fullscale}$ = 1.6 V	No averaging
		17.4			8 times average
		17.9			16 times average
		18.4			32 times average
		18.8			64 times average

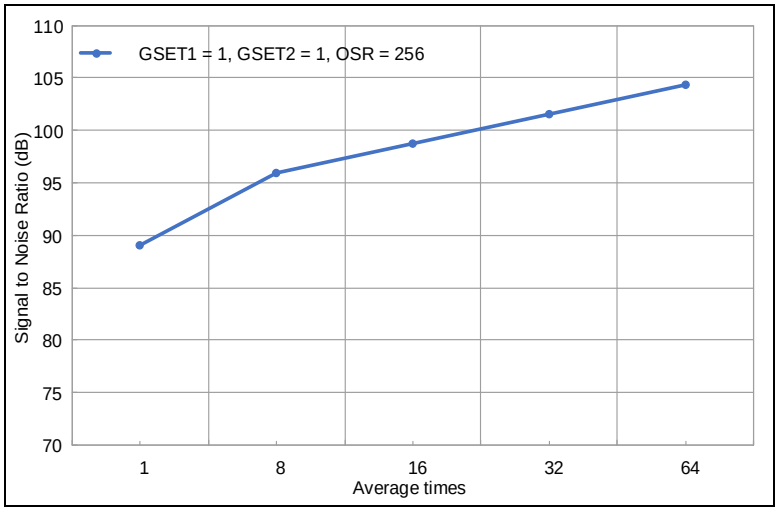

Figure 19. SNR versus Average Times

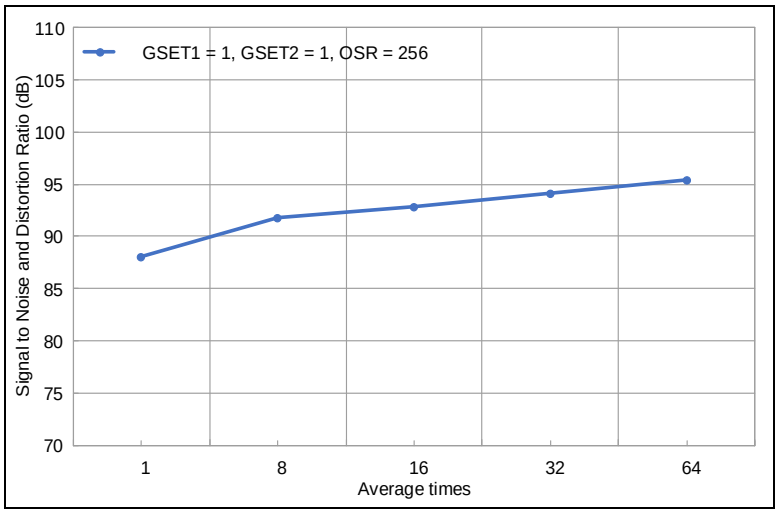

Figure 20. SINAD versus Average Times

2.4 Sensor Bias (SBIAS) Characteristics

Table 8 shows SBIAS drift characteristics evaluation results.
The average value ± 1σ of the evaluation results is defined as the typical and the average value ± 5σ of the evaluation results is defined as the maximum.

Table 8. SBIAS Drift Characteristics Evaluation Result

Conditions: VCC = AVCC0 = AVCC1 = 2.7V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V, Ta = –40 °C to 105°C,
SDADCSTC1.VREFSEL = 0, Connect the SBIAS/VREFI pin to AVSS1 pin by a 0.22 µF (-20% to +20%).

Parameter	Symbol	Typ*1	Max*2	Unit	Test Conditions
SBIAS drift	dE_{SBIAS}	18.7	89.1	ppm/°C	SBIAS = 0.8 V
		16.6	79.0		SBIAS = 1.0 V
		14.8	73.4		SBIAS = 1.2 V
		14.2	69.4		SBIAS = 1.4 V
		13.2	66.6		SBIAS = 1.6 V
		12.6	64.7		SBIAS = 1.8 V
		12.1	63.6		SBIAS = 2.0 V
		11.9	62.7		SBIAS = 2.2 V

Note: SBIAS drift is calculated by (Max (SBIAS error (T (-40°C) to T (125°C))) - Min (SBIAS error (T (-40°C) to T (125°C)))) / (125°C - (-40°C))

Notes: 1. Average ± 1σ
2. Average ± 5σ

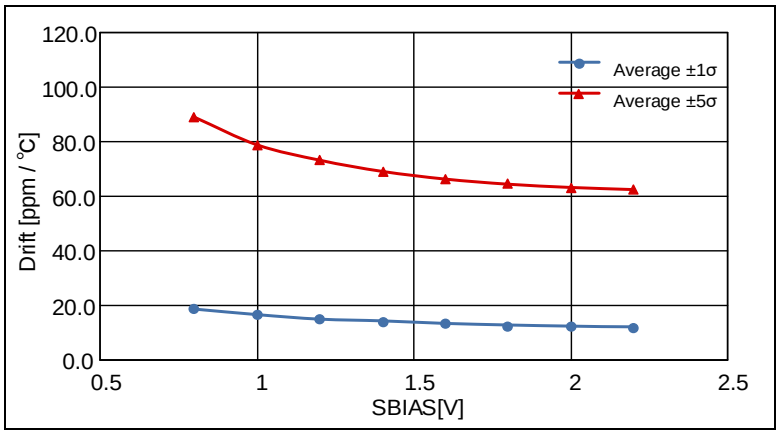

Figure 21. Drift versus SBIAS

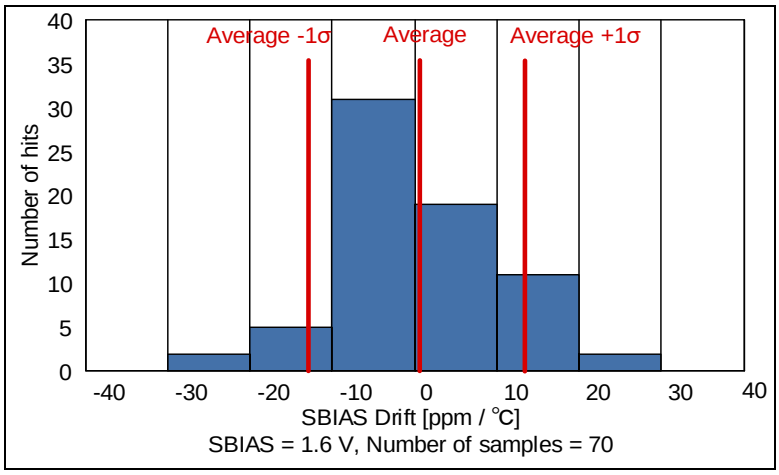

Figure 22. SBIAS Drift Histogram

2.5 Operating and Standby Current

Table 9 to Table 11 show operating current evaluation results of the A/D converter module-stop state, A/D conversion wait state, and A/D conversion state.

Table 9. Operating Current Evaluation Result of A/D Converter in Module-stop State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 1b, SDADCCKCR.SDADCCKEN = 0b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 0b, STC2.ADCPON = 0b, ADC2.SDADST = 0b

Parameter	Symbol	Typ	Unit	Test Conditions
Analog power supply current	I_{AVCC1}	0.1	µA	-

Table 10. Operating Current Evaluation Result in A/D Conversion Wait State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 0b, SDADCCKCR.SDADCCKEN = 1b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 1b, STC2.ADCPON = 1b, ADC2.SDADST = 0b

Parameter	Symbol	Typ	Unit	Test Conditions	
Analog power supply current	I_{AVCC1}	0.90	mA	SDADCSTC1.VREFSEL = 0, SBIAS=2.2V	Normal A/D conversion mode
		0.62			Low power A/D conversion mode

Table 11. Operating Current Evaluation Result in A/D Conversion State

Conditions: VCC = AVCC0 = AVCC1 = 3.3 V, VSS = AVSS0 = AVSS1 = 0 V, HOCO clock oscillation frequency = 64 MHz, PCLKB = 32 MHz, MSTPCRD.MSTPD17 = 0b, SDADCCKCR.SDADCCKEN = 1b, SDADCCKCR.SDADCCKSEL = 1b, STC2.BGRPON = 1b, STC2.ADCPON = 1b, ADC2.SDADST = 1b

Parameter	Symbol	Typ	Max	Unit	Test Conditions	
Analog power supply current	I_{AVCC1}	0.97	1.11	mA	SDADCSTC1.VREFSEL = 0, SBIAS=2.2V	Normal A/D conversion mode
		0.77	0.90			Low power A/D conversion mode
Reference power supply current	I_{REFI}	6.0	7.0	µA	SDADCSTC1.VREFSEL = 1, VREFI = 0.8V	
		18.0	22.0		SDADCSTC1.VREFSEL = 1, VREFI = 2.4V	

3. Calibration Function

Calibration allows high-precision A/D conversion by calculating the offset error correction value and gain error correction value under the conditions of use. The calibration function performs A/D conversion of the internal or user- specified reference voltage, and then determines the most appropriate correction value from the error included in the conversion result. Calibration is started when 1 is written to the CLBSTR.CLBST bit. A/D conversion is performed several times to calculate the correction factor.

The calibration function should be performed in an environment where the analog block power supply, reference power supply, analog inputs, and SDADC24 reference clock are stable. If calibration is performed in an unstable environment, A/D conversion accuracy might deteriorate.

Table 12. Settings and Operations of Calibration

Control register bits			Calculating correction factors for calibration
PGACn.PGASEL	**CLBC.CLBMD[1:0]**	**PGACn.PGACVE**	
0 (Differential input mode)	Don't care	0	Disabled
	00	1	Internal calibration operation
	01	1	External offset calibration operation
	10	1	External gain calibration operation

Note: The correction factors are not calculated for the channels set in single-ended input mode.

Calibration must be performed in the following cases:

- When differential input mode is used for the first time after reset.
- When the VREF mode is switched between external VREF mode and internal VREF mode using the STC1.VREFSEL bit in differential input mode.
- When the voltage is switched between the SBIAS output voltage and VREFI input voltage using the STC1.VSBIAS[3:0] bits in differential input mode.
- When the mode is switched from normal A/D conversion mode to low-power A/D conversion mode, or vice versa in differential input mode.
- When the gain is changed for the same channel in differential input mode.

Notes: 1. Bits for the channel number of an A/D conversion result (ADCR.SDADCRC[2:0]), bit for displaying the status of an A/D conversion result (ADCR.SDADCRS), and bits for the A/D converter conversion result (ADCR.SDADCRD[23:0]) are not updated during internal or external calibration.

2. When performing internal or external calibration, set the Automatic Scan Mode Selection bit of the Sigma-Delta A/D Converter Control Register 1 (ADC1) to 1 for single scan. For details, see section 3.4.3, Self-Diagnosis Flow of PGA Offset and section 3.4.4, Disconnection Detection Assist Flow.
3. The d_{OFR} voltage cannot be set to a value other than 0 mV (PGACn.PGAOFS[4:0] = 00000b (n = 0 to 4)) during calibration operation.
4. For external calibration operation, multiple channel settings cannot be set to PGACn.PGACVE = 1 (n = 0 to 4) at the same time.

3.1 Internal Calibration Operation Mode

In internal calibration operation mode, offset and gain error correction values are calculated by the internal analog input generated based on the internal reference voltage. The correction values for multiple input channels can be calculated by only one calibration operation. After calibration is started by the CLBSTR.CLBST bit, the offset and gain error correction values are calculated for all input channels set as the calibration targets. Calibration is complete after a calibration completion interrupt (SDADC_CALIEND) is generated. For details on the setting, see Figure 30.

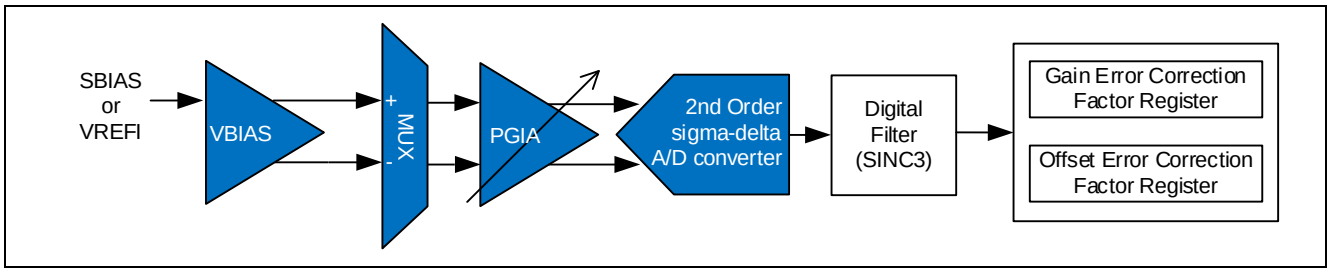

Figure 23. Internal Calibration

3.2 External Calibration Operation Mode

In external calibration operation mode, calibration is performed based on the user-specified reference voltage. The offset calibration calculates the correction value for the A/D conversion result corresponding to the differential analog input at the time of the offset calibration (VIDOCAL) to be corrected to 0. Gain calibration calculates the correction value for the A/D conversion result corresponding to the value (VIDGCAL - VIDOCAL) calculated by subtracting the differential analog input at the time of the offset calibration (VIDOCAL) from the differential analog input at the time of the gain calibration (VIDGCAL) to be corrected to 2^{23} - 1. The correction value for one channel is calculated by one calibration operation. To

calculate the offset and gain error correction values, two calibration operations must be performed. When each calibration completes, a calibration completion interrupt (SDADC_CALIEND) is generated. Set the reference voltage for the input channel before each calibration operation is performed (before setting the CLBSTR.CLBST bit to 1). Table 13 shows the user-specified reference voltage in external calibration operation mode. For details on the setting, see Figure 31.

Table 13. User-specified Reference Voltage in External Calibration Operation Mode

User-specified reference voltage		Min	Typ	Max	Unit
The differential analog input at the time of the external offset calibration (VIDOCAL)	ANSDnP – ANSDnN (n = 0 to 3) or OPAMP0 - OPAMP1	*1	0	*1	V
The differential analog input at the time of the external gain calibration (VIDGCAL)		$0.4/G_{TOTAL}$*1		$0.8/G_{TOTAL}$*1	V
VIDGCAL - VIDOCAL*1		$0.4/G_{TOTAL}$		$0.8/G_{TOTAL}$	V

Note 1. VIDOCAL and VIDGCAL must be used in a range that satisfies the minimum and maximum values of VIDGCAL - VIDOCAL.

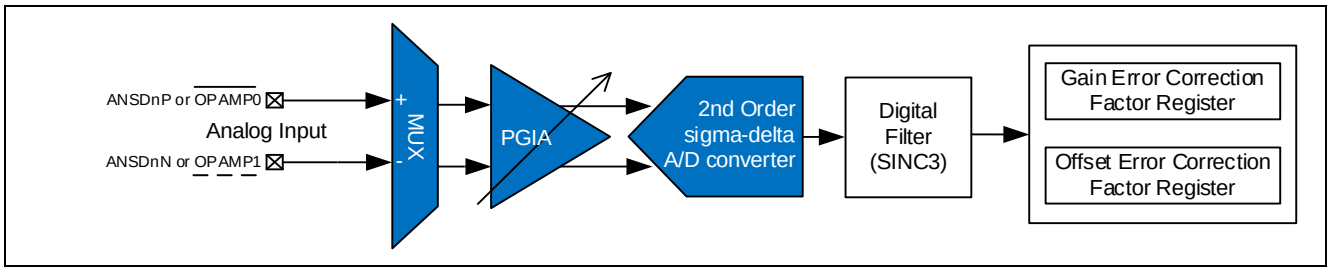

Figure 24. External Calibration

3.3 Recalibration Omitted

When using the differential input mode with the same STC1.SDADLPM, STC1.VSBIAS[3:0], STC1.VREFSEL and PGACn.PGAGC[4:0] bit settings as in the calibration execution, store the values of the GCVLR and OCVLR registers after calibration to the data flash. Recalibration can be omitted by copying the stored value to the GCVLR and OCVLR register from the next time. For details on the settings, see Figure 32.

However, when there is a large temperature change or there is a change in the user environment or use conditions, it is necessary to perform re-calibration.

3.4 Calibration Control Flows

Figure 26 to Figure 32 show the startup flow and calibration flow of the SDADC24.

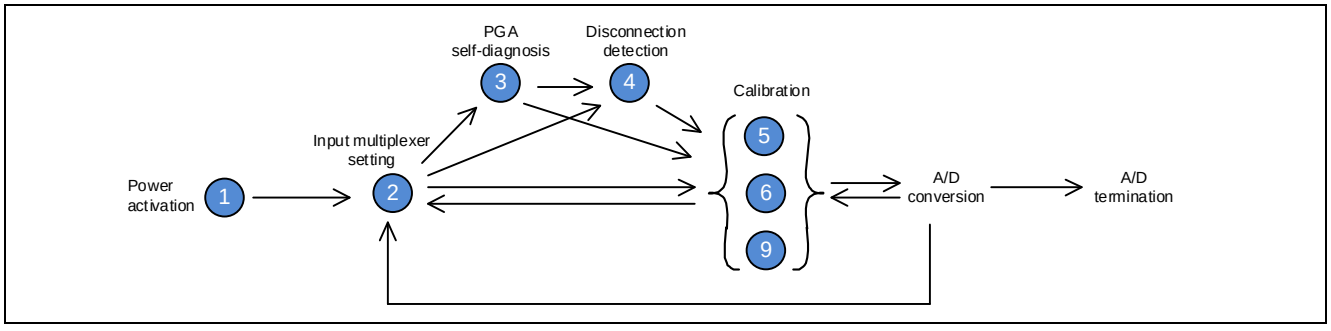

Figure 25. Overview of Flows

3.4.1 Analog Power Supply Activation Flow

Figure 26 shows the flow for analog power supply activation.

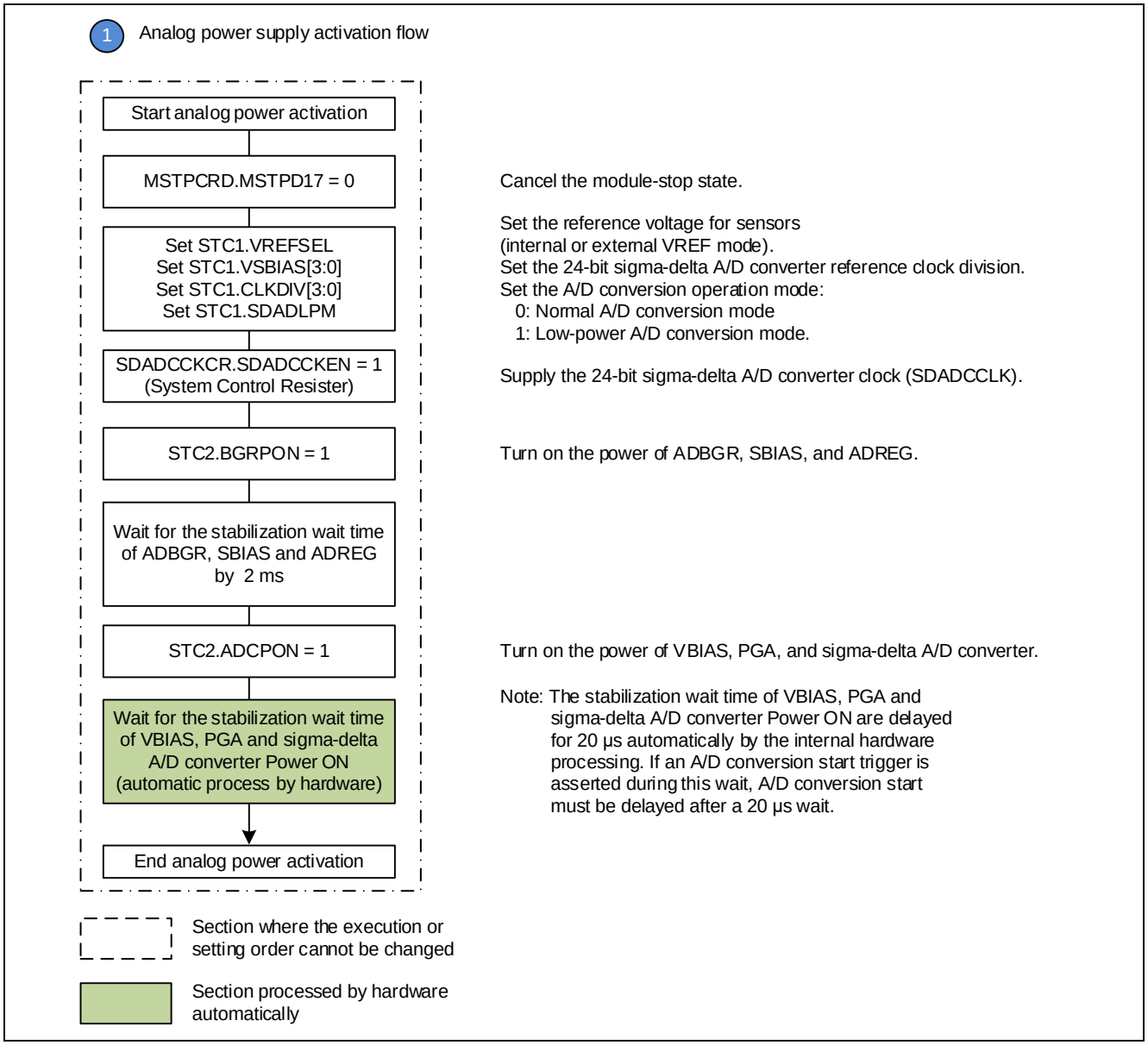

Figure 26. Analog Power Supply Activation Flow

3.4.2 Input Multiplexer Setting Flow

Figure 27 shows the flow for input multiplexer setting.

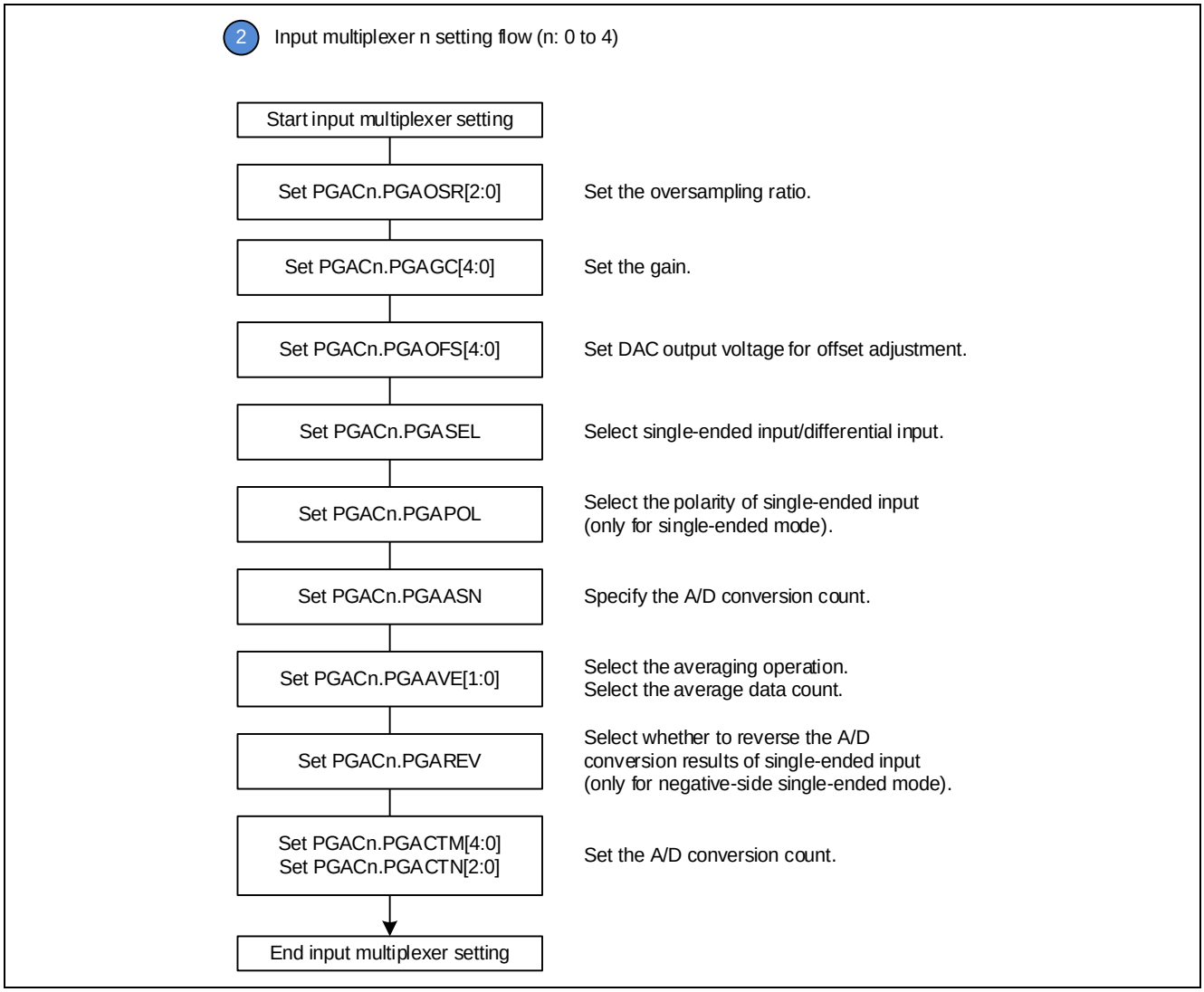

Figure 27. Input Multiplexer Setting Flow

3.4.3 Self-Diagnosis Flow of PGA Offset

Figure 28 shows the flow for self-diagnosis of PGA offset.

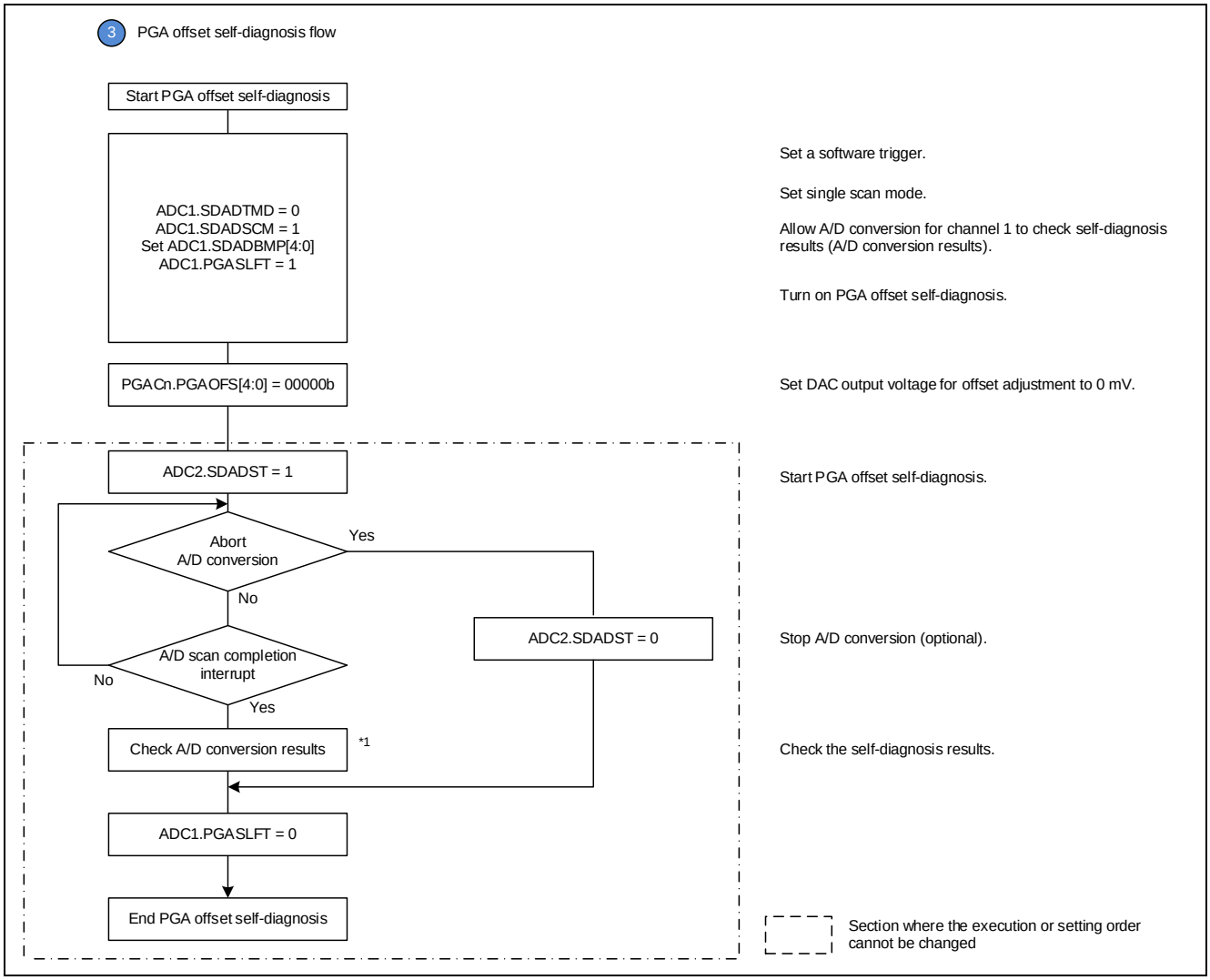

Figure 28. Self-diagnosis Flow for PGA Offset

Note: 1. The results of PGA offset self-diagnosis can be checked from A/D conversion results.

3.4.4 Disconnection Detection Assist Flow

Figure 29 shows the flow for disconnection detection assist.

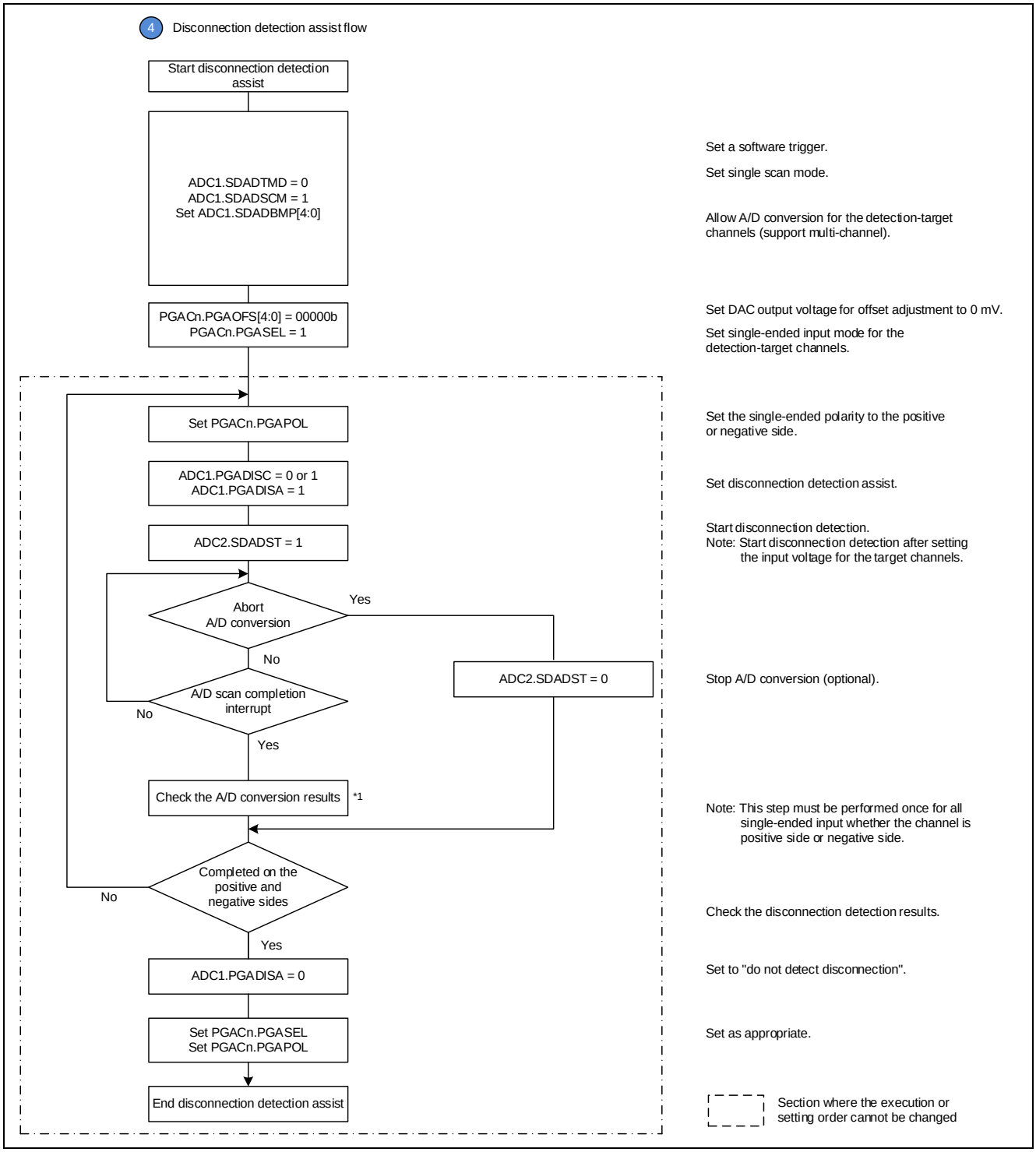

Figure 29. Disconnection Detection Assist Flow

Note 1. The disconnection detection status can be checked from the A/D conversion results.

3.4.5 Internal Calibration Flow

Figure 30 shows the flow for internal calibration.

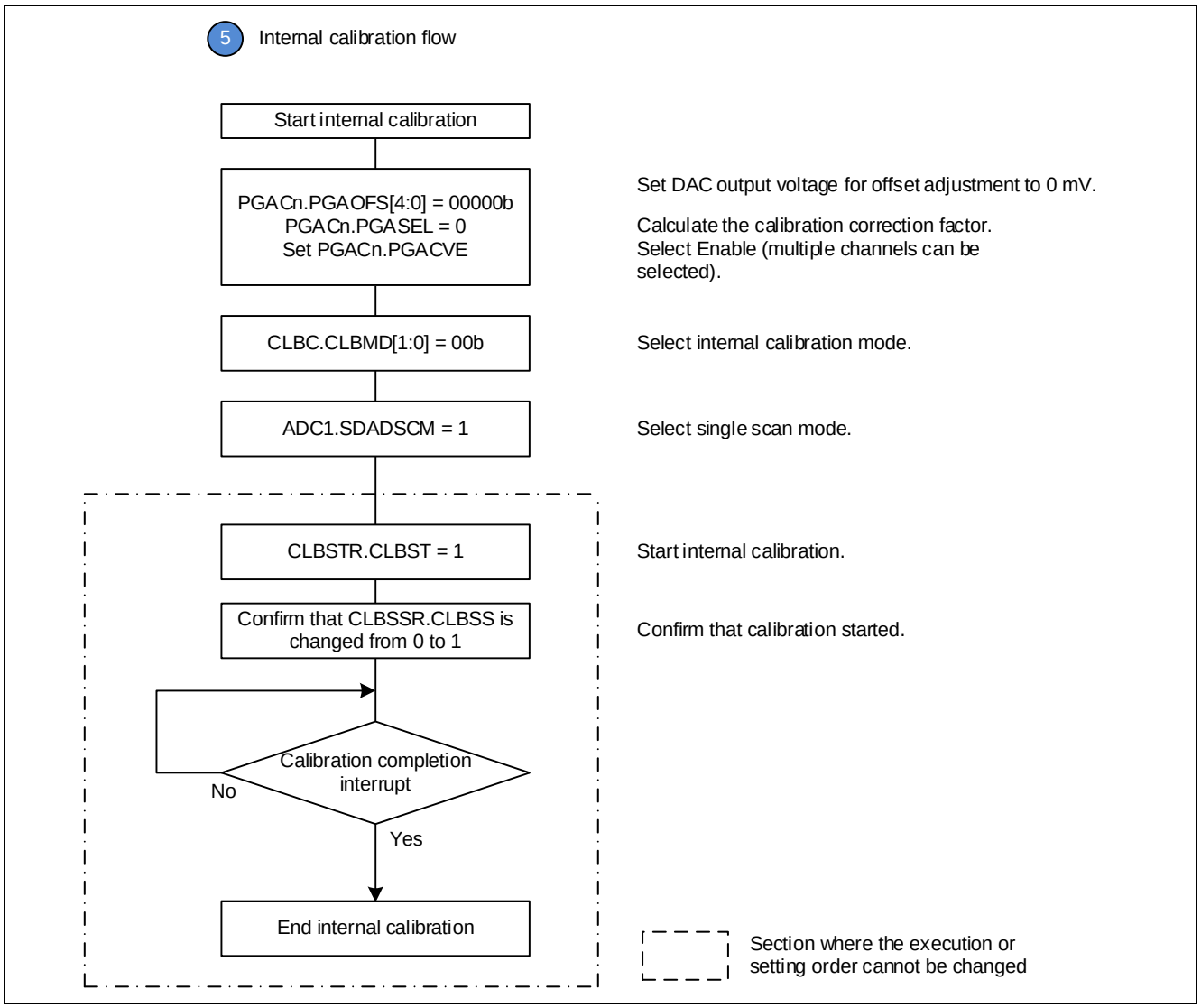

Figure 30. Internal Calibration Flow

3.4.6 External Calibration Flow

Figure 31 shows the flow for external calibration.

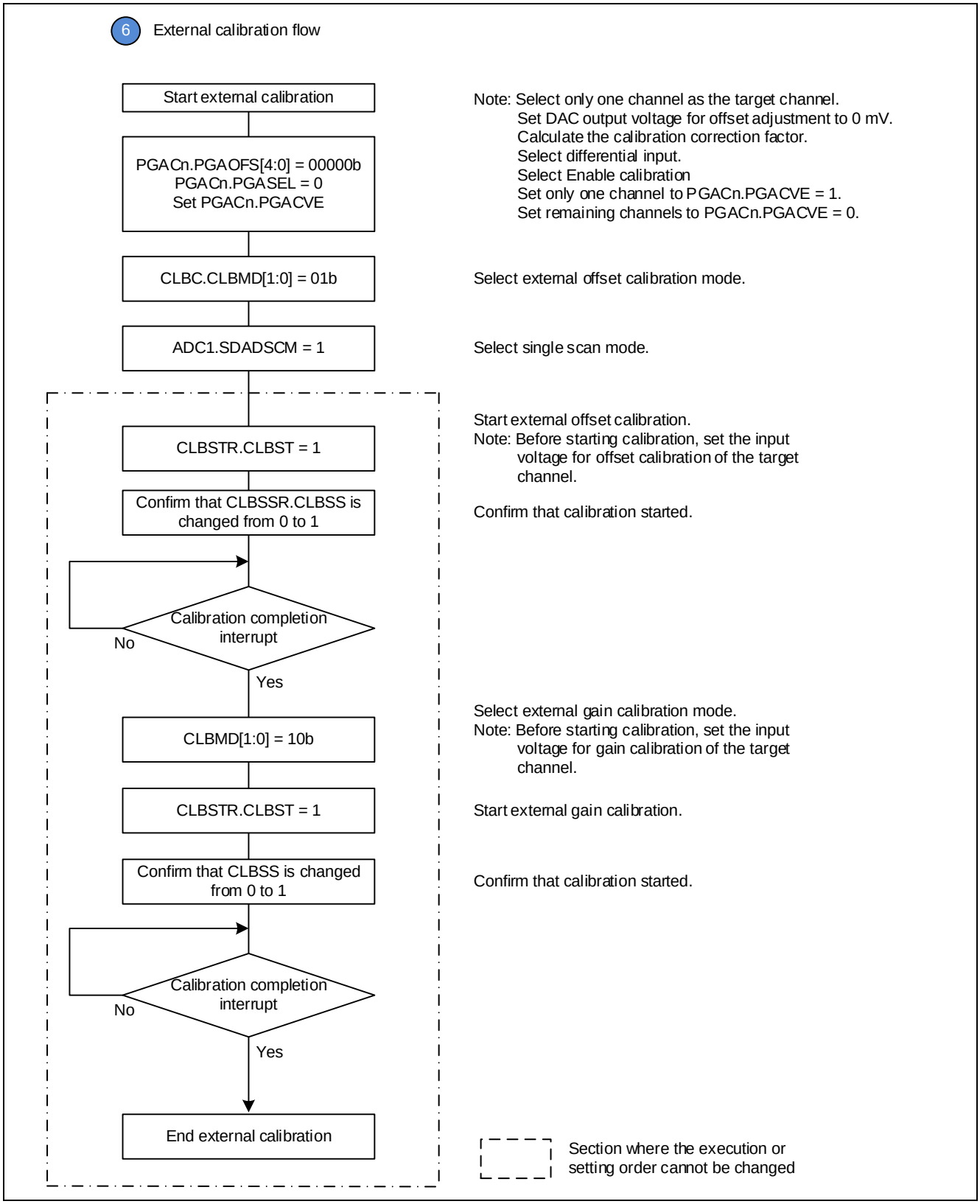

Figure 31. External Calibration Flow

Note: To perform external calibration for multiple channels, repeat this flow for each channel.

3.4.7 Recalibration Omitted Flow

Figure 32 shows the flow for omitting recalibration.

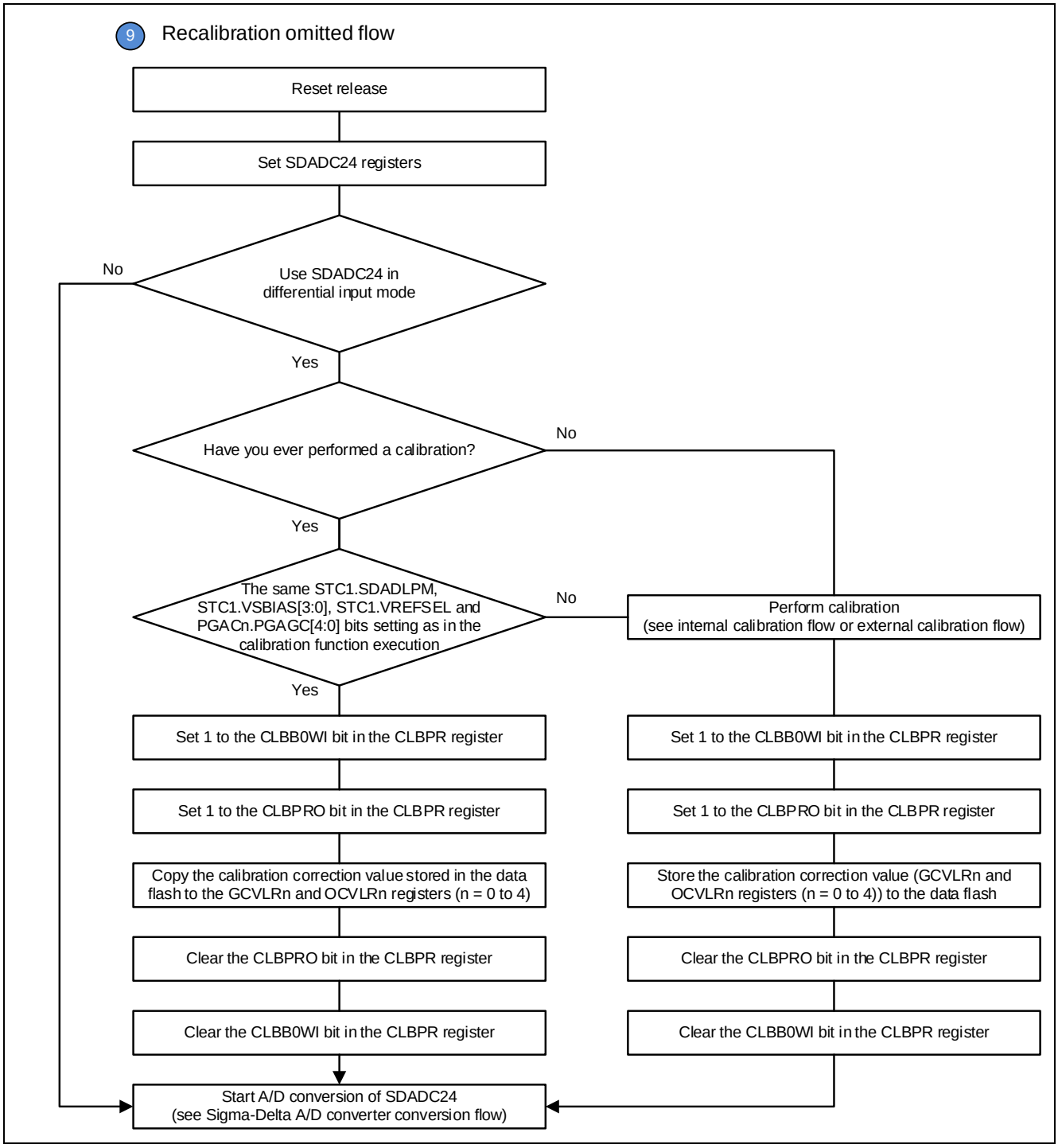

Figure 32. Recalibration Omitted Flow

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.19	—	First release document

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