GreenPAK Voltmeter with 2 digit LED display

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Introduction

What started out as a 7-segment LED digit display decoder/driver became the basis of voltmeter development using a single GreenPAK IC. Based on this Voltmeter circuit, designs can be extended to Tachometer, Thermometer, and SPI to DISPLAY devices. Device peculiarities are described below.

Display

Voltmeter construction requires 4-bit binary code conversion in order for the numbers to be shown on the 7-segment display. The display configuration table (Figure 1) helps to understand the decoder. Each segment of the indicator named a..g is controlled by one IC output pin.

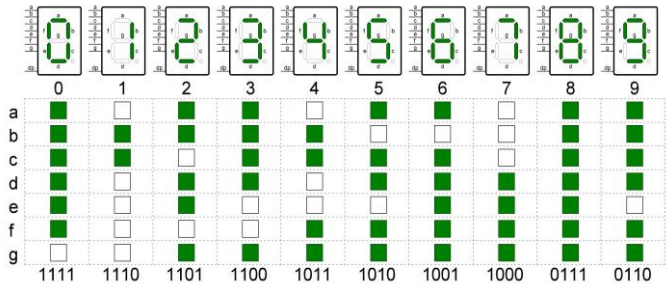


Figure 1. Display configuration table

Which segment to illuminate in order to show each number is also shown in Fig 1. Using this table for each segment, a decoder was created using LUTs (see Figure2).

Detailed decoder blocks configuration can be found in Appendix 1.

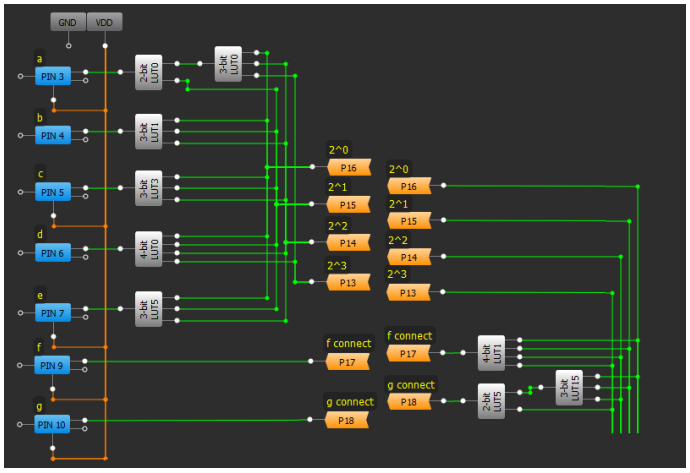


Figure 2. Decoder part review

Design approach

The Voltmeter input stage is a volt-interval converter based on the following cells: PGA, ADC and FSM0. It works as follows.

The ADC cell digitizes the input voltage value. Then the ADC data is loaded into a Finite state machine FSM0 is used as a counter with its output period dependent on the loaded data. When the input voltage is close to 0 volts, ADC data will be close to digital 0, which provides the shortest counter (FSM0) period and vice versa. When the input voltage is close to 1 volt, ADC data will be close to 255 and the FSM0 output period will be at its longest. For example, when ADC's input is at 0.5V, its output will be 128. FSM0's output will be a periodic waveform with a period of 128*FSM0 clock and a pulse width of 1 FSM0 clock.

The next circuit utilizes two 4-bit decimal counters (DC), implemented using DFF0, DFF1, DFF2, PIPE DELAY0 (for the first one) and DFF6, DFF7, DFF8, PIPE DELAY1 (for the second one) flip flops. These counters count 10 times from 1111_2 to 0110_2. After reaching the last value, the DCs will be reset by this design using 2-bit LUT1, 3-bit LUT2 for the first and 2-bit LUT6, 2-bit LUT7 for the second counter.

The first counter is used for the least significant digit, and the second one for the most significant digit.

The DCs interaction with the volt-interval converter is described as follows: A constant frequency signal is input to the first decimal counter (FDC) and its output value changes from 1111_2 to 0110_2. After that, 3-bit LUT2 generates a clock signal for the second decimal counter (SDC). So we receive a two-digit number and value between 0-99 in the specific binary code: FDC for the least significant digit and SDC for the most significant digit. At the FSM0 output's rising edge, it resets both DCs. At reset, the appropriate binary code is captured and decoded onto the 7 segment display. However, for the numerical values of the measured voltage and decimal counters contents to match, the decimal counters and FSM0 counter have to match in their periods. In other words, FSM0 clock times max FSM0 counter data (255) should be equal to DC clock times max DC data (99). In this design, FSM0 clock is sourced from CNT1(1.2ms) and DC clock is sourced from CNT0(3.1ms); 1.2*255=3.1*99. Since the DCs are always counting, they are not unsuitable for outputting signals directly to the display. So when FSM0 resets the DCs, their values are latched; LATCH3, LATCH4, LATCH5 and 3-bit LUT4 for FDC and LATCH10, LATCH11, 3-bit LUT13, 3-bit LUT14 for SDC. The circuit behaves as follows: When the FSM0 output goes HIGH, it is detected by the rising-edge detector (P DLY0), whose inverted signal sets the current values of DC into the latches. After this operation is finished, the second rising-edge detector (P DLY1) resets the DCs. After that, the data from latches is ready to be output to the display.

The ADC has a 50mV DC offset. This means that ADC outputs 0000_2 even when there is 50mV on its input. This problem can be solved with an ADC offset compensator circuit. It is built using 2-bit LUT3, CNT/DLY5, 3-bit LUT7 and 2-bit LUT2 cells. Its operation is as follows:

After the input voltage is applied, a HIGH level signal appears on the FSM0 output, and then 1111_2 code is set into the latch circuit (corresponds to 0 volt), and DCs are reset. FSM0 is stopped, because there is a high level on its RESET input. At the same time, DCs are operational. When the signal from FSM0 passes to the DLY5 cell output, then the RESET input of FSM0 will become LOW and FSM0 will start its operation.

Because of that circuit the equivalent of almost 50mV is added to the ADC. With that, the DCs' values will then be equal to a digital value of the measured analog voltage.

The digital compensation value is adjusted by choosing DLY5 counter data. Moreover, when DCs overflow happens, 2-bit LUT6, 2-bit LUT7, 2-bit LUT1 and 2-bit LUT2 cells provide full system reset (including FSM0).

Digits expansion

The GreenPAK IC contains enough internal circuitry to implement one display decoder, but we wanted a two digit display for this voltmeter. This is a circuit resource problem because we planned two DCs (representing two decimal numbers). To solve this problem a dynamic display driver was used.

For its implementation an RC OSC, DFF9, 3-bit LUT9, 3-bit LUT10, 3-bit LUT11, 3-bit LUT12 and 2-bit LUT4 cells were used. RC OSC output signal 20.8(3) kHz frequency is divided by two using DFF9 block to receive a signal with 50% duty cycle, which is necessary for even time (and intensity) division between two indicator displays.

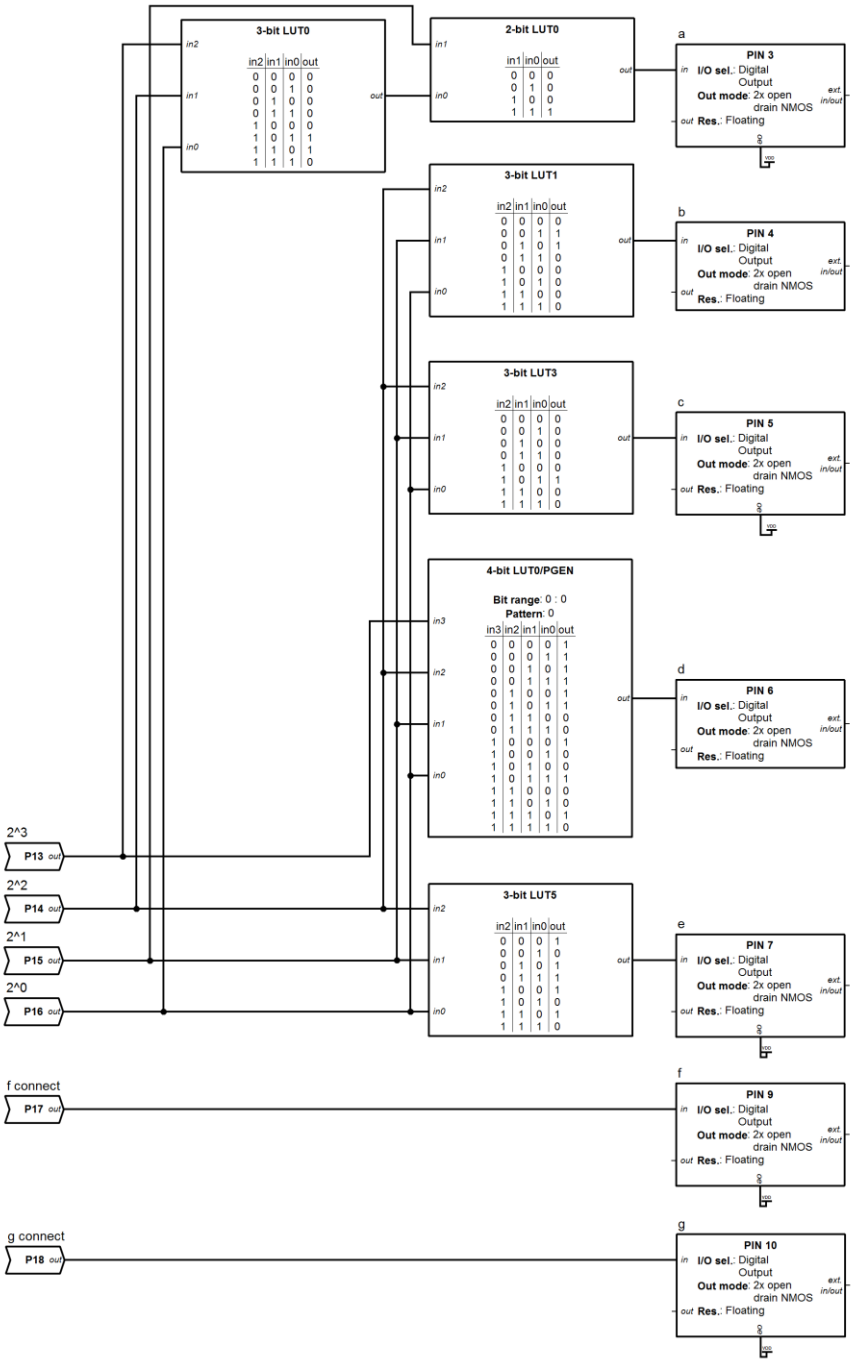
This control signal comes to a switch circuit, made of 3-bit LUT9, 3-bit LUT10, 3-bit LUT11, 3-bit LUT12, which provide alternating connection of FDC and SDC to the decoder.

In order to supply data to the proper indicator display (least significant digit or most significant digit) there are two additional outputs: SELECTOR_OUT 0x COM_ANODE (units indicator connection) and SELECTOR_OUT x0 COM_ANODE (tens indicator connection). These outputs are configured as open drain P-MOS. However, the decoder bus outputs are configured as open drain N-MOS. Using this configuration, the data from every DC comes to an appropriate display with 10 kHz frequency and 50% duty cycle. The design configuration can be found in Appendix 1. In Appendix 2 the schematic, PCB and device pictures are shown. Functional waveforms are shown in Appendix 3.

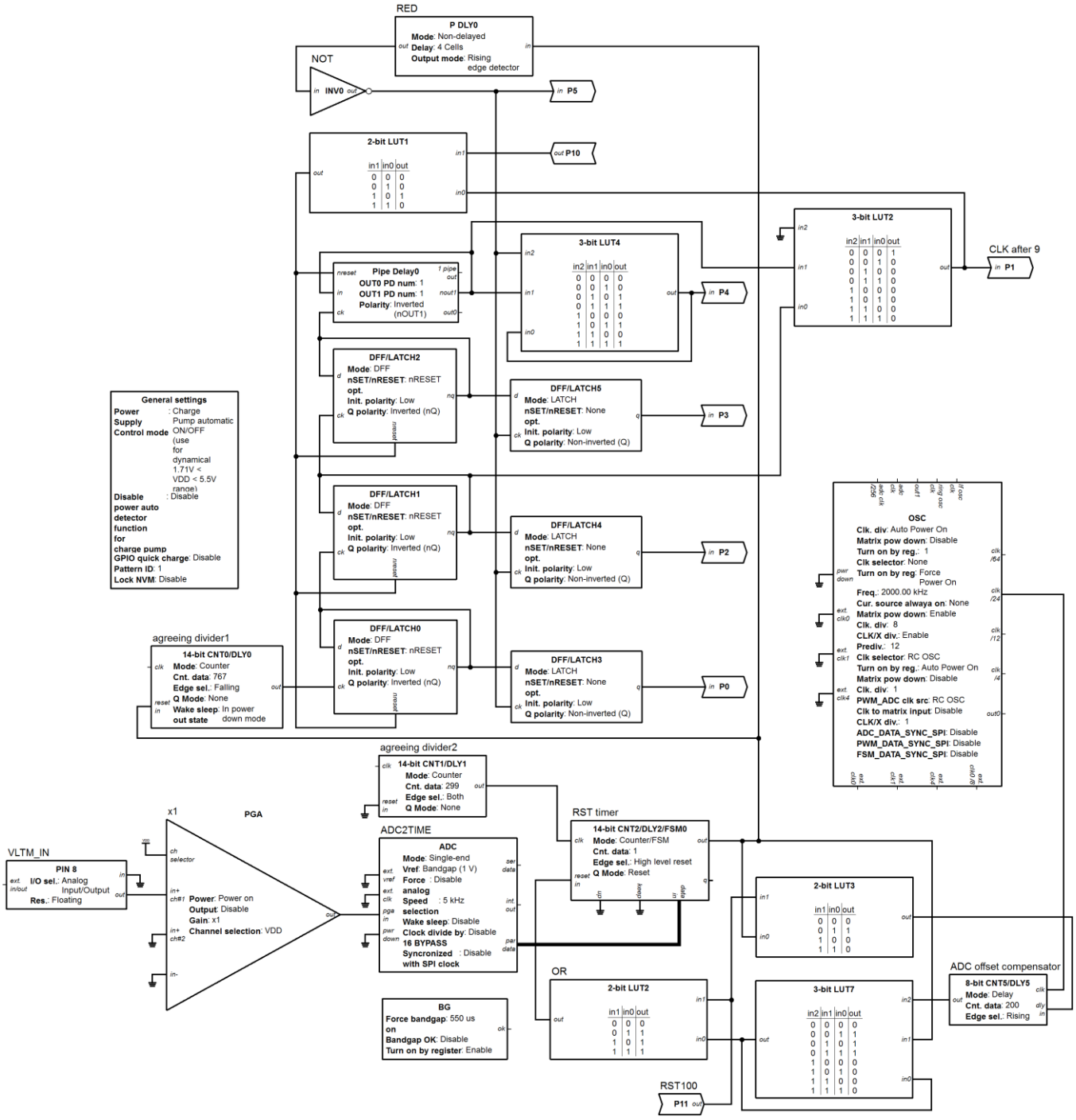
Conclusion

A 2-digit Voltmeter with 7-segment display has been proposed. Also demonstrated is how unexpectedly flexible the GreenPAK IC application can be. This design can be used for voltage measurements with two digits accuracy. The Voltmeter can be used as a voltage probe for Li-Ion Batteries or charging circuits. This Voltmeter can be used as a basis for other devices such as current meter, tachometer or thermometer.

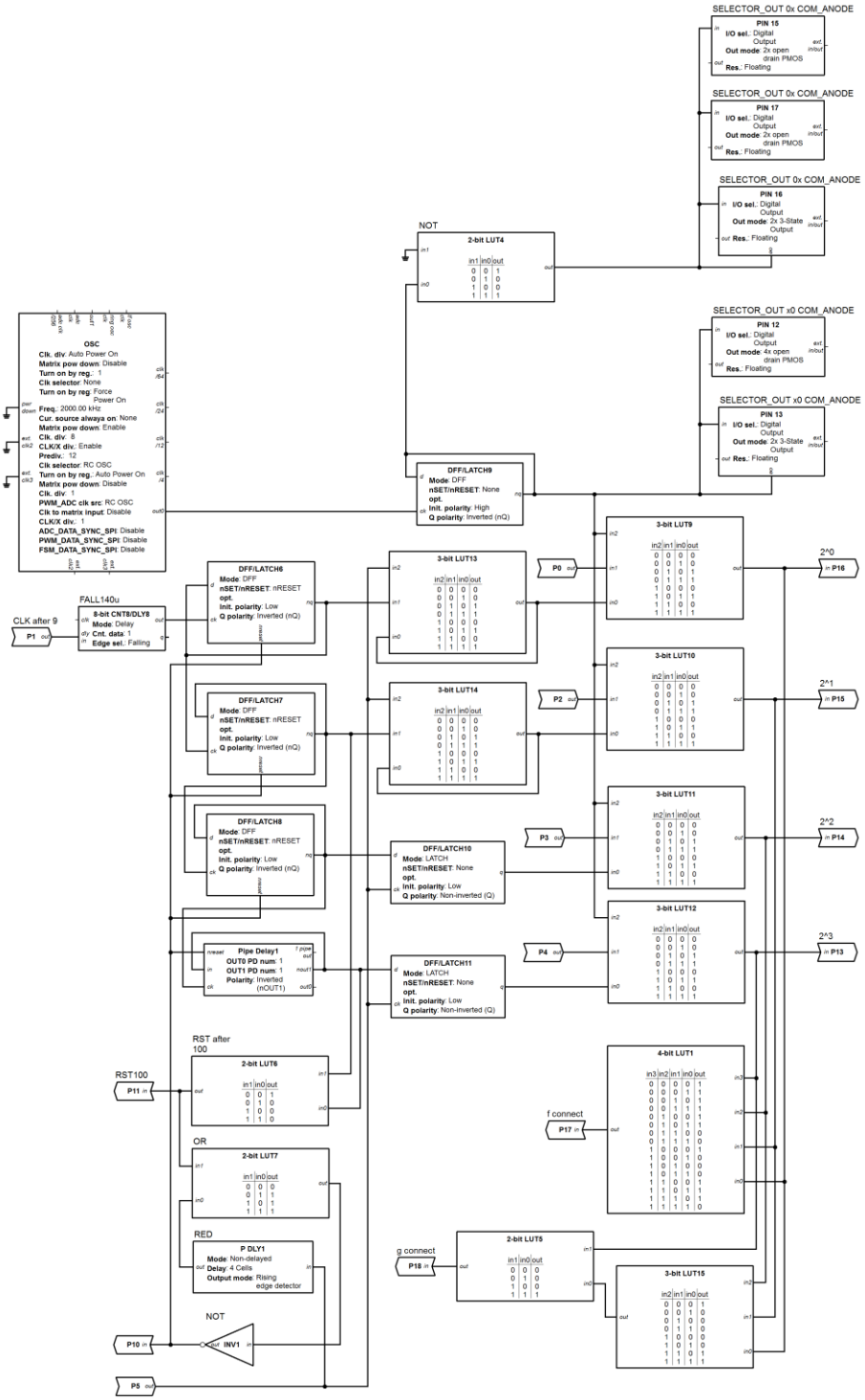
Appendix 1



Block Diagram for Design. Matrix0 Part 1. Decoder

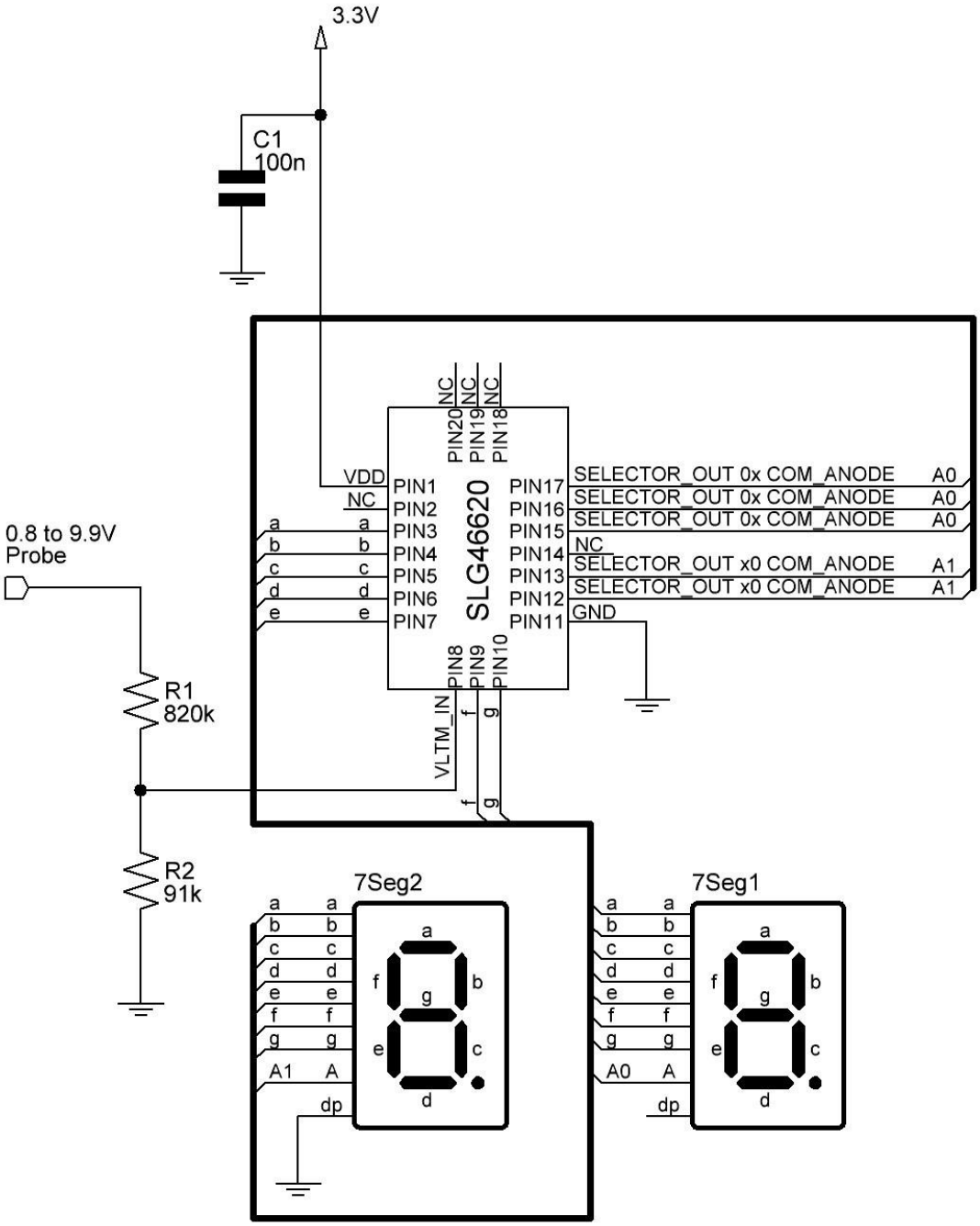


Block Diagram for Design. Matrix0 Part 2. Voltmeter architecture



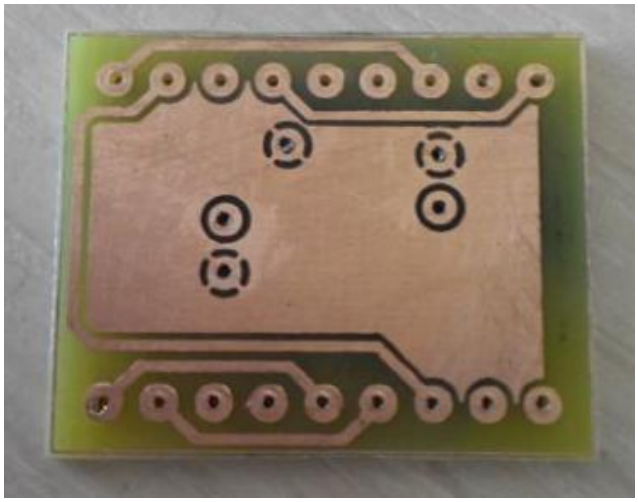
Block Diagram for Design. Matrix1 Part 3. Voltmeter architecture

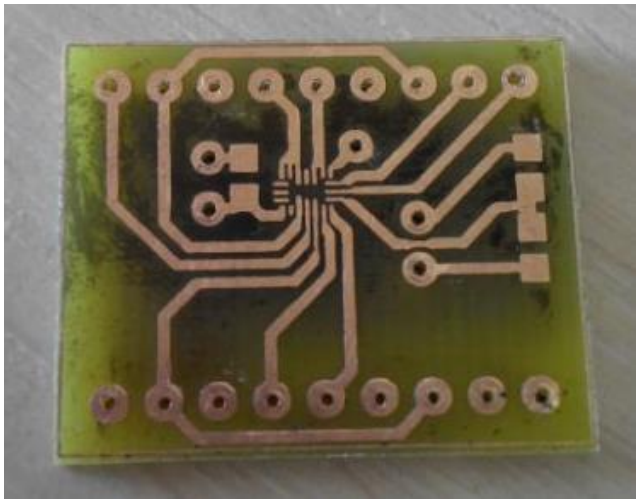
Appendix 2



Schematic

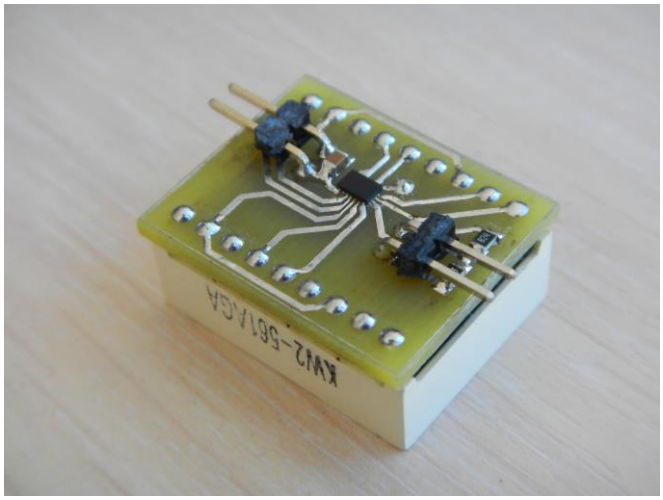
PCB pictures

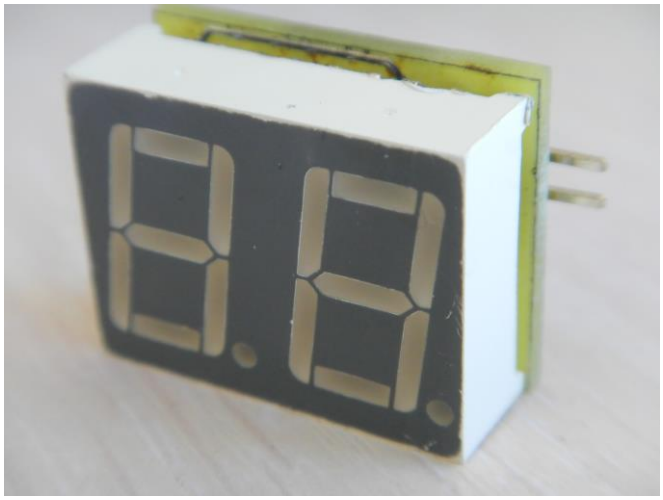




1. Bottom Layer
2. Top Layer

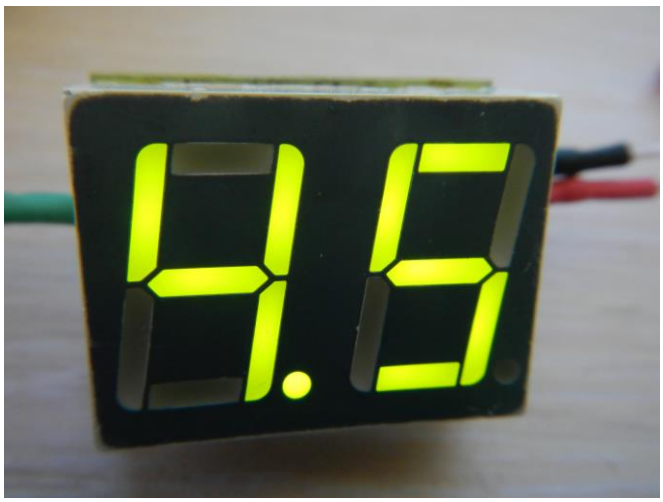
Devise pictures





1. Bottom device review:
2. Top device review

GPAK chip & SMD details



3. Voltage measurement 3.2V
4. Voltage measurement 4.5V

Appendix 3. Functionality waveforms

Channel 1 (yellow/top line) – PIN#8 (VLTM_IN)

Channel 2 (light blue/2nd line) – PIN#12 (SELECTOR_OUT x0 COM_ANODE) with external 5kΩ pull down resistor

Channel 4 (green/3rd line) – PIN#15 (SELECTOR_OUT 0x COM_ANODE) with external 5kΩ pull down resistor

D0 – PIN#3 (a) with external 5kΩ pull up resistor

D1 – PIN#4 (b) with external 5kΩ pull up resistor

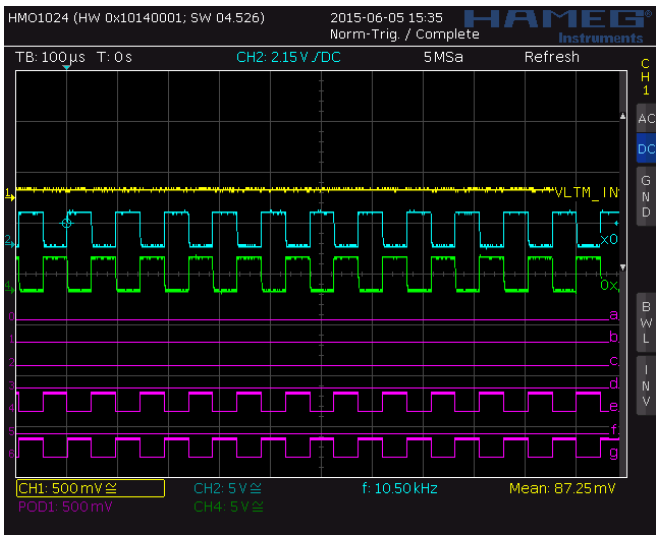
D2 – PIN#5 (c) with external 5kΩ pull up resistor

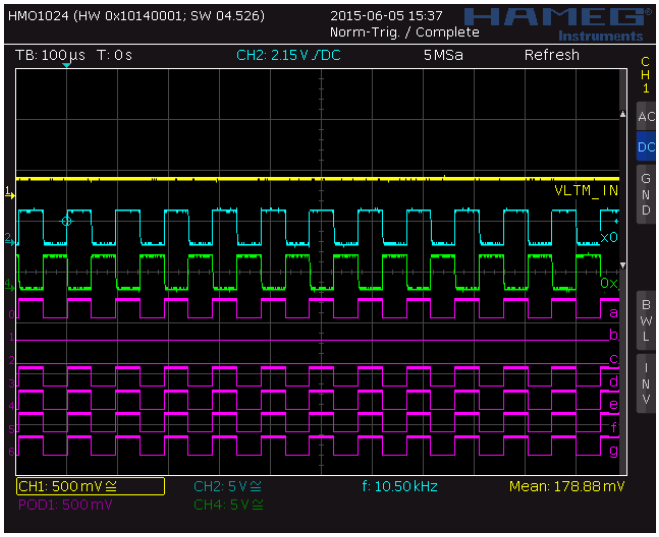
D3 – PIN#6 (d) with external 5kΩ pull up resistor

D4 – PIN#7 (e) with external 5kΩ pull up resistor

D5 – PIN#9 (f) with external 5kΩ pull up resistor

D6 – PIN#10 (g) with external 5kΩ pull up resistor





1. 90 mV on ADC input (‘0’ and ‘9’ are displayed)
2. 180 mV on ADC input (‘1’ and ‘8’ are displayed)

Channel 1 (yellow/top line) – PIN#8 (VLTM_IN)

Channel 2 (light blue/2nd line) – PIN#12 (SELECTOR_OUT x0 COM_ANODE) with external 5kΩ pull down resistor

Channel 4 (green/3rd line) – PIN#15 (SELECTOR_OUT 0x COM_ANODE) with external 5kΩ pull down resistor

D0 – PIN#3 (a) with external 5kΩ pull up resistor

D1 – PIN#4 (b) with external 5kΩ pull up resistor

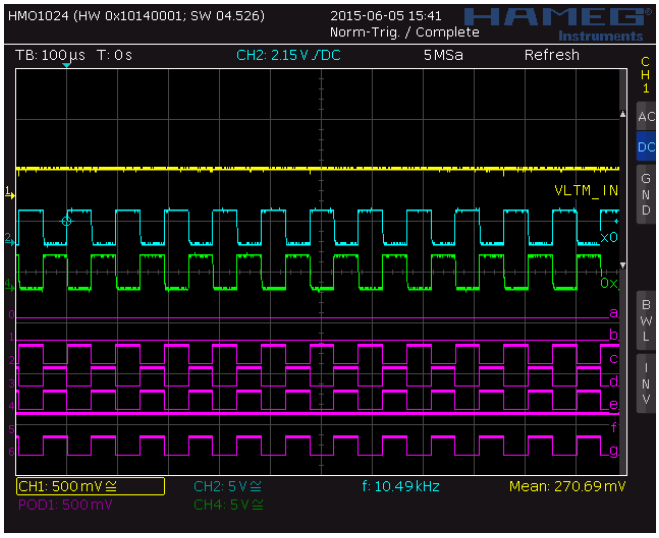
D2 – PIN#5 (c) with external 5kΩ pull up resistor

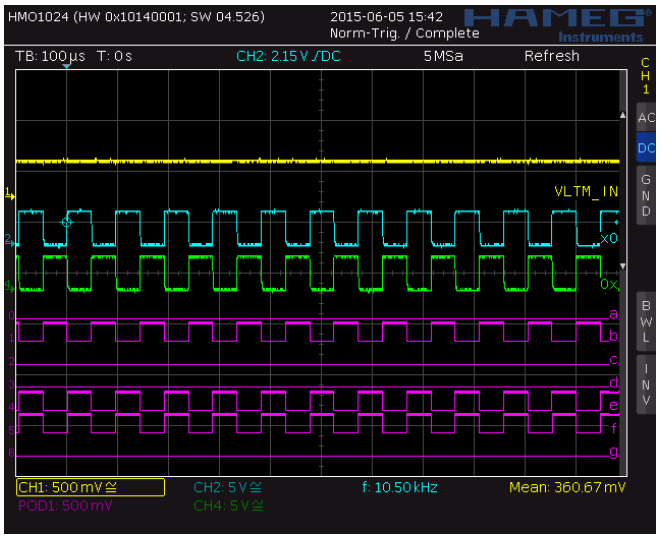
D3 – PIN#6 (d) with external 5kΩ pull up resistor

D4 – PIN#7 (e) with external 5kΩ pull up resistor

D5 – PIN#9 (f) with external 5kΩ pull up resistor

D6 – PIN#10 (g) with external 5kΩ pull up resistor





3. 270 mV on ADC input (‘2’ and ‘7’ are displayed)
4. 360 mV on ADC input (‘3’ and ‘6’ are displayed)

Channel 1 (yellow/top line) – PIN#8 (VLTM_IN)

Channel 2 (light blue/2nd line) – PIN#12 (SELECTOR_OUT x0 COM_ANODE) with external 5kΩ pull down resistor

Channel 4 (green/3rd line) – PIN#15 (SELECTOR_OUT 0x COM_ANODE) with external 5kΩ pull down resistor

D0 – PIN#3 (a) with external 5kΩ pull up resistor

D1 – PIN#4 (b) with external 5kΩ pull up resistor

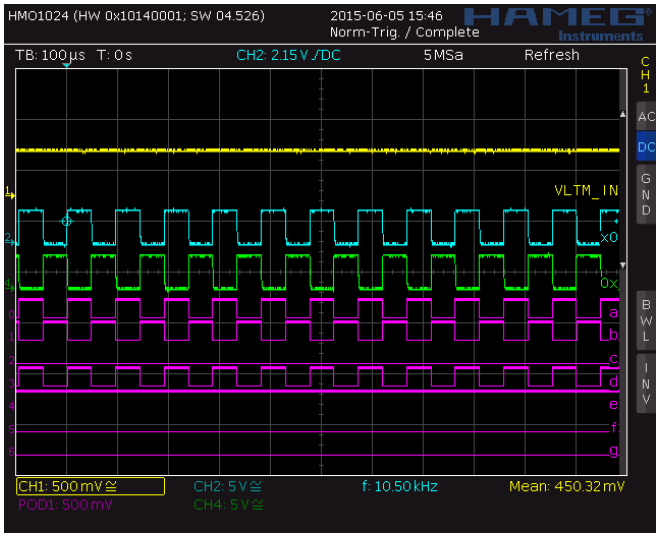
D2 – PIN#5 (c) with external 5kΩ pull up resistor

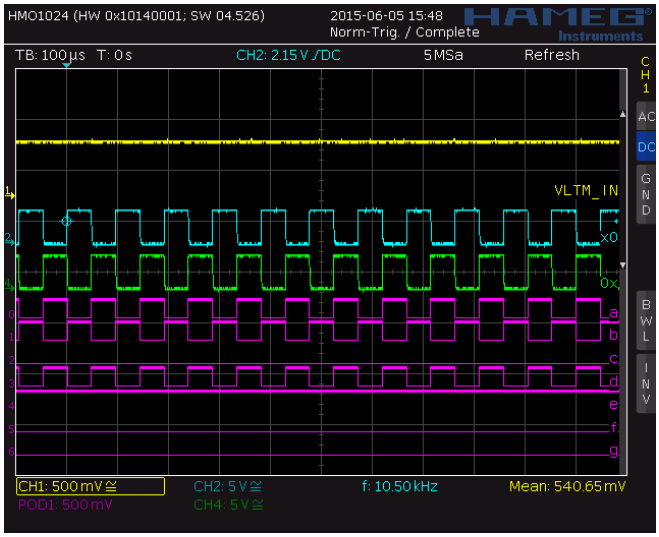
D3 – PIN#6 (d) with external 5kΩ pull up resistor

D4 – PIN#7 (e) with external 5kΩ pull up resistor

D5 – PIN#9 (f) with external 5kΩ pull up resistor

D6 – PIN#10 (g) with external 5kΩ pull up resistor





5. 450 mV on ADC input (‘4’ and ‘5’ are displayed)
6. 540 mV on ADC input (‘5’ and ‘4’ are displayed)

Channel 1 (yellow/top line) – PIN#8 (VLTM_IN)

Channel 2 (light blue/2nd line) – PIN#12 (SELECTOR_OUT x0 COM_ANODE) with external 5kΩ pull down resistor

Channel 4 (green/3rd line) – PIN#15 (SELECTOR_OUT 0x COM_ANODE) with external 5kΩ pull down resistor

D0 – PIN#3 (a) with external 5kΩ pull up resistor

D1 – PIN#4 (b) with external 5kΩ pull up resistor

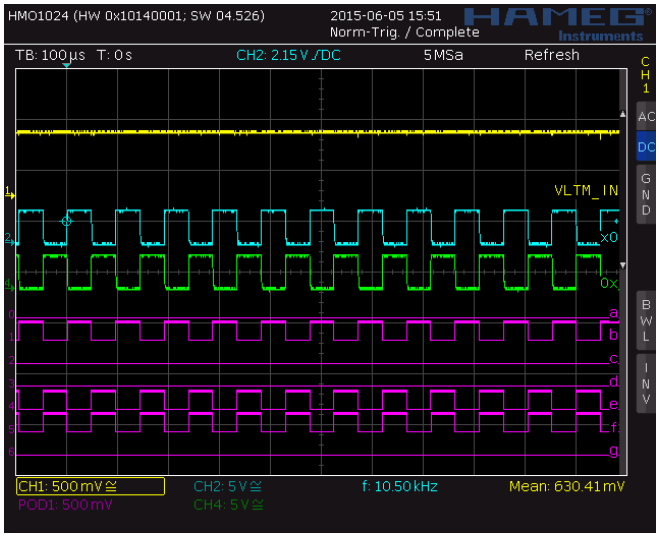
D2 – PIN#5 (c) with external 5kΩ pull up resistor

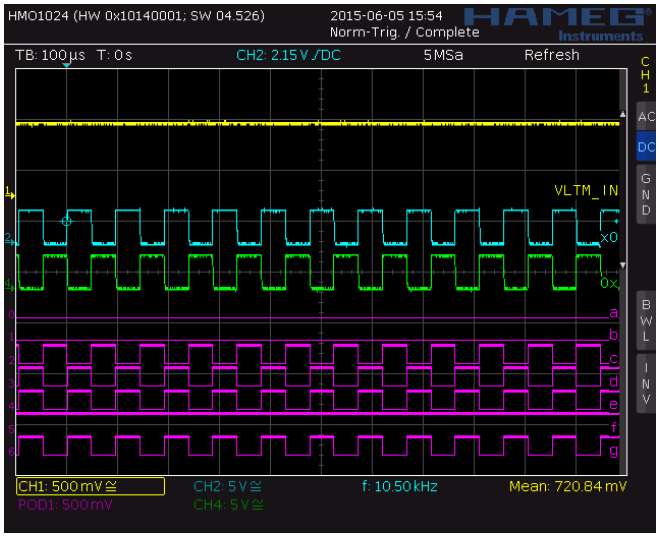
D3 – PIN#6 (d) with external 5kΩ pull up resistor

D4 – PIN#7 (e) with external 5kΩ pull up resistor

D5 – PIN#9 (f) with external 5kΩ pull up resistor

D6 – PIN#10 (g) with external 5kΩ pull up resistor





7. 630 mV on ADC input (‘6’ and ‘3’ are displayed)
8. 720 mV on ADC input (‘7’ and ‘2’ are displayed)

Channel 1 (yellow/top line) – PIN#8 (VLTM_IN)

Channel 2 (light blue/2nd line) – PIN#12 (SELECTOR_OUT x0 COM_ANODE) with external 5kΩ pull down resistor

Channel 4 (green/3rd line) – PIN#15 (SELECTOR_OUT 0x COM_ANODE) with external 5kΩ pull down resistor

D0 – PIN#3 (a) with external 5kΩ pull up resistor

D1 – PIN#4 (b) with external 5kΩ pull up resistor

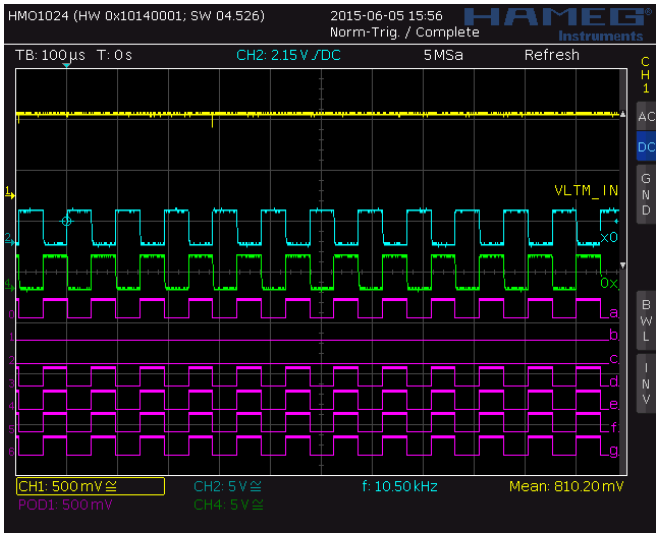
D2 – PIN#5 (c) with external 5kΩ pull up resistor

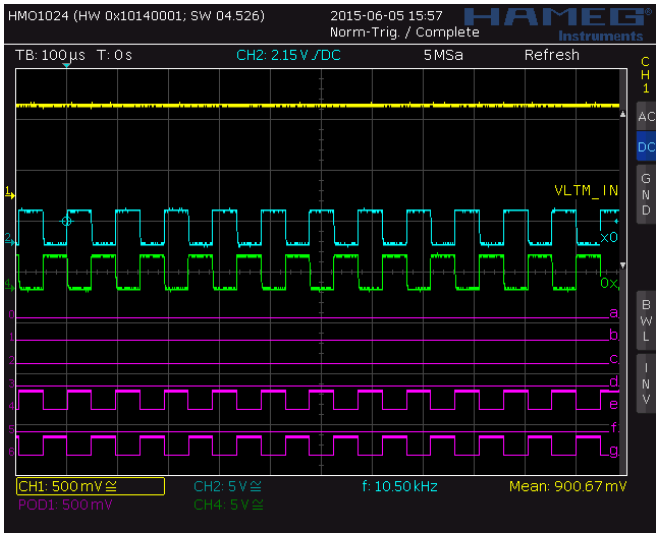
D3 – PIN#6 (d) with external 5kΩ pull up resistor

D4 – PIN#7 (e) with external 5kΩ pull up resistor

D5 – PIN#9 (f) with external 5kΩ pull up resistor

D6 – PIN#10 (g) with external 5kΩ pull up resistor





9. 810 mV on ADC input (‘8’ and ‘1’ are displayed)
10. 900 mV on ADC input (‘9’ and ‘0’ are displayed)

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