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Introduction

It is often necessary to divide a signal frequency by a fixed coefficient, which is simple if this coefficient is an even number equal to 2, 4, 8 and so on. However, dividing by odd or fractional coefficients is a more complicated task. Using the LUTs and DFFs resources in GreenPAK, one can efficiently divide a given frequency by 1.5, 2.5, 3, 3.5, 4.5, 5, and many other coefficients.

Figure 2. LUTs properties

Frequency divide by 1.5, 3, 3.5

Here DFFs each provide frequency division by 2, while XOR LUTs are used to eliminate the odd half input clock which comes to the first DFF. This makes it possible to get coefficients 2-0.5=1.5; 1.5*2=3; 4-0.5=3.5.

Blocks configurations are shown in figures 1-5 below.

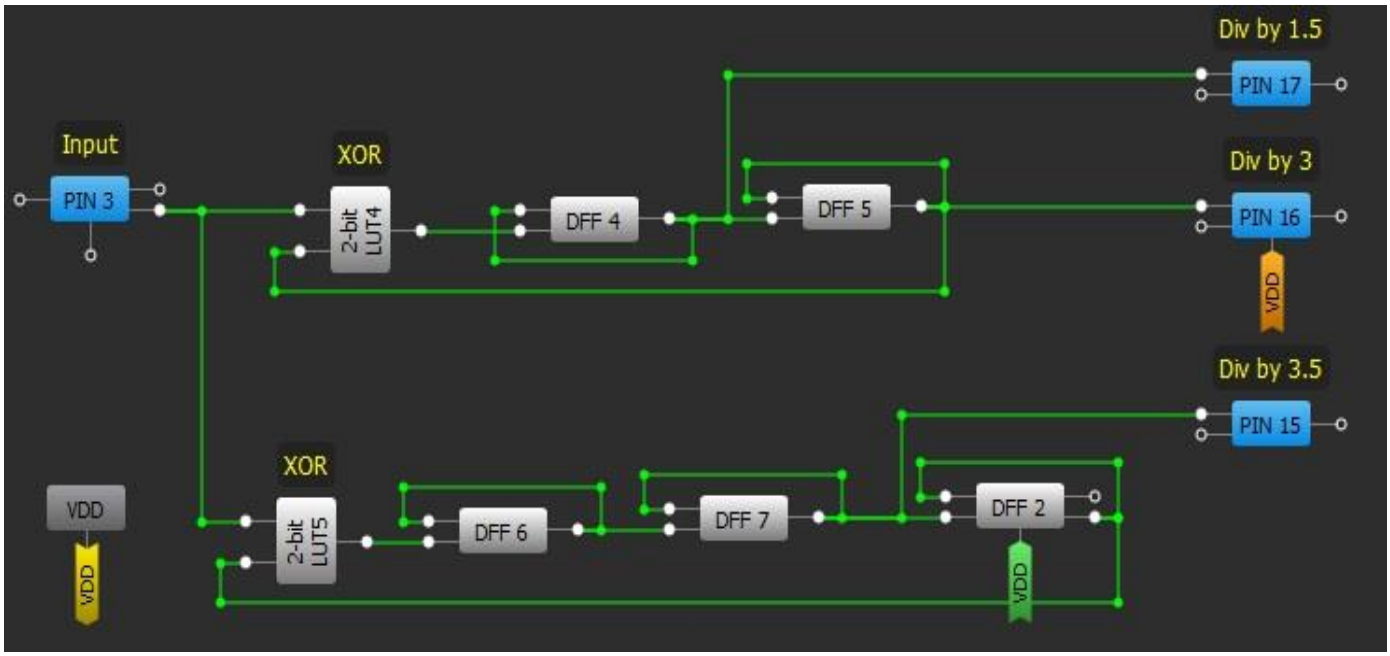

Figure 1. Frequency divide by 1.5, 3, 3.5 circuit design

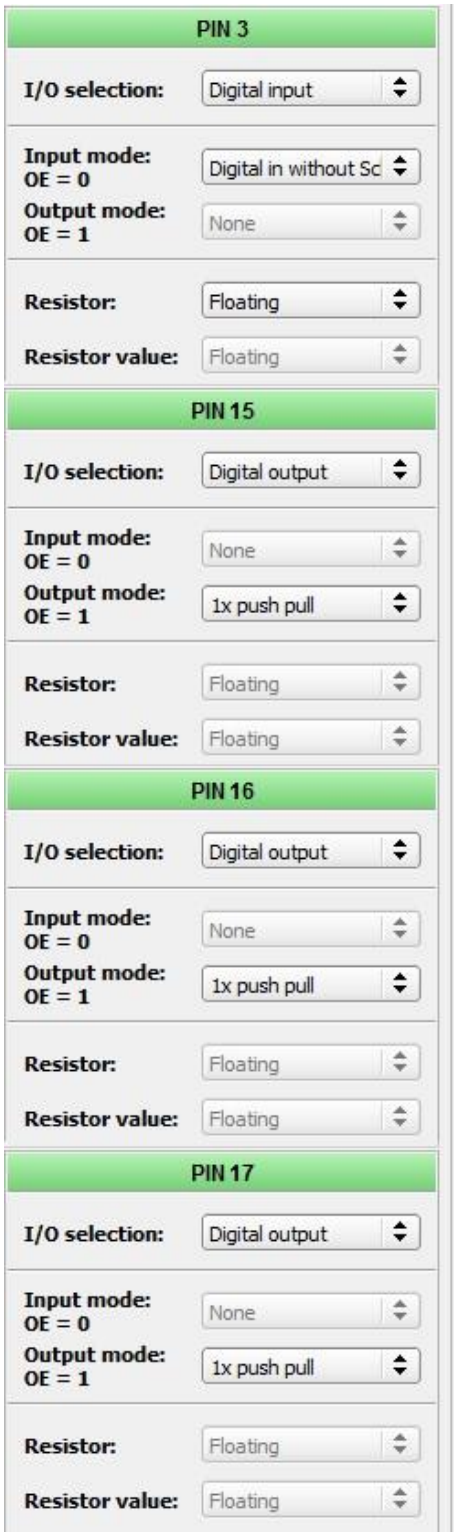

Figure 3. Pins properties

Figure 4. DFFs properties

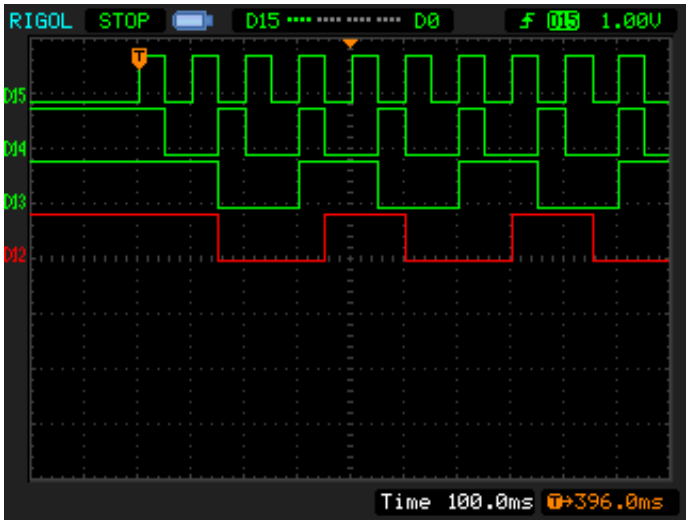

Figure 5. Frequency divider functional diagram

**(D15 – Input signal; D14 – F/1.5;
D13 – F/3; D12 – F/3.5)**

Frequency divide by 2.5, 5

This case operates differently than the previous 1.5, 3, 3.5 example. Here, the same CLK signal is supplied to a string of DFF CK inputs, but LUTs and feedback reconfigure their D inputs. In this way frequency division by 2.5 can be designed. DFF3 is used to divide by 2 a previously divided by 2.5 frequency and output the divide by 5 signal.

Blocks configurations are shown in figures 6-9.

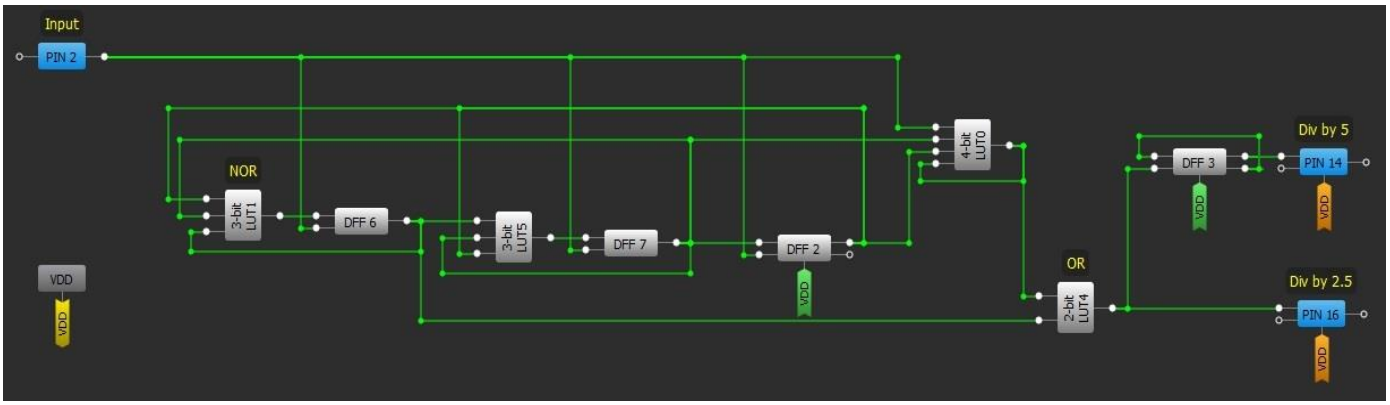

Figure 6. Frequency divider by 2.5; 5 circuit design

Figure 7. Pins properties

Figure 8. LUTs properties

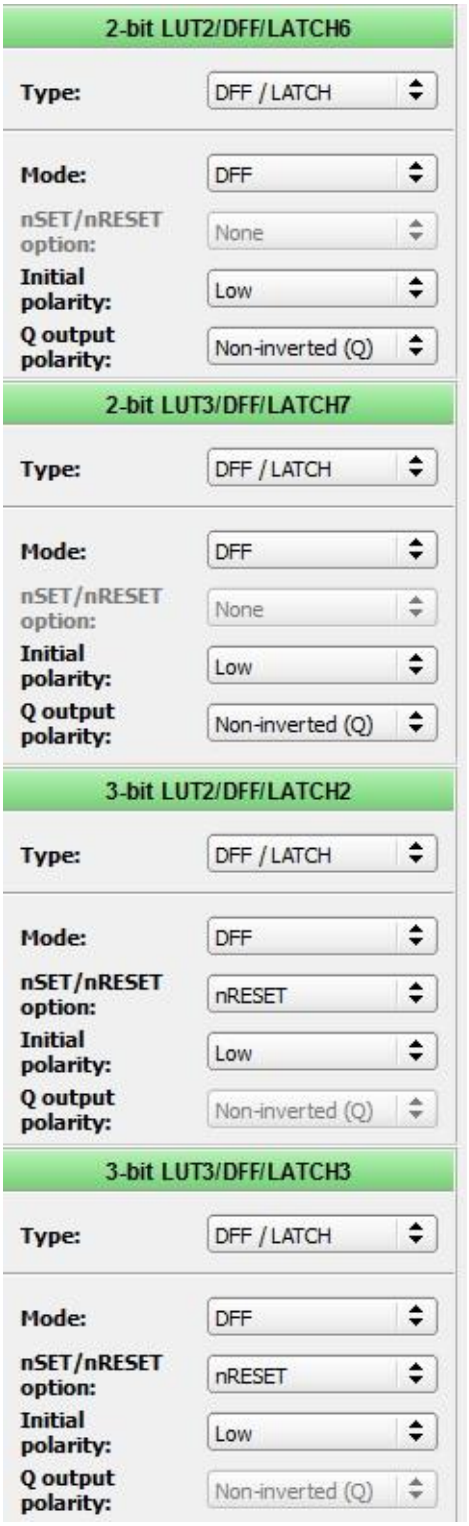

Figure 9. DFFs properties

By taking a signal from the other DFFs outputs it is possible to get a divide by 5 signal as well, but with different duty cycle (not 50%, as previously) and phase shift (see figure 10): D3 – DFF2, D4 – DFF7, D5 – DFF6.

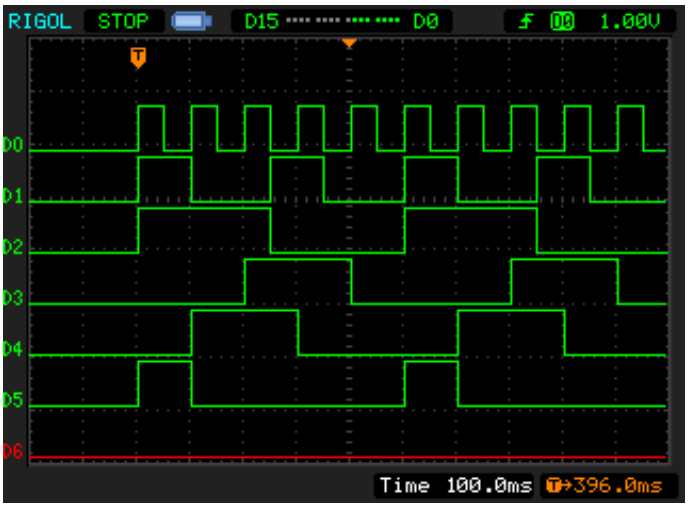

Figure 10. Frequency divider functional diagram (D0 – Input signal; D1 – F/2.5; D2, D3, D4, D5 – F/5)

Frequency divide by 4.5

Frequency division by 4.5 circuit is based on the previous circuit (divider by 5).

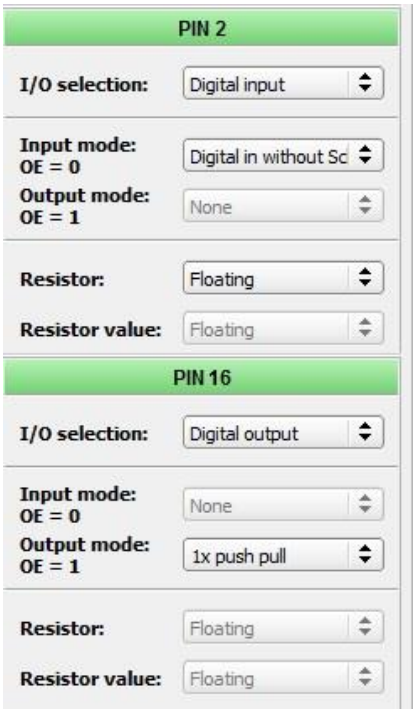

Figure 12. Pins properties

There are some additional blocks (DFF4 and 2-bit LUT5) which provide elimination of half clock period for DFFs (as in the divide by 1.5, 3, 3.5 circuit). This allows us to get divide by 4.5.

Blocks configurations are shown in figures 11-14.

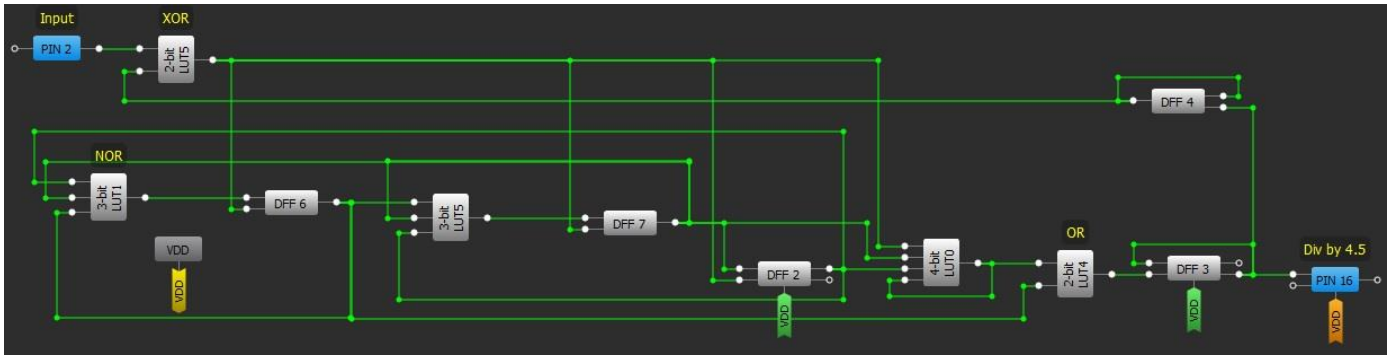

Figure 11. Frequency divide by 4.5 circuit design

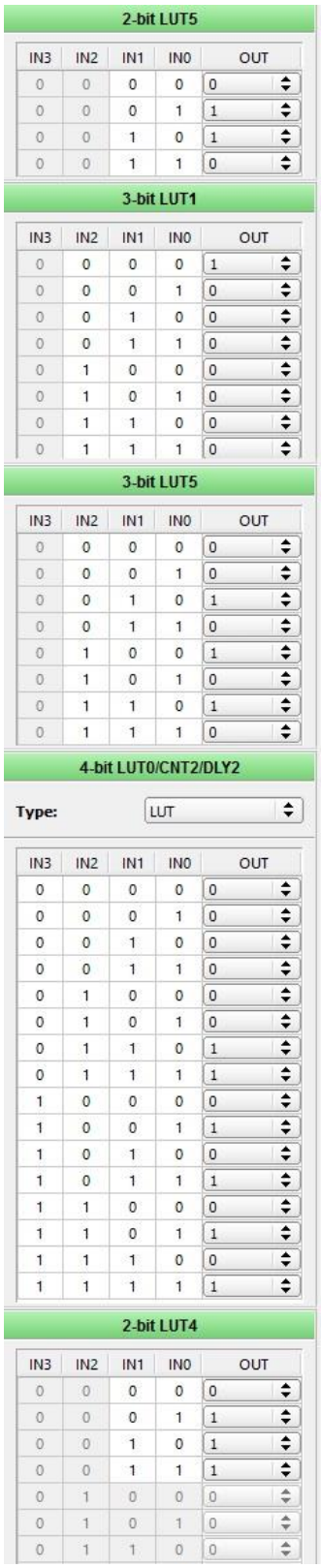

Figure 13. LUTs properties

Figure 14. DFFs properties

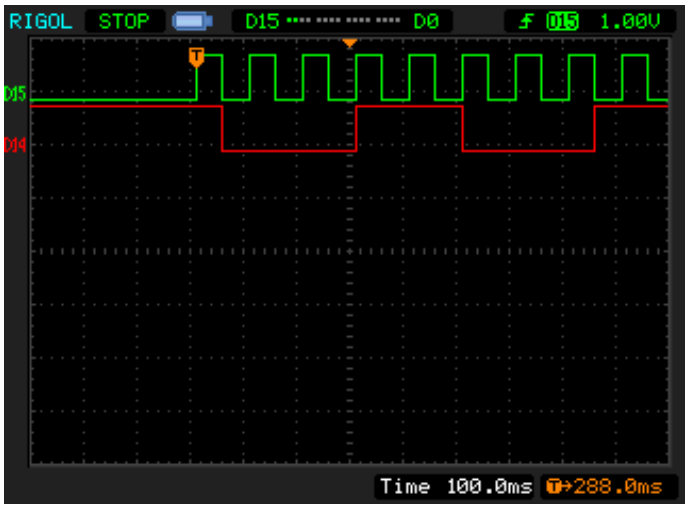

Figure 15. Frequency divider functional waveforms

(D15 – Input signal; D14 – F/4.5)

Conclusion

Frequency dividers which are typically not simple to realize can be constructed using LUTS and DFFs. As was shown, it is possible to divide a frequency by 1.5, 2.5, 3, 3.5, 4.5, 5. Such circuits may be used as a single device or as a part of a larger circuit.

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