Timing Accuracy for eCPRI Fronthaul and Open RAN

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Introduction

Open RAN is an eCPRI-based open fronthaul interface between the radio unit (RU) and distributed unit (DU) [1]. This white paper discusses timing accuracy for eCPRI fronthaul transport networks.

The eCPRI interface is supported by packet switched fronthaul transport networks. When the fronthaul network is used to synchronize an eCPRI node, it must provide timing at the user network interface according to the relevant 3GPP timing accuracy category. Time error budgets for 4 timing accuracy categories are given by the eCPRI Transport Network Requirements Specification [2].

Time synchronization for eCPRI nodes can be accomplished using the precision time protocol (PTP) per IEEE 1588 [3]. The ITU-T maintains a set of recommendations including G.8271.1 [4] and G.8273.2 [5] that cover PTP based synchronization. The ITU-T recommendations define the characteristics of telecom boundary clocks (T-BC) and telecom time slave clocks (T-TSC) that are used for PTP based synchronization; and they describe methods to estimate time error accumulation in networks.

The time error characteristics of the clocks within DUs, RUs, and switches and routers have a direct bearing on how many T-BC hops can be supported by the time error budget of a fronthaul network. The greater the number of T-BC hops the lower the number of primary reference time clocks (PRTC) that will be required and the lower the deployment cost. Further, the greater the number of allowed T-BC hops the greater the flexibility in the deployment.

Renesas **time synchronization hardware** and software products meet the tight time error requirements of eCPRI and Open RAN equipment. The product line includes system synchronizers for DUs, switches and routers used in fronthaul networks, and radio synchronizers for RUs. **Linux oriented PTP software** is available for both families of synchronizer products.

Renesas also offers a wide range of **jitter attenuators**, **clock generators**, clock synthesizers and **clock buffers** for **wireline** and **wireless timing applications**.

Acronyms

3GPP	3rd Generation Partnership Project	**RU**	Radio unit
CPRI	Common Public Radio Interface	**TAE**	Time alignment error
DU	Distributed unit	**T-BC**	Telecom boundary clock
FFO	Fractional frequency offset	**TE**	Time error
RAN	Radio access network	**T-GM**	Telecom grand master
PPS	Pulse per second	**T-TSC**	Telecom time slave clock
PRTC	Primary reference time clock	**UNI**	User network interface
PTP	Precision time protocol		

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Definitions

eCPRI

An interface defined by the CPRI industry cooperation for connecting eCPRI radio equipment control and eCPRI radio equipment via a fronthaul transport network

Maximum time error

The maximum of the absolute values of a set of time errors

Relative time error

The absolute value of the difference between time errors represented at two reference points

Time alignment error

The relative time eror between transmitter antenna ports

Time error

The difference between the time represented at a reference point and the time represented by an agreed common time reference [e.g., the Temps Atomique International (TAI)]

Time error budget

The maximum allowed for the relative time error between the input and output of a network or network element

Specifications for Timing Accuracy in Fronthaul Networks

O-RAN.WG4.CUS.0-v07.00

O-RAN.WG4.CUS.0-v07.00 [6] includes the specification of the O-RAN synchronization plane (S-Plane); it is available from the O-RAN Alliance. The O-RAN specification is eCPRI based [1].

eCPRI Transport Network Requirements Specification

The eCPRI Transport Network Requirements Specification [2] (eCPRI specification) defines the timing accuracy requirements for eCPRI transport networks.

IEEE 802.1CM™

IEEE 802.1CM™ [7] defines parameters that enable Ethernet bridged networks to transport time sensitive fronthaul streams.
IEEE 802.1CM™ includes time error budget calculations for the eCPRI timing categories and T-TSC deployment cases.

ITU-T G.8271.1

ITU-T G.8271.1 [4] (G.8271.1) defines network limits for time synchronization in packet networks with full timing support from the network. G.8271.1 describes network reference models and sets limits for time error at various reference points within networks; this recommendation also defines the synchronization deployment cases. G.8271.1 includes informative appendices that describe simplified, and simulation based methods to analyze time error accumulation.

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ITU-T G.8273.2

ITU-T G.8273.2 [5] (G.8273.2) defines the time characteristics of T-BCs and T-TSCs for use with full time support from the network. G.8273.2 specifies the time error characteristics for T-BCs and T-TSCs, class B and class C.

Time Error Budgets for eCPRI Fronthaul Networks

The eCPRI specification sets time error (TE) budgets for the user network interface (UNI) for fronthaul networks so that the time alignment error (TAE) requirements for four categories of 3GPP features and RANs are met. The eCPRI specification also defines the TE budgets for the T-TSCs that synchronize the RUs in two time synchronization deployment cases. The TE budget for RUs is not explicitly given, but it can be derived from the eCPRI specification.

This white paper focuses on eCPRI timing accuracy categories A, B and C, and time synchronization deployment cases 1.1 and 1.2 because these are most relevant to Open RAN applications.

Reference Points for eCPRI Fronthaul Networks

Figure 1 illustrates the |TE| and |TAE| reference points for eCPRI. Some of the reference points are named differently vs. the eCPRI specification for consistency with other sections of this document[1]. The synchronization source could be a PRTC+T-GM, or a DU that is directly or remotely synchronized by a PRTC

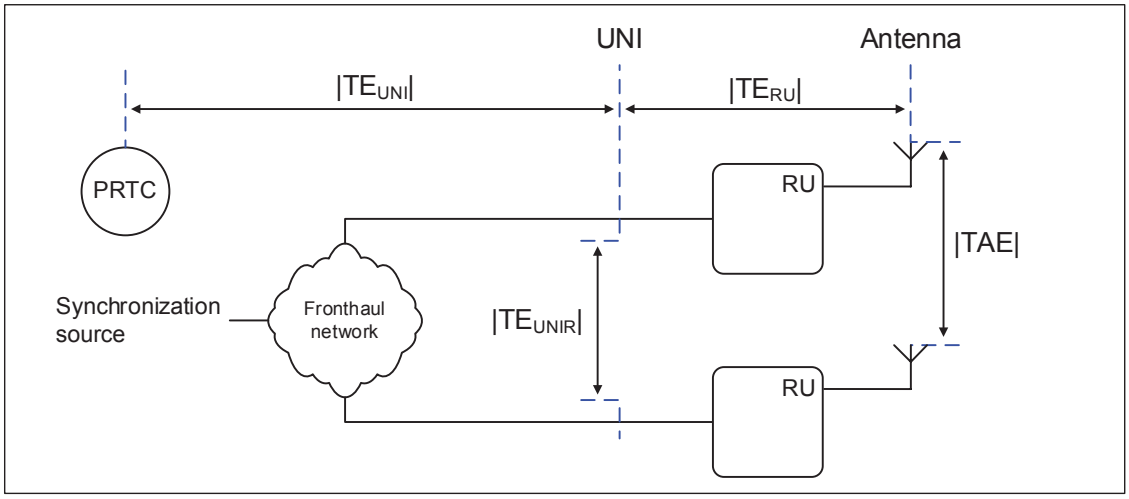

Figure 1: Fronthaul |TE| and |TAE| Reference Points

The terms used in Figure 1 are defined as follows:

- TE_{RU} refers to the time error budget for an RU
- TE_{UNI} refers to the maximum time error for a UNI
- TE_{UNIR} refers to the relative time error budget between two UNIs

[1] For the purposes of this white paper, the eCPRI radio equipment time error budget is applied to the radio unit.

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Time Synchronization Deployment Cases for eCPRI Fronthaul Networks

Figure 2 shows two fronthaul time synchronization deployment cases; these cases are defined in G.8271.1.

Deployment case 1

- The T-TSC is embedded in the RU (end application equipment)
- The T-TSC time error budget is included on the RU side of the UNI

Deployment case 2

- The T-TSC is external to the RU (end application equipment)
- The T-TSC time error budget is included on the fronthaul network side of the UNI

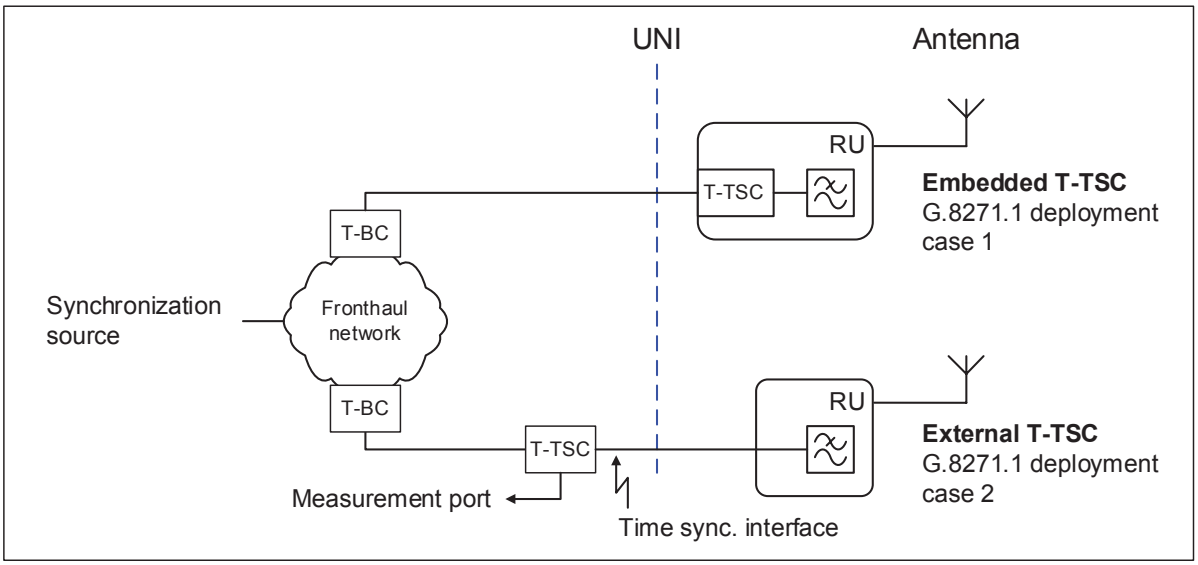

Figure 2: Fronthaul Time Synchronization Deployment Cases

An RU with embedded T-TSC, per deployment case 1, does not need to bear the cost of supporting a time synchronization interface (PPS and TOD) as required for an RU in deployment case 2.

The RU clock at the transmitter antenna port needs to meet 3GPP |TAE| and 3GPP fractional frequency offset (FFO) requirements. The output of a T-TSC might require significant additional low-pass filtering to meet 3GPP FFO requirements. For some embedded T-TSCs, the time clock and the frequency clock might need to be coherent (i.e., from the same source) in which case the T-TSC and additional low-pass filtering functions might need to be implemented by one integrated clock.

If an integrated T-TSC and RU clock uses a low-pass filter with a bandwidth below 50 mHz then the clock will not behave the same as a standalone T-TSC. Further, integrated implementations might not provide a measurement port to observe T-TSC behavior. This situation is acknowledged by G.8273.2 App. IV.

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Radio Unit Time Error Budgets for eCPRI Fronthaul Networks

Figure 3 illustrates a cluster of RUs using synchronization deployment case 1. The T-TSC is on the RU side of the UNI so the RU time error budget from Figure 1 is redefined to include $|TE_{T\text{-}TSC}|$ as shown.

The terms used in Figure 3 are defined as follows:

- $TE_{T\text{-}TSC}$ refers to the time error budget for a T-TSC
- TE_{RU} refers to the time error budget for an RU

Time error budgets in the eCPRI network specification accumulate linearly along a synchronization path.

The eCPRI specification describes two sub-cases for deployment case 1.

Deployment case 1.1

- Regular T-TSC with $|TE_{T\text{-}TSC}|$ budget according to G.8273.2 class B (60 ns)

Deployment case 1.2

- Enhanced T-TSC with $|TE_{T\text{-}TSC}|$ budget equal to 15 ns

Using this information and the |TE| and |TAE| budgets from the eCPRI specification, EQ1. can be used to solve for the $|TE_{RU}|$ budget as shown in Table 1.

Table 1 can be compared to Table 9-3 in [6].

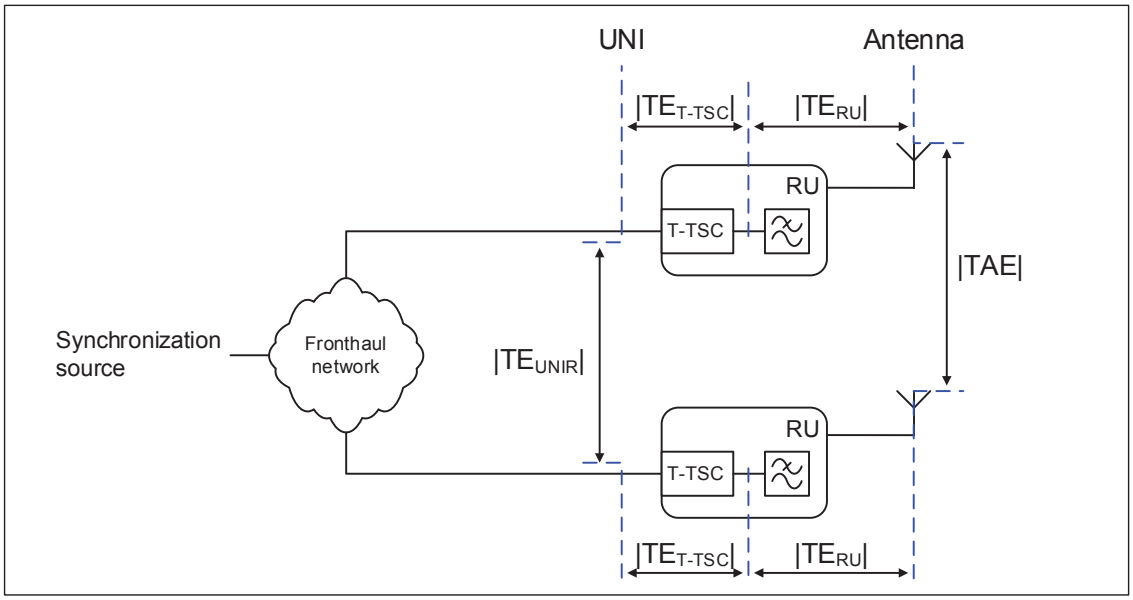

Figure 3: |TE| and |TAE| Reference Points for Synchronization Deployment Case 1

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$$|TE_{RU}| = \frac{|TAE| - |TE_{UNIR}|}{2} - |TE_{T-TSC}|$$

EQ1.

Table 1: Radio Unit Time Error Budget

eCPRI Category	Synchronization Deployment Case	|TAE| [a]	$\|TE_{UNIR}\|$ (Local cluster) [a]	$\|TE_{T\text{-}TSC}\|$	$\|TE_{RU}\|$	$\|TE_{T\text{-}TSC}\| + \|TE_{RU}\|$
Category A	1.1					
	1.2	130 ns	60 ns	15 ns [b]	20 ns	35 ns
Category B	1.1	260 ns	100 ns	60 ns [c]	20 ns	80 ns
	1.2	260 ns	190 ns	15 ns	20 ns	35 ns
Category C [d]	1.1			60 ns	20 ns	80 ns
	1.2			15 ns	20 ns	35 ns

[a] eCPRI network specification, Table 2.

[b] Enhanced T-TSC per eCPRI network specification, Table 2.

[c] Regular T-TSC; G.8273.2 Class B, |cTE| + $|dTE_L|$; the peak-to-peak value of $|dTE_L|$ is used.

[d] For Category C, the respective case 1.1 and case 1.2 values are copied from category A / category B.

Timing Accuracy Category C Time Error Budget Examples

For eCPRI category C, the base stations are not necessarily arranged in clusters and the |TAE| requirement is relaxed compared to the other categories. Figure 4 shows an example of a network that supports eCPRI category C.

The DU is synchronized via network distribution; G.8271.1 reference point C is located at the synchronization input to the DU.

The |TE| terms used in Figure 4 are defined as follows:

- G.8271.1 reference point C, the maximum absolute value time error at this point is 1100 ns
- TE_{DU} refers to the time error budget for a DU
- TE_{FN} refers to the time error budget for a fronthaul network

The overall |TAE| limit for Figure 4 is 3000 ns according to the eCPRI specification. Assuming the network branches have identical time error budgets, EQ3. applies and can be used to work out time error budgets, as shown in the examples in Table 2.

Table 2 can be compared to Table 9-3 in [6].

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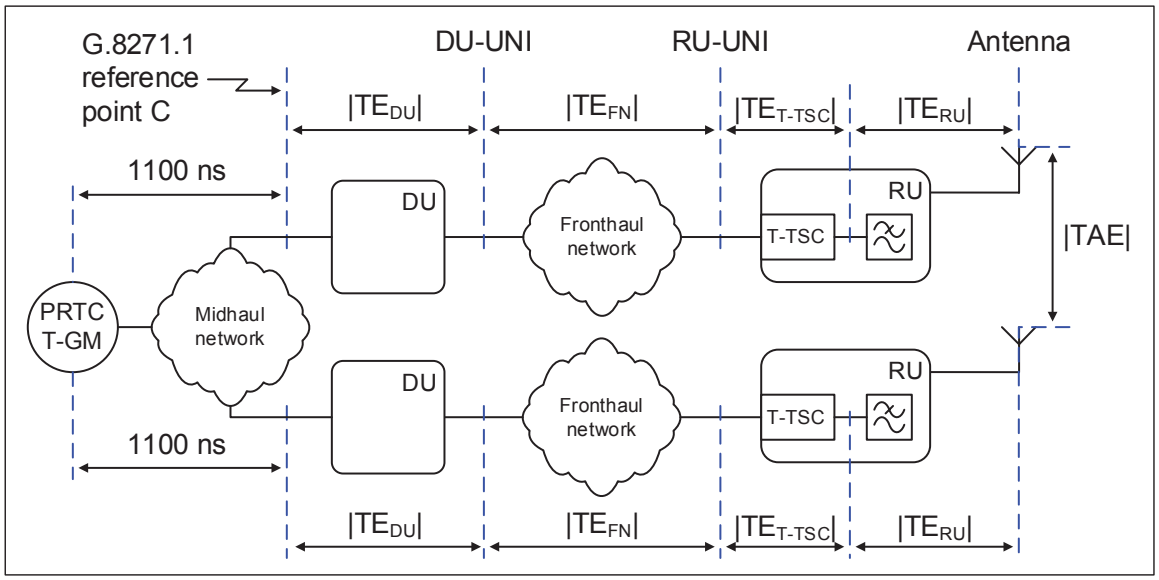

Figure 4: eCPRI Category C Fronthaul |TE| and |TAE| Reference Points

Time error budgets in the eCPRI network specification accumulate linearly along a synchronization path.

$$1100\ ns + |TE_{DU}| + |TE_{FN}| + |TE_{T-TSC}| + |TE_{RU}| = \frac{|TAE|}{2} = 1500\ \text{ns}$$

EQ2

$$|TE_{DU}| + |TE_{FN}| + |TE_{T-TSC}| + |TE_{RU}| = 400\ \text{ns}$$

EQ3.

Table 2: Timing Accuracy Category C Time Error Budget Examples for Deployment Cases 1.1 and 1.2

	|TE| for Reference Point C	**$\|TE_{DU}\|$**	**$\|TE_{FN}\|$**	**$\|TE_{T\text{-}TSC}\| + \|TE_{RU}\|$**	**Notes**
Example 1	1100 ns	225 ns	95 ns	80 ns	95 ns = 190 / 2 ns; like one branch of a fronthaul network capable of eCPRI category B. Deployment case 1.1
Example 2	1100 ns	225 ns	140 ns	35 ns	An enhanced T-TSC leaves more budget for the fronthaul network vs, Example 1. Deployment case 1.2.
Example 3	1100 ns	320 ns	0 ns	80 ns	Point-to-point connection between the DU and RU with no intervening T-BC hops. Deployment case 1.1.

Models for Time Error Accumulation in Fronthaul Networks

The time error budgets in the eCPRI specification accumulate linearly along a synchronization path. Efficient synchronization planning requires more sophisticated methods to estimate time error accumulation for a chain of T-BCs. To this end, G.8271.1 describes simplified and simulation models for time error accumulation.

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Simplified Model for Time Error Accumulation

G.8271.1 App. IV presents the simplified model of time error accumulation in synchronization distribution networks. The analysis decomposes time error into a constant time error component, denoted cTE; and a dynamic time error component, denoted dTE. The analysis further decomposes dTE into a low-pass filtered component denoted dTE_L, and a high pass filtered component denoted dTE_H. The low-pass filter and high-pass filter cut-off frequencies are both 0.1Hz.

- Constant TE is unaffected by clock filters, and it accumulates linearly, T-BC by T-BC, along a synchronization path.
- Dynamic TE_L tends to pass through clock filters, and it accumulates incoherently, T-BC by T-BC, along a synchronization path. Dynamic TE_L accumulates as the square-root of the sum of squares of the individual dTE_L contributions. Depending on the network model, dTE_L can be assumed to be between two extremes: fully symmetric about cTE; and fully asymmetric about cTE. In the symmetric case, the peak value ($dTE_L/2$) contributes for each T-BC; in the asymmetric case, the peak-to-peak value (dTE_L) contributes for each T-BC.
- Dynamic TE_H tends to be filtered by each clock in the chain and only the dTE_H generated by the last clock in the chain contributes to the final TE. Note that dTE_H plays a role in determining frequency error for an RU. Dynamic TE_H is not considered further in this document.

Figure 5 illustrates a fronthaul synchronization network for a cluster of two RUs connected to a common DU. The common DU contains a T-BC. The synchronization chain for each branch is composed of an equal number of T-BCs.[2]

- X represents the number of T-BC hops between the DU and the RU per network branch
- cTE represents the constant time error for each T-BC
- dTE_L represents the dynamic time error, low-pass filtered, for each T-BC
- dTE_{DURL} represents the relative dynamic time error, low-pass filtered, between DU ports
- cTE_{DUR} represents the relative constant time error between DU ports
- dTE_{UNIRL} represents the dynamic relative time error, low-pass filtered, between UNIs
- cTE_{UNIR} represents the relative constant time error between UNIs
- TE_{UNIRL} represents the maximum relative time error, low-pass filtered, between UNIs

Applying the analysis in G.8271.1 App. IV, one can estimate $|TE_{UNIRL}|$ using EQ4, EQ5 and EQ6.

$$|cTE_{UNIR}| \leq 2 * X * |cTE| + |cTE_{DUR}|$$

EQ4

$$|dTE_{UNIRL}| \leq \sqrt{2 * X * |dTE_L|^2 + |dTE_{DURL}|^2}$$

EQ5

$$|TE_{UNIRL}| \leq |cTE_{UNIR}| + |dTE_{UNIRL}|$$

EQ6

[2] The T-BC numbering in Figure 5 is intended to ease comparison with Open RAN documentation; this numbering is different from that used in G.8271.1 App. II.1.3.

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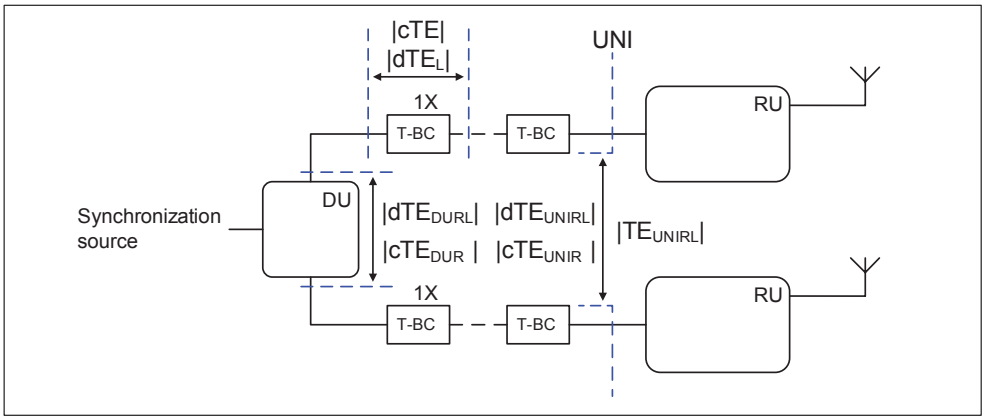

Figure 5: Example Fronthaul Synchronization Network

Table 3 shows results of TE accumulation (|TE_{UNIRL}|) calculations for T-BC classes C and B using the simplified model. For both classes the "X" shown is the maximum number of T-BCs that can be accommodated by the |TE_{UNIRL}| budget while leaving allowance for uncompensated link asymmetry. In these examples, the T-BC in the DU is assumed to be the same class as the T-BCs in the fronthaul network.

Table 3: TE Budgets Using the Simplified Model

eCPRI Category	Deployment Case	|TE_{UNIRL}| Budget	Clock Class	Supported Hops (X) [a]	|cTE_{UNIR}| [b] [c]	|dTE_{UNIRL}| Calculated [d] [e] [f]	|TE_{UNIRL}|	|TE_{UNIRL}| Unused Budget [g]
Cat. B	Case 1.1	100 ns	C	2	52 ns	17 ns	69 ns	31 ns
			B	0	40 ns	14 ns	54 ns	46 ns
	Case 1.2	190 ns	C	7	152 ns	23 ns	175 ns	15 ns
			B	2	120 ns	42 ns	162 ns	28 ns

[a] "X" represents the number of T-BC hops between the DU and RU per network branch. G.8271.1 App. II.1.3 uses "M" to represent the length of a clock chain; M= X+1.

[b] |cTE| is 20 ns for Class B, and 10 ns for Class C.

[c] |cTE_{DUR}| is 40 ns for Class B (G.8271.1 App. XII.5), and 12 ns for Class C.

[d] Using EQ5.

[e] |dTE_L| is 20 ns (peak value) for Class B, and 5 ns (peak value) for Class C.

[f] |dTE_{DURL}| is 14 ns class C; assume the same for class B.

[g] The unused budget is available for uncompensated link asymmetry in the fronthaul network.

The simplified model assumes dTE noise generated by clocks in a synchronization path is uncorrelated and that the measurement filters are ideal. These assumptions trade-off accuracy for simplicity.

Simulation Model for Time Error Accumulation

G.8271.1 App. XII.5 presents the results of a simulation model for dTE accumulation. Using simulation based values for |dTE_{UNIRL}|, one can estimate |TE_{UNIRL}| using EQ4 and EQ6.

Table 4 shows results of TE accumulation (|TE_{UNIRL}|) calculations for T-BC classes C and B using the simulation model. For both classes the "X" shown is the maximum number of T-BCs that can be accommodated by the |TE_{UNIRL}| budget while leaving allowance for uncompensated link asymmetry. In these examples, the T-BC in the DU is assumed to be the same class as the T-BCs in the fronthaul network.

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For deployment case 1.2 using class C T-BCs, the simulation model allows for one less T-BC hop compared to the simplified model. For the other scenarios, the number of T-BC hops is the same as the simplified model, although the unused budgets that are available for uncompensated link asymmetry are different.

Table 4 can be compared to Table H-2 in [6].

G.8271.1 App. XII.5 recommends that the simulation model results should be considered together with the simplified model when studying noise accumulation.

Table 4: TE Budgets Using the Simulation Model

eCPRI Category	Deployment Case	$\lvert TE_{UNIRL} \rvert$ Budget	Clock Class	Supported Hops (X) [a]	$\lvert cTE_{UNIR} \rvert$ [b] [c]	$\lvert dTE_{UNIRL} \rvert$ Simulated [d]	$\lvert TE_{UNIRL} \rvert$	$\lvert TE_{UNIRL} \rvert$ Unused Budget [e]
Cat. B	Case 1.1	100 ns	C	2	52 ns	14 ns	66 ns	34 ns
			B	0	40 ns	14 ns	54 ns	46 ns
	Case 1.2	190 ns	C	6	132 ns	28 ns	160 ns	30 ns
			B	2	120 ns	37 ns	157 ns	33 ns

[a] "X" represents the number of T-BC hops between the DU and RU per network branch. G.8271.1 App. II.1.3 uses "M" to represent the length of a clock chain; M= X+1.

[b] $\lvert cTE \rvert$ is 20 ns for Class B, and 10 ns for Class C.

[c] $\lvert cTE_{DUR} \rvert$ is 40 ns for Class B (G.8271.1 App. XII.5), and 12 ns for Class C.

[d] Using simulation data from G.8271.1 App. XII.5.

[e] The unused budget is available for uncompensated link asymmetry in the fronthaul network.

Conclusion

The time error characteristics of DUs, RUs, and switches and routers have a direct bearing on how many T-BC hops can be supported by the time error budget of a fronthaul network. The greater the number of T-BC hops a fronthaul network can support the lower the number of PRTCs that will be required and the lower the deployment cost. Further, the greater the number of allowed T-BC hops the greater the flexibility in the deployment.

Class C T-BCs are more efficient with time error budgets than Class B T-BCs. As shown in Table 4, both deployment cases 1.1 and 1.2 can benefit from a larger number of T-BC hops when class C clocks are used.

RUs for deployment case 1.2 use enhanced T-TSCs that consume 90 ns less of the TAE budget than the regular T TSCs used for deployment case 1.1. The result, as shown in Table 4, is that enhanced T-TSCs allow up to 4 more T-BC class C hops per branch in category B applications than regular T-TSCs.

Renesas time synchronization hardware and software products support Class C (and better) T-BCs and T-TSCs to meet the tight time error requirements of eCPRI and Open RAN equipment. The product line includes system synchronizers for DUs, switches and routers used in fronthaul networks, and radio synchronizers for RUs.

Renesas synchronizer hardware minimizes constant time error and relative constant time error in single or multi-card systems. The devices include precision time to digital converters to measure internal and external clock skew with picosecond resolution; and they support input-to-output skew control, also with picosecond resolution.

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The Renesas synchronizer devices minimize dynamic time error with digitally controlled oscillators that enable high precision phase and frequency adjustments. In multi-card systems they minimize relative dynamic time error by supporting clocks with embedded pulse per second allowing wideband DPLLs on separate cards to closely track a central synchronizer.

The **Renesas synchronizers** are supported by Linux kernel drivers and Linux PTP so that G.8273.2 clocks can be implemented using only open source software. There is an option to license Renesas proprietary **PTP Clock Manager software** for additional functionality such as packet delay variation filtering.

Renesas also offers a wide range of **jitter attenuators**, **clock generators**, clock synthesizers and **clock buffers** for **wireline** and **wireless timing applications**.

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